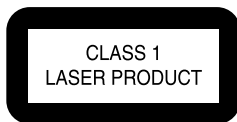


Service
Service
Service



Service Manual



Contents	Page
1 Technical Specifications and Connection Facilities	2
Diversity Matrix	2
PCB Locations	5
2 Safety Information, General Notes	6
3 Directions for Use	8
4 Mechanical Instructions	45
5 Diagnostic Software	49
6 <i>Block Diagrams, Waveforms, Wiring Diagram</i>	89
Wiring Diagram	92
Waveforms	93
Testpoints	97
7 <i>Circuit Diagrams and PWB Layouts</i>	102
Display Panel (Diagram 1)	102
Front Connector (FC) (Diagram 2)	103
Standby Panel (STBY) (Diagram 3)	107
Tray Left Panel (TRL) (Diagram 4)	108
Tray Right Panel (TRR) (Diagram 5)	109
Analog Board: Fronted Video (FV) (Diagram 1)	110
Analog Board: In / Out Video (IOV) (Diagram 2)	111
Analog Board: In / Out Audio (IOA) (Diagram 3)	112
An. Brd for VAE8020: Power Supply (PS) (Diagram 4)	113
An. Brd for VAD8031: Power Supply (PS) (Diagram 5)	114
Analog Board: Multi Sound Processing (MSP) (Diagram 5)	115
Analog Board: VPS (Diagram 6)	116
Analog Board: Follow Me (FOME) (Diagram 7)	116
Analog Board: Digital In/Out (DIGIO) (Diagram 8)	117
Analog Board: Audio Converter 603 3033 (DAC_ADC) (Diagram 9)	118
Analog Board: Audio Converter 603 3028 (DAC_ADC) (Diagram 10)	119

Contents	Page
UP Sub Board: Central Controller (CECO) (Diagram 11)	128
UP Sub Board: Fan Control (FACO) (Diagram 12)	129
DVIO Board: 1394 Interface (Diagram 1)	132
DVIO Board: Link + Codec (Diagram 2)	133
DVIO Board: uP Part (Diagram 3)	134
DVIO Board: Interface + DAC (Diagram 4)	135
DVIO Board: Clock (Diagram 5)	136
Digital Board 1.5: VSM Buffer Memory and Bit Engine Interface (Diagram 1)	140
Digital Board 1.5: AV Dec. STI5519 (Diagram 2)	141
Digital Board 1.5: AV Decoder Mem. (Diagram 3)	142
Digital Board 1.5: Video Enc. Empress (Diagram 4)	143
Digital Board 1.5: VIP CVBS Y/C Video Input (Diagram 5)	144
Digital Board 1.5: Analog Board Cons. Video In/Out (Diagram 6)	145
Digital Board 1.5: Progressive Scan (Diagram 7)	146
Digital Board 1.5: Progressive Scan (Diagram 8)	147
Digital Board 1.5: Power, Clock and Reset (Diagram 9)	148
DB Chrysalis 2.1: IDE, UARTS, RESET, BE (Diagram 1)	155
DB Chrysalis 2.1: 1394 (Diagram 2)	156
DB Chrysalis 2.1: Audio PLL (Diagram 3)	157
DB Chrysalis 2.1: Chrysalis (Diagram 4)	158
DB Chrysalis 2.1: 1.8V Power (Diagram 5)	159
DB Chrysalis 2.1: Prog. scan DAC (Diagram 6)	160
DB Chrysalis 2.1: Flash SDRAM EEPROM (Diagram 7)	161
DB Chrysalis 2.1: Video IO (Diagram 8)	162
DB Chrysalis 2.1: VIPs (Diagram 9)	163
8 Alignments	167
9 Circuit-, IC Descriptions and List of Abbreviations	170
10 Spare Parts List	246
11 Revision List	260

©Copyright 2002 Philips Consumer Electronics B.V. Eindhoven, The Netherlands. All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, or otherwise without the prior permission of Philips.

For service manual of Basic Engine VAE8020 please refer to 3122 785 12473.
For service manual of Basic Engine VAD8031 please refer to 3122 785 13680.



PHILIPS

1. Technical Specifications and Connection Facilities

1.1 Diversity Matrix for sets with drive VAE8020 (AV2)

Type		DVDR	75/001	75/021	75/051	70/001	70/021	70/051
		Version						
		A' Lead	X	X	X			
		A Lead				X	X	X
DVIO		DVIO 1.8	<VN05	<VN05	<VN05			
Digital Board (Chrysalis) 2.1		E1	>VN04	>VN04	>VN04			
		E2				>VN04	>VN04	>VN04
Digital Board (Empress) 1.5		E1	<VN05	<VN05	<VN05	<VN05	<VN05	<VN05
Basic Engine	VAE 8020		X	X	X	X	X	X
UP Sub		AL E1	X	X	X	X	X	X
Analog-Board	3103 603 3033	AL E2/PS			<VN04			<VN04
		AL E1/PS	<VN03	<VN04		<VN03	<VN04	
	3103 603 3028	AL E2			>VN03			>VN03
		AL E1	>VN02	>VN03		>VN02	>VN03	
Display Board		DC1 AL	X	X	X	X	X	

Remarks:

<VN03 ... This module is used in sets with production codes VN01 and VN02. Please see the type plate of the set for the production code.

>VN02 ... This module is used in sets with production code VN03 and higher.

E1 ... Digital Board Chrysalis Version Euro 1 for sets with DV input
 E2 ... Digital Board Chrysalis Version Euro 2 for sets without DV input

AL E1/PS ... Analog Board version A-Lead Euro 1, used from production start onwards.
 AL E2/PS ... Analog Board version A-Lead Euro 2 for UK, used from Production Start onwards.

The Analog Board versions "AL Ex/PS" are based on the PWB layout code 3103 603 3033.
 This layout code can also be seen on the underside of the Analog Board in the copper near the power supply part.

AL E1 ... Analog Board version A-Lead Euro 1 replaces "AL E1/PS" at a certain production date.
 AL E2 ... Analog Board version A-Lead Euro 2 for UK replaces "AL E2/PS" at a certain production date.

The Analog Board versions "AL Ex" are based on the PWB layout code 3103 603 3028.
 The main difference to the Analog Board used at production start is the used audio digital/analogue converter; see Analog Board circuit diagram 9.

1.2 Diversity Matrix for sets with drive VAD8031 (AV3)

Sets with VAD8031 can be identified by the production code starting with VN1A, (then VN1B, VN1C...) and by the presence of a set fan.

Type		DVDR	75/001	75/021	75/051	70/001	70/021	70/051
		Version						
		A' Lead	X	X	X			
		A Lead				X	X	X
Digital Board (Chrysalis) 2.1		E1 /AV3	X	X	X			
		E2 /AV3				X	X	X
BasicEngine	VAD 8031		X	X	X	X	X	X
UP Sub		AL E1/AV3	X	X	X	X	X	X
Analog-Board	use PWB drawing 603 3028	AL E2/AV3			X			X
		AL E1/AV3	X	X		X	X	
Display Board		DC1 AL	X	X	X	X	X	X

1.3 General:

Mains voltage	: 198V-276V
Mains frequency	: 43 Hz - 63Hz
Power consumption mains	: 28 W
Power consumption standby	: < 7 W
Power consumption low power stand-by	: < 3 W

Maximum tuning error of a recalled program	: ± 62.5 kHz
Maximum tuning error during operation	: ± 100 kHz

Tuning Principle

automatic B,G, I, DK and L/L' detection
manual selection in "STORE" mode

1.4 RF Tuner

Test equipment:Fluke 54200 TV Signal generator
Test streams:PAL BG Philips Standard test pattern

1.4.1 System:

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.4.2 RF - Loop Through:

Frequency range	: 45 MHz - 860 MHz
Gain: (ANT IN - ANT OUT)	: -6 dB to 0dB

1.4.3 Radio Interference:

input voltage /3 tone method (+40 dB min)	: no limit
---	------------

1.4.4 Receiver:

PLL tuning with AFC for optimum reception	
Frequency range:	: 45.25 MHz - 857 MHz
Sensitivity at 40 dB S/N	: ≥ 60dBµV at 75Ω (video unweighted)

1.4.5 Video Performance:

Channel 25 / 503,25 MHz,	
Test pattern: PAL BG PHILIPS standard test pattern,	
RF Level 74 dBV	
Measured on SCART 1	
Frequency response:	: 0 - 4.00 MHz +0-4dB
Group delay (0.1 MHz - 4.4 MHz)	: 0 nsec ± 150nsec

1.4.6 Audio Performance:

Audio Performance Analogue - HiFi:

Frequency response at SCART 1 (L+R) output:	
	: 100 Hz - 12 kHz / 0± 3dB
S/N according to DIN 45405, 7, 1967 : and PHILIPS standard test pattern video signal:	
	: FM: ≥ 50dB; AM ≥ 45dB, unweighted
Harmonic distortion (1 kHz, ± 25 kHz deviation):	
	: FM ≤ 1.5%; AM ≤ 2%

Audio Performance NICAM:

Frequency response at SCART 1(L+R) output:	
	: 40 Hz - 15 kHz 0 ± 3dB
S/N according to DIN 45405, 7, 1967 : and PHILIPS standard test pattern video signal:	
	: ≥ 60 dB unweighted
Harmonic distortion (1 kHz):	
	: ≤ 0.5 %

1.4.7 Tuning

Automatic Search Tuning

scanning time without antenna	: typ. 3 min. PAL
stop level (vision carrier)	: ≥ 37dBµV

1.5 Analogue Inputs

1.5.1 SCART 1 (Connected to TV)







Pin Signals:

1	- Audio R	1.8V RMS	
2	- Audio R		
3	- Audio L	1.8V RMS	
4	- Audio GND		
5	- Blue/Chroma		
GND			
6	- Audio L		
7	- Blue out/		
Chroma in	0.7Vpp ± 0.1V into 75 Ohm (*)		
8	- Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD	
9	- Green GND		
10	- P50 control		
11	- Green	0.7Vpp ± 0.1V into 75 Ohm (*)	
12	- Nc		
13	- Red/Chroma		
GND			
14	- fast switch		
GND			
15	- Red out/		
Chroma out	0.7Vpp ± 0.1V into 75 Ohm (*) ± 3dB 0.3Vpp Chroma (burst)		
16	- fast switch		
RGB/ CVBS	or Y <0.4V into 75 Ohm = CVBS >1V / <3V into 75 Ohm = RGB		
17	- Y/CVBS GND		
OUT			
18	- Y/CVBS GND		
IN			
19	- CVBS/Y	1Vpp ± 0.1V into 75 Ohm (*)	
20	- CVBS/Y		
21	- Shield		

1.5.2 SCART 2 (Connected to AUX)

Pin Signals:

1	-Audio R	1.8V RMS	
2	-Audio R		
3	-Audio L	1.8V RMS	
4	-Audio GND		
5	-Blue/Chroma		
GND			
6	-Audio L		
7	-Blue in/		
Chroma out	± 3dB 0.3Vpp Chroma (burst)		
8	-Function switch		
9	-Green GND		
10	-P50 control		
11	-Green		
12	-Nc		
13	-Red/Chroma		
GND			
14	-fast switch		
GND			
15	-Red in/		
Chroma in			

16	-fast switch RGB/ CVBS or Y	
17	-CVBS GND OUT	
18	-CVBS GND IN	
19	-CVBS/Y/RGB sync 1Vpp ± 0.1V into 75 Ohm (*)	
20	-CVBS/Y	
21	-Shield	

(*) for 100% white

Intermodulation distortion	: >70dB
Mute (spin-up, pause, access)	: >85dB
Outband attenuation:	: >40dB above 25kHz

1.8 Digital Output

1.8.1 Coaxial

CDDA/ LPCM (incl MPEG1)	: according IEC958
MPEG2, AC3 audio	: according IEC1937
DTS	: according IEC1937, amendment 1

1.5.3 Audio/Video Front Input Connectors

Audio

Input voltage	: 2 Vrms
Input impedance	: >10kΩ

Video - Cinch

Input voltage	: 1 Vpp ± 3dB
Input impedance	: 75 Ω

Video - YC (Hosiden)

Input voltage Y	: 1Vpp ± 3dB
Input impedance Y	: 75 Ω
Input voltage C	: burst 300 mVpp ± 3 dB
Input impedance C	: 75 Ω

1.6 Video Performance

All outputs loaded with 75 Ohm
SNR measurements over full bandwidth without weighting.

1.6.1 SCART (RGB)

SNR	: > -65 dB on all output
Bandwidth	: 4.8 MHz ± 2dB

1.7 Audio Performance CD

1.7.1 Cinch Output Rear

Output voltage 2 channel mode	: 2Vrms ± 2dB
Channel unbalance (1kHz)	: <1dB
Crosstalk 1kHz	: >95dB
Crosstalk 20Hz-20kHz	: >85dB
Frequency response 20Hz- 20kHz	: ±0.2dB max
Signal to noise ratio	: >95 dB
Dynamic range 1kHz	: >85dB
Dynamic range 20Hz-20kHz	: >80dB
Distortion and noise 1kHz	: >85dB
Distortion and noise 20Hz-20kHz	: >75dB
Intermodulation distortion	: >77dB
Mute	: >95dB
Outband attenuation:	: >40dB above 30kHz

1.7.2 Scart Audio

Output voltage 2 channel mode	: 1.6Vrms ± 2dB
Channel unbalance (1kHz)	: <1dB
Crosstalk 1kHz	: >85dB
Crosstalk 20Hz-20kHz	: >70dB
Frequency response 20Hz- 20kHz	: ± 0.2dB max
Signal to noise ratio	: >85 dB
Dynamic range 1kHz	: >75dB
Dynamic range 20Hz-20kHz	: >70dB
Distortion and noise 1kHz	: >75dB
Distortion and noise 20Hz-20kHz	: >65dB

1.9 Digital Video Input (IEEE 1394)

1.9.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)
Specification of consumer use digital VCR's using 6.3 mm
magnetic tape - dec.1994
Mechanical connection according:
Annex A of 61883-1

1.10 P50 System Control

Via SCART pin nr 10

1.11 Dimensions and Weight

Height of feet	: 10mm
Apparatus tray closed	: WxDxH :435 x 324.5 x 88cm
Apparatus tray open	: WxDxH :435 x 366 x 88cm
Weight without packaging	: app. 4 kg ± 0.5 kg
Weight in packaging	: app. 6.5 kg

1.12 Laser Output Power & Wavelength

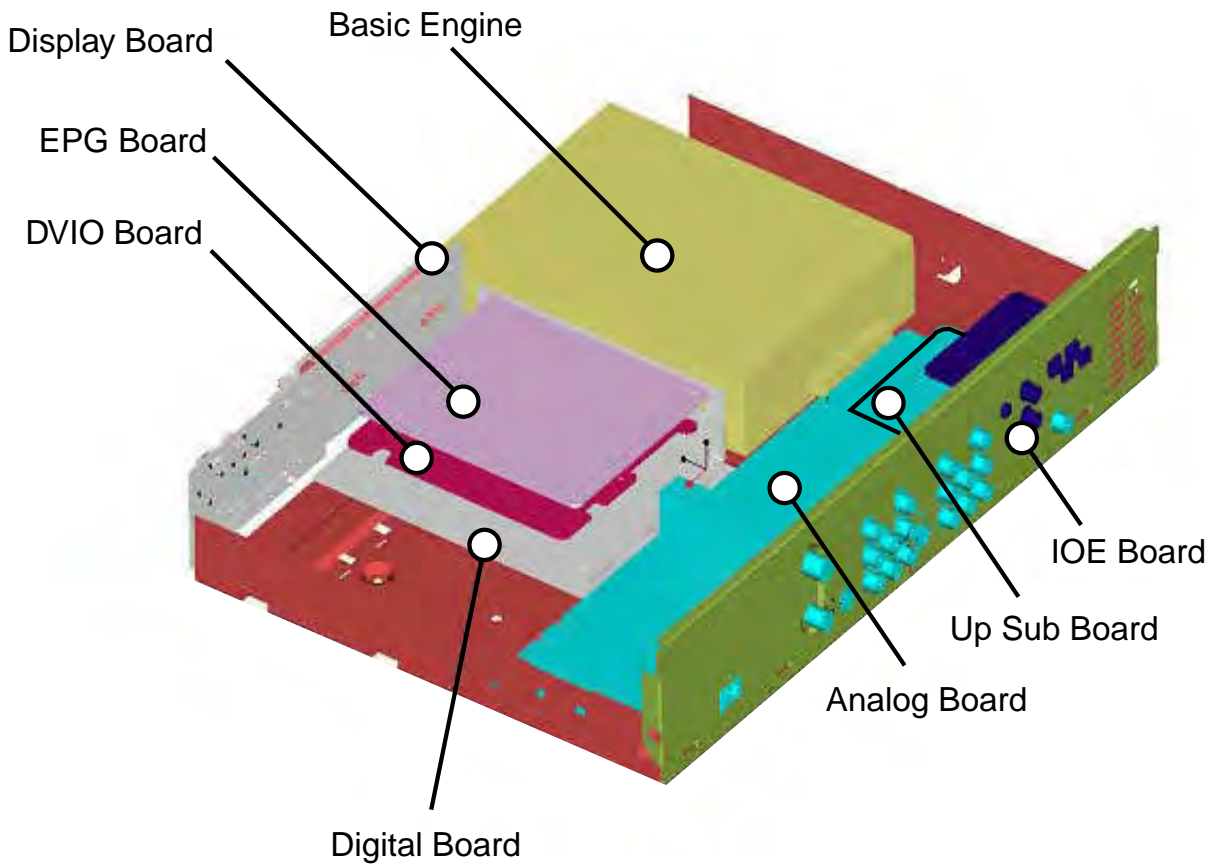
1.12.1 DVD

Output power during reading	: 0.8mW
Output power during writing	: 20mW
Wavelength	: 660nm

1.12.2 CD

Output power	: 0.3mW
Wavelength	: 780nm

1.13 PCB Locations



TR 06002_001
300103

Remarks:

The EPG Board and the In/Out Extension Board IOE are only used in the DVDR80.


The DVIO Board is only present in the DVDR75 and only in combination with the Digital Board 1.5 (Empress). It is not present in DVDR75 with Digital Board 2.1 (Chrysalis).

2. Safety Information, General Notes

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:

- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol , only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:

- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
 1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
 2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
 3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
 4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
 5. Verify this, before you return the unit to the customer/user (ref. UL-standard no. 1492).
 6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	: Semiconductor laser GaAlAs
Wavelength	: 650 nm (DVD) : 780 nm (VCD/CD)
Output Power	: 20 mW (DVD+RW writing) : 0.8 mW (DVD reading) : 0.3 mW (VCD/CD reading)
Beam divergence	: 60 degree

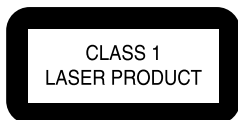



Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential.

Available ESD protection equipment:

- Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
- Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off!'). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
 ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDSÅ UDSÆTTELSE FOR STRÅLING
 ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLING
 VARNING SYNLIG OG OSYNLIG LASERSTRÅLING NÅR DENNA DEL ÅR ÖPPNAD BETRÄKTA EJ STRÅLEN
 VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTT ÖMÄLLE LASER SÄTEILYLLE ÄLÄ KATSO SÄTEESEEN
 VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETZEN
 DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
 ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Figure 2-2

2.2.3 Notes

Dolby

Manufactured under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works.

©1992-1997 Dolby Laboratories, Inc. All rights reserved.



Figure 2-3

Trusurround

TRUSURROUND, SRS and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence from SRS labs, Inc.



Figure 2-4

Video Plus

“Video Plus+” and “PlusCode” are registered trademarks of the Gemstar Development Corporation. The “Video Plus+” system is manufactured under licence from the Gemstar Development Corporation.



Figure 2-5

Macrovision

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.

Use of this copyright protection technology must be authorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

3. Directions For Use

◀◀	Select previous title/search backwards : Briefly press the button during playback: Previous chapter/film or previous title Hold down the button: Search backwards Hold down button during still picture, slow motion backwards
▶▶	Select next title/search forwards : Briefly press the button during playback: Next chapter/film or next title Hold down the button: Search forwards Hold down button during still picture, slow motion forwards
STOP ■	Stop: Stop playback/recording, except with programmed recordings (TIMER) Hold down button, opens and closes the disc tray.
AUDIO	Audio: Select the audio language. For recording language 1 or 2
RECOTR ●	Record: Record the current TV channel
PAUSE II	Pause (still picture): If this button is pressed during playback, the DVD recorder switches to pause. You will see a still picture. If this button is pressed during recording, the DVD recorder will also switch to pause.

Additional TV functions

This will only work with TV sets with the same remote control code (RC5) (e.g. Philips TV sets)

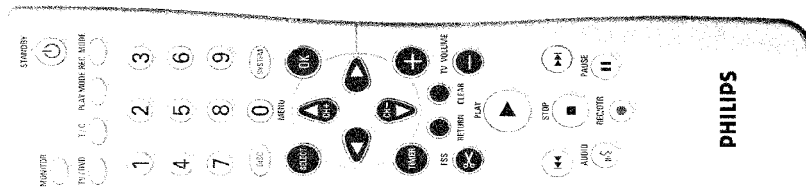
TV VOLUME +	TV volume: Increase TV volume
TV VOLUME -	TV volume: Reduce TV volume

For the following functions you need to hold down the button at the side **DVD/TV** and then select the function you need with the appropriate button.

STANDBY ◊	Switching the TV off:
0.9	Number buttons: 0 - 9
CH+ ▲	TV programme number: To select a higher programme number
CH- ▼	TV programme number: To select a lower programme number

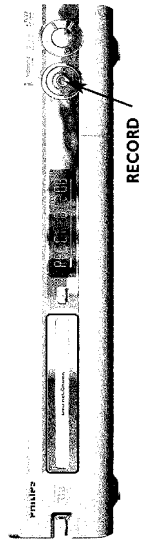
The remote control

MONITOR	Monitor: This button lets you switch between the TV receiver (internal tuner) in the DVD recorder (TV picture on the TV set) and playback on the DVD recorder.
STANDBY ◊	Switch on or off: To switch set on or off; interrupt menu function, interrupt a programmed recording (TIMER)
TV/DVD	TV/DVD switch: Switches the start socket: EXT 2 AUX-IO directly to the TV set. This lets you watch the picture from any unit connected to this start socket (set-top box, video recorder or satellite receiver) and at the same time record from another source. If you have not connected a device to the EXT 2 AUX-IO socket, use this button to switch between TV reception and the DVD recorder. But this only works if you use a start cable to connect the TV set to your DVD recorder (EXT 1 TO TV/IO socket) and your TV set responds to this switch-over.
T/C	Title/Chapter: Choose the T (Title) C (Chapter) directly from the menu bar If HFIT appears in the display, the index menu from a recorded disc or an introductory film will be shown. In this case, this function is not available.
PLAY MODE	Playback type: Choose between repeat, shuffle play and intro-scan
REC MODE	Record type (quality): To select the maximum possible record time
0-9	Number buttons: 0 - 9
DISC-MENU	Disc menu: To show the DVD menu or the index screen
SYSTEM-MENU	System menu: Call up/cancel the main menu (menu bar at the top of the screen)
SELECT	Select: Select function/value
OK	Store/confirm: To store or confirm entry
◀ ▶	Cursor keys: Cursor left, right
CH+ ▲	Cursor buttons/Plus: Cursor up/Next programme number
CH- ▼	Cursor buttons/Minus: Cursor down / Previous programme number
TIMER	TIMER: To make a TIMER programming with ShowView®/without ShowView® or to alter or clear a programmed TIMER
FSS ✕	EDIT: For displaying the edit menu for DVD+R(W) discs, for setting chapter markers
RETURN	Back: Return to previous menu on a video CD (VCD). This also works with some DVDs.
CLEAR	Delete: To delete last entry or clear programmed recording (TIMER)
PLAY ▶	Playback: To play a recorded disc.



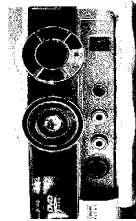
ENGLISH

Front of the device



- STANDBY/ON** **Switch on or off:** To switch off or on, interrupt a programmed recording (TIMER)
- OPEN/CLOSE** **Open/close disc tray:** Open/close disc tray
- RECORD** **Record:** Record the current TV channel
- Playback:** To play a recorded disc
- Select previous title/search backwards
- Select next title/search forwards
- Stop:** Interrupt playback/recording

Behind the flap at the right-hand corner on the front

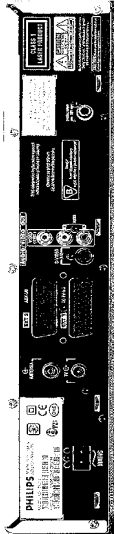


- S-VIDEO** **S-Video socket:** Connection of SVHS/Hi8 camcorders or SVHS/Hi8 video recorders (programme number **CH1**)
- Yellow socket VIDEO** **Video input socket:** Connection of camcorders or video recorders (programme number **CH1**)
- White/red socket left AUDIO right** **Audio input socket left/right:** Connection of camcorders or video recorders (programme number **CH1**)

Switching between the **S-VIDEO** and **VIDEO** sockets takes place automatically. If both sockets are in use, the signal at the **S-VIDEO** socket has priority.

DV IN
i-Link/IDV socket (digital video input, IEEE 1394, FireWire):
 Connecting a digital camcorder or other suitable device (programme number **CH2**).

Back of the unit



- ~MAINS** **Mains socket:** Connection to the mains supply (230V/50Hz)
- ANTENNA IN** **Aerial input:** Connection of the aerial
- TV OUT** **Aerial output:** Connection of the TV set
- EXT 2 AUX-IO** **Scart socket 2:** Connection of an additional device (satellite receiver, set-top box, video recorder, camcorder, etc.)
- EXT 1 TO TV-IO** **Scart socket 1:** Connection of a TV set, RGB output

Output sockets (AUDIO/VIDEO OUT)

- OUT S-VIDEO (V/C)** **S-Video output:** Connection of an S-Video-compatible TV set
- OUT VIDEO** **Video output (yellow socket):** Connecting a TV set with a video input (CVBS, Composite Video)
- OUT L AUDIO R** **Analogue audio output (white/red socket):** Connection of a TV set with audio input sockets or connection of an additional device

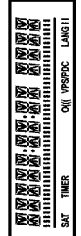
Output socket (DIGITAL AUDIO OUT)

DIGITAL AUDIO OUT **Digital audio output:** Connection of a digital audio device (amplifier/receiver)

The symbols on your DVD recorder display

These symbols can light up on your DVD recorder display:

- Multi-function display/text line
 - Clock
 - Disc/title playing time
 - OTR switch-off time
 - Title name
 - Display of the programme number of the TV channel/playing time/channel name/function
 - Display of information and alerts



EMPTY DISC	The disc inserted is either new or has been completely erased (no recordings).
PROTECTED	The disc is protected against recording.
MAX TITLE	The maximum number of titles per disc has been reached. The maximum number of titles per disc is 46.
MAX CHAP	The maximum number of chapters per title/disc has been reached. The maximum number of chapters per title is 124.
DISC FULL	The disc is full. There is no space for new recordings.
PAL DISC	A disc with PAL recordings has been inserted. The machine is trying to record an NTSC signal. Insert a new disc or one that contains NTSC recordings.
NTSC DISC	A disc with NTSC recordings has been inserted. The machine is trying to record a PAL signal. Insert a new disc or one that contains PAL recordings.
RECORDING	An illegal action (e.g. OPEN/CLOSE button) was attempted during recording.
FREE TITLE	Playback was started for an empty title or the following title is empty.
DISC LOCK	An attempt has been made to record during playback of a protected disc. This message appears if an attempt is made to insert a chapter marker (FSS < button).
DISC ERR	An error occurred when writing the title. If this error keeps occurring please clean the disc or use a new one. For instructions on how to clean a disc see the section on 'Cleaning the disc' in the next chapter.
DISC WARN	An error occurred when writing the title. Recording was continued; the error was skipped.
SETUP	After the automatic search the menu for setting the date/time will appear on the screen.
INIT 01	During the automatic search the TV channels found are counted.
BLOCKED	The disc tray cannot be closed/opened.
SAFE REC	The new recording will be added at the end of all the other recordings (SAFE RECORD).
ESCALINK	Data is being transferred from the 'EasyLink' TV.
POST-FORMAT	Post-format.

ENGLISH

	Disc bar: Displays the current position on the disc (disc pointer). Play/Record: Single flashing segment at the current position. Pause: Flashing segment on both sides of the current position. Stop: Illuminated segment at the current position.
SAT	A satellite recording has been programmed.
TIMER	A recording (timer) has been programmed.
o(((A remote control signal has been received.
VPS/PDC	Video programming system / programme delivery control. A VPS or PDC code will be transmitted for the selected TV program.
LANG II	During playback a HiFi/2 channel tone was detected or a HiFi/2 channel tone was received. 'I' or 'II' lights up depending on which sound channel has been selected.

Messages in the DVD recorder display

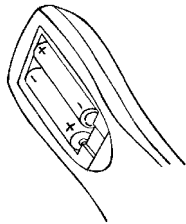
READING

The following messages may appear in your DVD recorder display

DISC TRAY	The DVD recorder is in initial installation mode. Switch the TV on, then read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.
NO SIGNAL	No input signal available (signal inadequate or unstable)
MENU	The menu on the screen is active
OPENING	Disc tray opening
TRAY OPEN	Disc tray open
CLOSING	Disc tray closing
READING	Disc being read
MENU UPDT	Once recording has been successfully completed the table of contents is created.
INIT MENU	The menu structure is created after the first recording has been made on a new disc
COPY PROT	You have tried to copy a copy-protected DVD/video cassette.
INIT	Please wait until this message disappears. The DVD recorder is busy performing a task.
NO DISC	A disc has not been inserted for recording. If a disc has been inserted, it cannot be read.
INFO	Information about the inserted DVD is displayed on the screen
BUSY	The DVD recorder is processing the changes to make them DVD compatible
ERASING	The entire disc is erased

Connecting the DVD recorder

Preparing the remote control for operation



The remote control and its batteries are packed separately in the original DVD recorder packaging. You must install the batteries in the remote control before use - described in the following section.

- 1 Take the remote control and the enclosed batteries (2 batteries).
- 2 Open the battery compartment, insert the batteries as shown and then close the battery compartment.

The remote control is now ready to use. Its range is approximately 5 to 10 meters.

'Aim' correctly

In the following sections, you will need the remote control for the first time. Aim the remote control at the DVD recorder and not at the TV set.



Tip

Connecting your DVD recorder to the TV set

The necessary cable connections must be made before you can record or playback TV programmes using your DVD recorder.

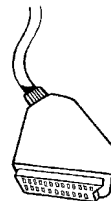
Connect the DVD recorder **directly** to your TV set. If there is a video recorder in between the picture quality may be poor.

We recommend that you use a scart cable to connect your TV set and DVD recorder.



What is a scart cable?

The scart or Euro AV cable serves as the universal connector for picture, sound and control signals. With this type of connection, there is practically no loss of quality in picture or sound transmission.



ENGLISH

When you install your DVD recorder for the first time, select one of the following options:

'Connecting with a scart cable and Easy Link'

If your TV set is equipped with 'Easy Link', Cinema Link, NextView Link, Q-Link, Smart Link, MegaLink, Datalink, ... and you wish to use a scart cable.

'Connecting with a scart cable without Easy Link'

If your TV set is not equipped with 'Easy Link', Cinema Link, NextView Link, Q-Link, Smart Link, MegaLink, Datalink, ... and you wish to use a scart cable.

'Connecting with an S-Video(Y/C) cable'

If your TV set is equipped with an S-Video(SVHS) socket.

'Connecting with video(CVBS) cable'

If your TV set is equipped only with an video(CVBS) socket.

Connecting with a scart cable and 'Easy Link'

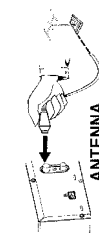
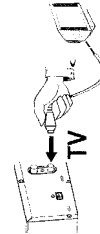
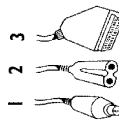


Your DVD recorder can exchange information with your TV set using 'Easy Link'. Your TV channels can also be transferred in the same order from your TV set to your DVD recorder using 'Easy Link'.

Please see your TV's operating instructions.

Have the following cables ready:

an aerial cable (1, supplied), a mains cable (2, supplied), a special scart cable (3, suitable for Easylink).



1 Switch off your TV set.

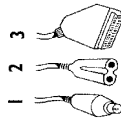
2 Remove the aerial cable plug from your TV set. Insert it into the ANTENNA IN socket at the back of the DVD recorder.

3 Insert one end of the supplied aerial cable into the TV OUT socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.

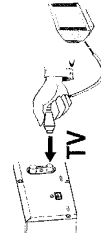
4 Plug in a special scart cable (for Easylink) into the scart socket. EXT 1 TO TV-IO at the back of the DVD recorder and the corresponding scart socket at the back of the TV set (see TV set operating instructions).

Connecting with a scart cable without 'Easy Link'

Have the following cables ready: an aerial cable (1. supplied), a mains cable (2. supplied), a scart cable (3).



1 Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA IN** socket at the back of the DVD recorder.



2 Insert one end of the supplied aerial cable into the **TV OUT** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.



3 Plug a scart cable into the scart socket. **EXT 1 TO TV-IO** at the back of the DVD recorder and the scart socket for the DVD recorder at the back of the TV set (see TV set operating instructions).

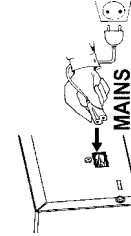


My TV set has several scart sockets. Which one should I use?
Select the scart socket that is suitable for both video output and for video input.
My TV set shows me a selection menu for the scart socket.
Select 'VCR' as the source for this scart socket.



4 Switch on the TV set.

5 Insert one end of the supplied mains cable into the mains socket **~MAINS** at the back of the DVD recorder and the other end into the wall socket.



The most important features of the DVD recorder will appear in scrolling text on the display. After the first installation is completed this function will be switched off. How you switch on this function again, read in the chapter 'User preferences' in the section 'standby'.

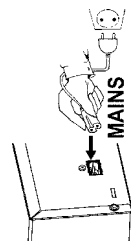
6 Switch on the DVD recorder using **STANDBY/ON** . '15 TV ON' will appear on the display.

7 If the connection was properly made and your TV was automatically switched to the programme number for the scart socket, e.g. 'EXT', '0', 'AV', you will see the following picture:

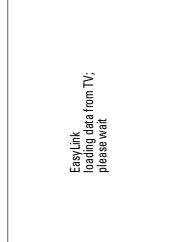
ENGLISH

5 Switch on the TV set.

6 Insert one end of the supplied mains cable into the mains socket **~MAINS** at the back of the DVD recorder and the other end into the wall socket.



7 A message appears on the screen announcing that the transfer has started. **English data from TV; please wait.** The TV set transfers all saved TV channels, in the same order, to the DVD recorder. This may take several minutes.



x 'Time', 'Year', 'Month', 'Date' appears on the TV screen
Normally the date and time are taken from the data sent by the TV channel stored on programme P01. If the aerial signal is too weak or there is excessive interference, you should set the date and time manually.

- 1 Check if the time in 'Time' is correct.
- 2 If you need, change the time with the number buttons 0..9 on your remote control.
- 3 Select the next line with **CH+▲** or **CH-▼**.
- 4 Check if the displayed settings for 'Year', 'Month' and 'Date' are correct.
- 5 When all information is correct, save by pressing **OK**.



Problem

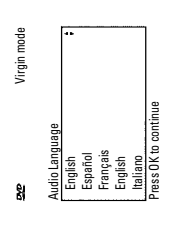
x I can see more installation menus on my TV set
Not all the necessary data has been transferred. Please enter the settings by hand as follows. For more information on the various functions see 'Initial installation' in 'Installing your DVD recorder'.

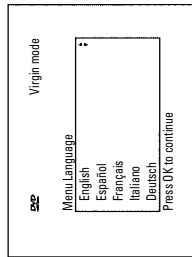
- 1 Select the desired audio language using **CH-▼** or **CH+▲** and confirm with **OK**.
- 2 Select the desired subtitle language with **CH-▼** or **CH+▲** and confirm with **OK**.
- 3 Select the desired screen format: position using **CH-▼** or **CH+▲**.
'4:3 letterbox' For a 4:3 TV set; cinema format (black bars above and below the picture)
'4:3 panscan' For a 4:3 TV set; full height format with the sides cut off
'16:9' For a 16:9 TV set.
- 4 Confirm with **OK**.
- 5 Select the country of your residence with **CH-▼** or **CH+▲**. If your country does not appear, select **'Other'**.
- 6 Confirm with **OK**.



Problem

Initial installation is now complete.





Problem

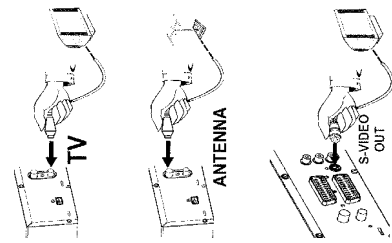
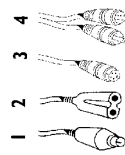
*** My screen is empty.**

- ✓ Many TV sets are switched by the DVD recorder to the programme number for the start socket by way of a control signal sent through the start cable.
- ✓ If the TV set does not automatically switch to the start socket programme number, manually change to the corresponding programme number on your TV set (see your TV's operating instructions).
- ✓ Check that the start cable is connected from the TV set to the **EXT 1 TO TV/IO** socket on the DVD recorder. The **EXT 2 AUX-IO** socket is intended only for additional devices.

Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

Connecting with an S-Video(Y/C) cable

This connecting cable, also known as the SVHS cable, is used to transmit the brightness signal (Y signal) and colour signal (C signal) separately. This mini DIN socket/plug is also called a Hosiden socket/plug.

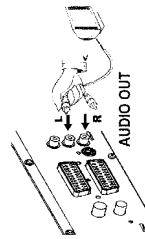


Have the following cables ready:
 an aerial cable (1, supplied), a mains cable (2, supplied), an S-Video(SVHS) cable (3), an audio cable (4, supplied, red/white plug).

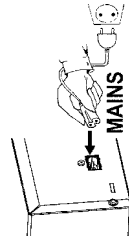
1 Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA IN** socket at the back of the DVD recorder.

2 Insert one end of the supplied aerial cable into the **TV OUT** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.

3 Insert one end of an S-Video(SVHS) cable into the **OUT S-VIDEO** (Y/C) socket at the back of the DVD recorder and the other end into the S-Video (SVHS) input socket on the TV set (usually labelled 'S-Video in' or 'SVHS in'. See TV operating instructions).



4 Insert one end of the supplied audio (Cinch) cable into the red/white Cinch socket **OUT L AUDIO R** at the back of the DVD recorder and the other end into the audio input socket (usually red/white) on the TV set (usually labelled 'Audio in' or 'AV in'. See TV operating instructions).



6 Insert one end of the supplied mains cable into the mains socket **^MAINS** at the back of the DVD recorder and the other end into the wall socket.

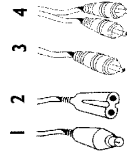
The most important features of the DVD recorder will appear in scrolling text on the display. After the first installation is completed this function will be switched off. How you switch on this function again, read in the chapter 'User preferences' in the section 'standby'.

7 Switch on the DVD recorder using **STANDBY/ON**. 15 TV **DM²** will appear on the display.

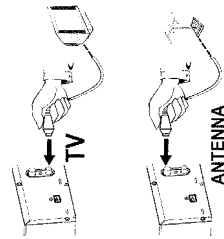
Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

Connecting with video(CVBS) cable

This cable, usually with yellow Cinch connectors, is used for transmitting the Composite Video signal (FBAS, CVBS). In this method of transmission the colour signal and the brightness signal are transmitted on the same cable. In certain circumstances, this can lead to problems with the picture, such as 'Moiré' patterns.



Have the following cables ready:
 an aerial cable (1, supplied), a mains cable (2, supplied), a video (CVBS)cable (3, supplied, yellow plug), an audio cable (4, supplied, red/white plug).

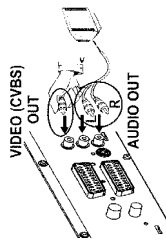


1 Remove the aerial cable plug from your TV set. Insert it into the **ANTENNA IN** socket at the back of the DVD recorder.

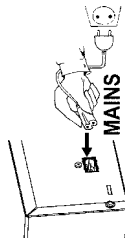
2 Insert one end of the supplied aerial cable into the **TV OUT** socket at the back of the DVD recorder and the other end into the aerial input socket at the back of the TV set.

3

Connecting additional devices



- 3 Insert one end of the supplied video (CVBS) cable into the yellow Cinch socket **OUT VIDEO (CVBS)** at the back of the DVD recorder and the other end into the video input socket (usually yellow) on the TV set (usually labelled 'Video in' or 'AV in'. See TV operating instructions).
- 4 Insert one end of the supplied audio (Cinch) cable into the red/white Cinch socket **OUT L AUDIO R** at the back of the DVD recorder and the other end into the audio input socket (usually red/white) on the TV set (usually labelled 'Audio in' or 'AV in'. See TV operating instructions).
- 5 Switch on the TV set. Switch the TV set over to the Video/Audio input socket or select the relevant programme number. Please see your TV's operating instructions for the programme number you need.

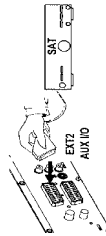


- 6 Insert one end of the supplied mains cable into the mains socket **MAINS** at the back of the DVD recorder and the other end into the wall socket.
The most important features of the DVD recorder will appear in scrolling text on the display. After the first installation is completed this function will be switched off. How you switch on this function again, read in the chapter 'User preferences' in the section 'standby'.
- 7 Switch on the DVD recorder using **STANDBYON** (⏻) on the display. will appear on the display.

Then, read the paragraph on 'Initial installation' in 'Installing your DVD recorder'.

ENGLISH

Connecting additional devices to the second scart socket



You can connect additional devices such as decoders, satellite receivers, camcorders, etc. to the **EXT 2 AUX-IO** socket. When playback is started on this additional device the DVD recorder automatically connects the **EXT 2 AUX-IO** socket with the **EXT 1 TO TV-IO** scart socket. You will then see the picture from the additional device on your TV set, even if the DVD recorder is switched off.
The **TV/DVD** button on the remote control allows you to switch between playback through the **EXT 2 AUX-IO** scart socket and playback from the DVD recorder.

Connecting additional video recorders

You can connect a video recorder to the **EXT 2 AUX-IO** socket. If you have an SVHS video recorder you can also use the **OUT S-VIDEO (VS)** socket and the **OUT L AUDIO R** sockets.

Please note:

Most prerecorded video cassettes and DVDs are copy-protected. If you try to copy them you will see the message 'COPY PROTECT' on the DVD recorder's display.

<ul style="list-style-type: none"> ✓ When copying video cassettes the display on the DVD recorder shows 'COPY PROTECT'. ✓ Check that the cable is plugged in firmly. ✓ If a recording is made from a video recorder, change the tracking on the video recorder. ✓ The DVD recorder may not be able to recognise the video input signal if this signal is poor or does not comply with relevant standards. 	
<ul style="list-style-type: none"> ✗ When I copy DVD video discs or prerecorded video cassettes the picture is fuzzy and the brightness varies ✓ This happens if you try to copy DVDs or video cassettes that have been copy-protected. Even though the picture on the TV is fine the recording on a DVD-R(W) is faulty. This interference is unavoidable with copy-protected DVDs or video cassettes. 	<p>Problem</p>

Connecting audio devices to the digital audio socket



At the back of the DVD recorder there is a digital audio output socket **DIGITAL AUDIO OUT** for an coaxial cable.

- These can be used to connect the following:
- an AV receiver or an AV amplifier with a digital multi-channel sound decoder
 - a receiver with two-channel digital stereo (PCM)

Digital multi-channel sound

Digital multi-channel sound offers the best possible sound quality. You will need a multi-channel AV receiver or amplifier that supports at least one of the audio formats of the DVD recorder (MPEG2, Dolby Digital and DTS). Consult the operating instructions for your receiver to find out which audio formats it supports.



Problem

* All I can hear from my loudspeakers is a loud distorted noise


✓ The receiver is not compatible with the digital audio format of the DVD recorder. The audio format of the DVD disc is displayed in the status window when you switch to another language. Playback in six-channel digital surround sound is only possible if the receiver has a digital multi-channel sound decoder.

Connect camcorder to the front sockets

To copy camcorder recordings, you can use the front sockets. These sockets are located behind the flap on the left-hand side.

Best picture quality

If you have a DV or Digital 8 camcorder, connect the **DV IN** input of the DVD recorder to the appropriate DV output on the camcorder.

When films are transferred the original recording data and time are stored as DVD subtitles. On playback, this data can be displayed on the TV screen by using the  function (Subtitle).

Very good picture quality

If you have a Hi8 or S-VHS(C) camcorder, connect the **S-VIDEO** input of the DVD recorder to the appropriate S-VHS output on the camcorder.

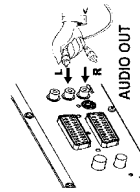
You must also connect the audio input **left AUDIO right** on the DVD recorder to the audio output on the camcorder.

Good picture quality

If you have a camcorder that only has a single video output (Composite Video, CVBS), connect the **VIDEO** input on the DVD recorder to the appropriate output on the camcorder.

You must also connect the audio input **left AUDIO right** on the DVD recorder to the audio output on the camcorder.

Connecting audio devices to the analogue audio sockets



Two audio output sockets **OUT L-AUDIO R** are located on the back of the DVD recorder (audio signal output left/right)

These can be used to connect the following:

- a receiver with **Dolby Surround Pro Logic**
- a receiver with **two-channel analogue stereo**

Can I use the 'Phono' input on my amplifier?

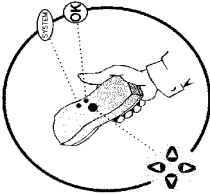
This socket (input) on the amplifier is designed only for record players without preamplifiers. Do **not** use this input for connecting the DVD recorder.

The DVD recorder or the amplifier may be damaged as a result.



ENGLISH

Installing your DVD recorder



Initial installation

After successfully connecting your DVD recorder to the TV set and other additional devices as described in the previous chapters, this chapter will show you how to start the initial installation. The DVD recorder automatically seeks out and stores all available TV channels.

ENGLISH



Connecting additional devices

If you have connected additional devices such as a satellite receiver to the aerial cable, switch them on. The automatic channel search will recognise it and save it.

No aerial connected

Even if you only want to use the DVD recorder to play back or have only connected a satellite receiver, you must still complete the initial installation. This is necessary so that the basic settings are stored correctly. Once initial installation is complete you can use the DVD recorder as normal.

Tip



Select the desired language for the on-screen menu by pressing **CH-▼** or **CH+▲**.

What is an onscreen menu?

The multi-language onscreen menu takes the mystery out of using your new DVD recorder. All settings and/or functions are displayed on your TV screen in the relevant language.

Confirm with **OK**.



Select the desired audio language using **CH-▼** or **CH+▲**.

What is an audio language?

The DVD will play the sound in the language you select, provided this language is available on the disc. If it is not available on the disc the first language on the DVD will be used instead. The DVD Video Disc menu, if available, will also be displayed in the language you select.

Confirm with **OK**.



Select the desired language for the subtitles by pressing **CH-▼** or **CH+▲**.

What is the subtitle language?

The subtitles will be displayed in the language you select, provided this language is available on the disc. If it is not available on the disc the first language on the DVD will be used instead.

Confirm with **OK**.

Virgin mode

Menu Language

- English
- Español
- Français
- Italiano
- Deutsch

Press OK to continue

Virgin mode

Audio Language

- English
- Español
- Français
- English
- Italiano

Press OK to continue

Virgin mode

Subtitle Language

- English
- Español
- Français
- English
- Italiano

Press OK to continue

7

Virgin mode

TV Shape

- 4:3 letterbox
- 4:3 panscan
- 16:9

Press OK to continue

Select the desired screen format position using **CH-▼** or **CH+▲**. These settings will only be used if you insert a DVD that contains this information.

Which screen formats can I select?

4:3 letterbox for a 'wide-screen' (cinema format) picture with black bars at the top and bottom.

4:3 panscan for a full-height picture with the sides trimmed.

16:9 for a wide-screen TV set (screen edge ratio 16:9)



Confirm with **OK**.

8

Virgin mode

Country

- Austria
- Belgium
- Denmark
- Finland
- France

Press OK to continue

Select the country of your residence with **CH-▼** or **CH+▲**. If your country does not appear, select **Other**.

Why do I have to select a country?

To call up the specific settings for the respective country, you must first install the country.



Confirm with **OK**.

9

After you connect the aerial (or cable TV, satellite receiver, etc.) to the DVD recorder, press **OK**. The automatic TV channel search starts. **HFi iTV** will appear on the display.

Installation

Autom. search

Searching for TV channels

00 Channels found

Please wait



* The DVD recorder cannot find any TV stations

✓ Select channel 1 on the TV set. Can you see the stored TV channel on the TV set?

If not, check the cable connection from the aerial (aerial socket) to the DVD recorder and to the TV set.

✓ Please have patience.

The DVD recorder searches the entire frequency range in order to find and save the largest possible number of TV channels.

✓ If you have not connected an aerial, go through all the basic settings right to the end and then, if you wish, start the automatic search (see 'Automatic TV station search').

Problem

10

When the automatic TV channel search is complete, **Autom. search complete** will appear on the TV screen. **'Time', 'Year', 'Month', 'Date'** will then appear on the TV screen.

11

Check if the time in **'Time'** is correct

12

If required, change the time with the number buttons **0..9** on your remote control.

13

Select the next line with **CH+▲** or **CH-▼**.

14

Autom. search

Autom. search complete

00 Channels found

Time 2001

Year 2008

Month 01

Date 01

To continue Press OK

15

- 16 Check if the displayed settings for 'Year', 'Month' and 'Date' are correct.
- 17 When all information is correct, save by pressing **OK**.

The initial installation is now complete.

Satellite receiver

If you are connecting a satellite receiver, please read the section on 'Using a satellite receiver'.

Decoder

If you are connecting a decoder, you must install it as described in the next section.

Tip

* **Sound may be distorted on some TV channels.**

✓ If the sound is distorted on any of the stored TV channels or if there is no sound at all, the wrong TV system may have been stored for the TV channel. Read 'Manual TV channel search' for information on how to change the TV system.

Problem

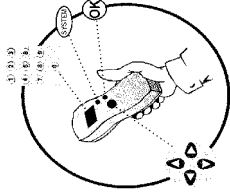
Using a satellite receiver

TV channels from a satellite receiver (connected to scart socket **EXT 2 AUX-I/O**) are received on the DVD recorder on programme number **EXT2**.

If necessary, use the **MONITOR** button to switch to the internal tuner. Select programme number **EXT1** with **0** on the remote control and then select programme number **EXT2** with **CH-▼**. You should select the TV channels to be received by the satellite receiver directly on the receiver itself.

Allocating a decoder

Some TV channels send coded TV signals that can only be viewed properly with a purchased or rented decoder. You can connect such a decoder (descrambler) to your DVD recorder. The following function automatically activates the connected decoder for the TV channel you want to watch.



How do I allocate the decoder for Easy Link?

If your TC-V set supports 'Easy Link', the decoder must be assigned to the relevant TV channel on the TV set (see the operating instructions for your TV set). Settings cannot then be made in this menu.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Use the **CH+▲** and **CH-▼** buttons or the number buttons **0-9** on the remote control to select the TV channel for which you want to use the decoder. If necessary, use the **MONITOR** button to switch to the internal tuner.
- 4 Press the **SYSTEM-MENU** button on the remote control. The menu bar appears.
- 5 Select **TA** symbol with **◀** or **▶**.
- 6 Select **'Installation'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 7 Select **'Manual search'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 8 Select **'Decoder'** using **CH-▼** or **CH+▲**.
- 9 Select **'On'** with **◀** or **▶**.

How do I switch the decoder off again?

Use **▶** to select **Off** in the **Decoder** line on the screen (Decoder off).

Confirm with **OK**.

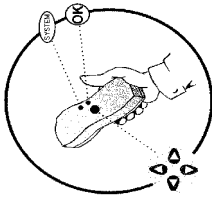
To end, press **SYSTEM-MENU**.

Installation	CH
Manual search	01
Channel/freq.	BBC1
Entry/search	Off
Programme number	Off
TV system	PAL-BG
Decoder	On
NICAM	0
Fine tuning	To stop Press OK

Your decoder has now been allocated to this TV channel.

Manual TV channel search

In some cases, not all of the available TV channels may have been found and stored during initial installation. In this case, you will need to search for and store the missing or coded TV channels manually.



ENGLISH



Tip

Manual search with EasyLink

With 'Easy Link', the DVD recorder will automatically download the TV channels stored on the TV set. This is why some lines have no function. To store new TV channels, they must first be stored on the TV set. The information will then be transferred to the DVD recorder automatically.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 4 Select **TV** symbol with **◀** or **▶**.
- 5 Select **'Installation'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Select **'Manual search'** using **CH-▼** or **CH+▲** and confirm with **▶**.

Installation	
Manual search	
Channel/freq.	CH
Entry/search	01
TV channel number	BBC1
TV channel name	0ff
Decoder	PAL-BG
TV system	0
NICAM	TV, stereo
Fine tuning	Press OK



Problem

***I don't know the channel for my TV station**
 ✓ In this case, press **▶** to start the automatic search. A changing channel number/frequency number will appear on the TV screen. Continue the automatic search until you have found the TV channel you are looking for.

Using **◀** or **▶** in **'Programme number'**, select the programme number you want to use for the TV channel, e.g. **01**.

How can I change the symbol of a TV channel?

- 1 In **'TV channel name'**, press **▶**.
- 2 Select the desired symbol position using **◀** or **▶**.
- 3 Change the symbol at the symbol position with **CH-▼** or **CH+▲**.
- 4 Select the next symbol position in the same way.
- 5 Keep pressing **▶** until the cursor disappears.



Tip

How can I change the TV system of the TV channel?

In **'TV system'**, use **◀** or **▶** to select the TV system that produces the least distortion of picture and sound.

What is NICAM?

NICAM is a digital sound transmission system. Using NICAM, you can transmit either 1 stereo channel or 2 separate mono channels. However, if reception is poor and the sound distorted you can turn off NICAM. In **'NICAM'**, select **'Off'** using **◀** or **▶**.

How can I improve the automatic process for storing channels?

To change the automatic process for storing channels (fine tuning), select **'Fine tuning'**. Using **◀** or **▶** you can try to fine-tune the TV channel manually.



Tip

- 10 Press **OK** to store the TV channel.
- 11 To search for other TV channels, begin again at **8**.
- 12 To end, press **SYSTEM-MENU**.

Sorting TV channels automatically (Follow TV)

When the automatic channel search function is activated, the TV channels are stored in a specific order. This may differ from the order in which the TV channels appear on your TV set. This function changes the order of the TV channels stored in your DVD recorder to match the order on the TV set.

This only works if the DVD recorder (**EXT 1 TO TV/IO** socket) and the TV set are connected with a **scart cable**.



Tip

What does EasyLink do?

If your TV set supports 'EasyLink', TV channels will be stored during initial installation in the same order as they appear on the TV set. To store the TV channels in a different order, you'll need to change the order on the TV set. When you start the Follow TV function the information is transferred again from the TV set.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.

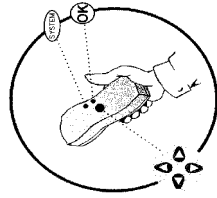
Automatic TV channel search

During installation, all available TV channels are searched for and stored. If the channel assignments of your cable or satellite TV provider change or if you are reinstalling the DVD recorder, e.g. after moving house, you can start this procedure again. This will replace the stored TV channels with the new ones.

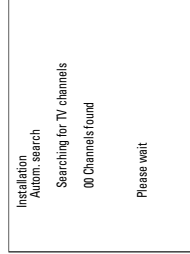


What does Easy Link do?

With EasyLink, you can search for and store TV channels only on the TV set. These settings are accepted by the DVD recorder. Use this function to start the transfer of TV channels from the TV set.



- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 4 Select **TV** symbol with **◀** or **▶**.
- 5 Select **Installer** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Select **Autom. search** using **CH-▼** or **CH+▲**.
- 7 Press **▶**.
- 8 The automatic TV channel search starts. This allows the DVD recorder to save all available TV channels. This procedure may take several minutes.
- 9 When all the TV channels have been found, **Autom. search complete** will appear on the TV screen.
- 10 To end, press **SYSTEM-MENU**.



You can read about how to search for a TV channel manually in 'Manual TV channel search'.

- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press the **SYSTEM-MENU** button on the remote control. The menu bar appears.
- 4 Select **TV** symbol with **◀** or **▶**.
- 5 Select **Installer** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Select line **Follow TV** with **CH-▼** or **CH+▲**, and confirm with the **▶** button.
- 7 Confirm the message on the screen with **OK**. **TV** will appear in the DVD recorder display.
- 8 Select programme number **1** on the TV set.



Problem

x I cannot switch my TV set to programme number '1'.
 ✓ If you have connected additional devices to the **EXT 2 AUX/IO** socket, please disconnect these devices. Other connected devices may have switched the TV set to the programme number of the start socket.

- 9 Confirm with **OK** on the DVD recorder remote control. **TV 01** will appear in the display. The DVD recorder compares the TV channels on the TV set and the DVD recorder. If the DVD recorder finds the same TV channel as on the TV set it stores it as 'P01'.



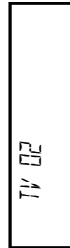
x **HEI!** will appear in the display. The DVD recorder is not receiving a video signal from the TV set.
 ✓ Check the connectors at both ends of the start cable.
 ✓ Check your TV's operating instructions to see which start socket is used for video signals.
 ✓ If the problem persists, you won't be able to use this feature. Please read 'Adding and clearing TV channels manually'.

Problem



Wait until for example **TV 02** appears in the display.

- 10 Wait until for example **TV 02** appears in the display.
- 11 Select the next programme number on the TV set, e.g. '2'.
- 12 Confirm with **OK** on the DVD recorder remote control.



Deleting sorting

You can delete incorrect TV channel sorting by pressing **◀**.

Tip

- 13 Repeat steps 10 to 12 until you have assigned all the TV channels.
- 14 To end, press **SYSTEM-MENU**.

Adding and clearing TV channels manually

After you have performed the automatic channel search you may not agree with the sequence in which the individual TV channels have been allocated to the programme positions (programme numbers). You can use this function to rearrange the TV channels already stored or to delete TV channels you don't want or those with poor reception.

EasyLink

With EasyLink you can search for and store TV channels only on the TV set. These settings are then accepted by the DVD recorder. That is why you cannot select this function manually.

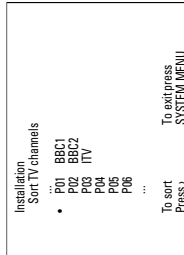
The teletext clock resets automatically

If you store a TV channel which transmits TXT/PDC on programme number 'P01', the date and time will automatically be transmitted and constantly updated. As a result, the changes from summer time to winter time and back again will be made automatically.



Tip

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder. Press the **SYSTEM-MENU** button on the remote control. The menu bar appears.
- 3 Select **TV** symbol with **◀** or **▶**.
- 4 Select **'Installation'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 5 Select **'Sort TV channels'** using **CH-▼** or **CH+▲** and confirm with **▶**.



Tip

- 6 Using **CH-▼** or **CH+▲** select the TV channel that you want to delete or whose order you want to change.
- 7 Confirm with **▶**.

Deleting TV channels

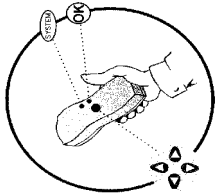
Unwanted channels or those with poor reception can be deleted using **CLEAR**. Proceed as step 6.

- 8 Using **CH-▼** or **CH+▲**, shift the TV channel to the desired position and press the **◀** button. The DVD recorder will insert the TV channel.
- 9 Repeat steps 6 to 8 until you have resorted/deleted all the TV channels you want.
- 10 To store, press **OK**.
- 11 To end, press **SYSTEM-MENU**.

Setting the language/country

You can select the country and, for DVD playback, the language for the subtitles and the audio language. Please note that, with some DVDs the audio language and/or subtitle language can be changed only via the DVD menu.

For bilingual shows you can also select the sound channel of the TV station for recording. You also have the option of setting one of the displayed languages for the on-screen menu (OSD). However, the DVD recorder display will only display English text regardless of this setting.



- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 4 Select **TV** symbol with **◀** or **▶**.
- 5 Select line **'Language'** with **CH-▼** or **CH+▲**, and confirm with the **▶** button.
- 6 Select the appropriate line and confirm with **▶**.

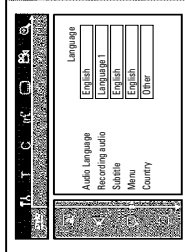
Which settings can I choose?

'Audio Language': Playback language (audio language)
'Recording audio': Type of audio recording **'Language 1'** or **'Language 2'**
'Subtitle': Subtitle language
'Menu': Language of the OSD menu
'Country': Location (country)



Tip

- 7 Select the appropriate setting using **CH-▼** or **CH+▲** and confirm with **OK**.
- 8 To end, press **SYSTEM-MENU**.



Switching over audio recording (2-channel sound)

Some TV programmes transmit an extra audio signal in stereo in addition to the normal audio signal (2-channel sound). In most cases this means that an additional language is available. If a TV programme is available in, say, English and German, German may be available as the second language.

To record TV programmes in stereo or 2-channel sound you can select Stereo or the language you want as the default setting. This setting does not become active until the sound of a TV programme is transmitted in 2-channel sound. When you play back the recording you can play back the sound only in the language you used for the recording.

5

On-screen information

You can check or change many of the functions and settings of your DVD recorder via the system menu bar. The menu bar cannot be displayed during recording.

Symbols in the menu bar

Press **SYSTEM-MENU** to open and close the menu bar (main menu). Use **◀** and **▶** to select the relevant function. Use **CH-▼** to confirm the function and go either to another menu or execute the function directly. Some functions may not be available, depending on the disc inserted.

Menu bar 1

	User preferences
	Title/track
	Chapter/index
	Audio language
	Subtitle language
	Camera angle
	Zoom

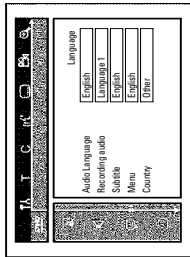
Menu bar 2

While menu bar 1 is being displayed you can go to menu bar 2 by pressing **▶** again.

	Sound
	Frame advance
	Slow motion
	Fast forward
	Search by time

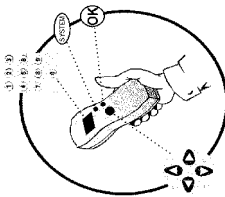
ENGLISH

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 4 Select **T** symbol with **◀** or **▶**.
- 5 Select line 'Language' with **CH-▼** or **CH+▲**, and confirm with the **▶** button.
- 6 Select line 'Recording audio' and confirm with **▶**.
- 7 Select 'Language 1' or 'Language 2' with **CH-▼** or **CH+▲** and confirm with **OK**.
- 8 To end, press **SYSTEM-MENU**.

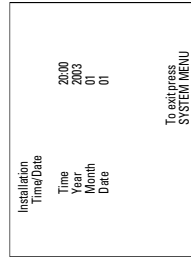


Setting the time and date

If the display shows an incorrect time or "–:–", the time and date must be reset manually. If a TV channel which transmits TXTPDC (teletext/PGC) is stored under programme number 'P01', the time and date will automatically be taken from the TXTPDC information.



- 1 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 2 Select **T** symbol with **◀** or **▶**.
- 3 Select 'Installation' using **CH-▼** or **CH+▲** and confirm with **▶**.
- 4 Select 'Time/Date' using **CH-▼** or **CH+▲** and confirm with **▶**.
- 5 Check if the time in 'Time' is correct. If required, change the time with the number buttons 0...9 on your remote control.
- 6 Check 'Year', 'Month' and 'Date' in the same way. To move between the fields, use **CH-▼** or **CH+▲**.
- 7 Check the displayed settings and confirm with **OK**. 'Stored' will appear briefly on the screen.
- 8 To end, press **SYSTEM-MENU**.



Field for temporary messages

The top left corner of the menu line contains a field for temporary messages relating to the various operating modes. This information appears briefly on the screen when certain disc functions have been activated.

	Shuffle
	Scan
	Repeat entire disc
	Repeat title
	Repeat track
	Repeat chapter
	Repeat from A to the end
	Repeat from A to B
	Camera angle
	Child lock enabled
	Resume playback
	Illegal action

Status field

The status field shows the current operating mode (status) of the DVD recorder and the type of disc inserted. This display can be disabled.

Disc type symbols

	DVD+RW
	DVD+R
	DVD-Video
	Video-CD
	No disc
	Error

Operating mode symbols

	Recording
	Stop
	Playback
	Playback-Pause
	Record-Pause
	Search forwards (8x speed)
	Search backwards (8x speed)
	Slow motion

Tuner information box

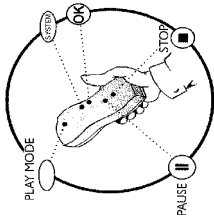
This field is located in the bottom left-hand corner of the screen. The aerial signal, the TV channel and the TV channel name for the selected programme are displayed.

	Current channel/selected input socket
	No signal The TV channel is not available/the additional device is not connected or it is switched off
	Copy-protected signal

Timer information box

This box appears above the tuner information box. When a timer recording is set, it shows the timer icon and the start time or date of the first programme to be recorded. If no timer recording is scheduled, the current time is displayed. This box disappears during playback of a disc or after a recording starts.

	Timer starts on the day shown
	OTR recording runs until the stop time displayed
	Current time No timer event programmed



General notes on playback

With this DVD recorder you can play back the following systems:

- DVD Video
- (Super)Video CD Disc
- DVD-RW Disc
- DVD-R Disc
- DVD-RW (video mode, finalised)
- DVD-R
- CD-R
- CD-RW
- Audio CD
- MP3 CD

You can operate the video recorder using the remote control or the buttons on the front of the DVD recorder.

ENGLISH

*** The display will read "!" ***

- ✓ The child lock has been activated for the inserted disc. Read the sections on 'Child lock' and 'Releasing a disc' in the chapter on 'Access control (child lock)'

*** The menu on the screen is showing an 'X' ***

- ✓ Some DVD discs can be manufactured so that certain steps are required before the disc can be played, or so that only limited operation is possible during playback. When an 'X' appears on the screen the selected feature is not possible.

*** The screen is showing regional code information ***

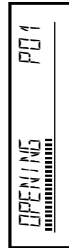
- ✓ Since DVD films are not normally released in all parts of the world at the same time, all DVD players have a specific regional code. Discs can be given a regional code. If the regional codes differ between the player and the disc, playback is not possible.
- ✓ The regional code is shown on the label on the back of the machine.
- ✓ The regional code does not apply to recordable DVD discs.



Problem

Inserting a disc

- 1 Press the **OPEN/CLOSE** button on the front. The disc tray will open. While the disc tray is opening, **OPENING** and then **TRAY OPEN** when the tray is fully open.
- 2 Carefully place the disc in the tray with the label facing up and, press **PLAY** or **OPEN/CLOSE**. **CLOSING** and then **TRAY OPEN** will appear in the display. The information on the disc will be read.



How do I insert a double-sided DVD?

Double-sided discs do not have labelling over the whole surface. The labelling for each side is in the centre of the disc. To play a side its label must be facing up.



Tip

Opening/closing the tray using the remote control
You can open and close the disc tray using the remote control. Press and hold the **STOP** button on the remote control until the dialog box shows **OPENING** or **CLOSING**.

3

Playback starts automatically.

A menu may appear when a DVD is played back. If the titles and chapters are numbered, press a number button on the remote control. You can also use the **CH+▲**, **CH-▼** buttons or number buttons **0-9** to select a menu item and confirm with **OK**. You can also access the menu using **DISC-MENU** on the remote control. For further information see 'Playing a DVD video disc'.



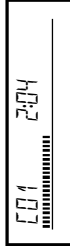
When a DVD-RW is played back the index overview appears. Using **CH+▼**, **CH+▲**, **◀◀**, **▶▶** select the title you want to play back. Confirm with **OK**. For further information see 'Playing back a DVD-RW/+R Disc'.

If playback does not start automatically, press **PLAY▶**. For further information see 'Playing an audio CD'.

If the **■** symbol appears in the display, start playback by pressing **PLAY▶**. If a menu appears on the screen, use the remote control buttons indicated on the screen to select the menu option you want (**PREV=◀◀**, **NEXT=▶▶**) or with the number buttons **0-9**. For further information see 'Playing a (Super) Video CD'.

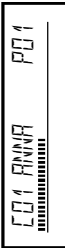
Playing a DVD video disc

- 1 If playback does not start automatically, press **PLAY▶**. This will appear on the display. title, chapter, elapsed time.
- 2 To stop playback, press **STOP■** on the remote control or **■** on the DVD recorder.
- 3 To eject the disc, press **OPEN/CLOSE▲** on the front of the DVD recorder.



Playing a DVD+RW/ +R disc

- 1 If the disc is write-protected or a finalised DVD+R disc, playback starts automatically.
- 2 If playback does not start automatically, use the **CH- ▾** or **CH+ ▲** button to select the title you want to play on the index screen.
You can also use the **⏮** or **⏭** button on the front.
- 3 Press the **PLAY ▶** button.
This will appear on the display:
title number, recording quality.



ENGLISH



Problem

*I can see the message "P01" or "P02".
✓ The disc does not contain any recordings.

- 4 To stop playback, press **STOP ■** on the remote control or **■** on the DVD recorder.
- 5 To eject the disc, press **OPEN/CLOSE ▲** on the front of the DVD recorder.



What should I note when playing back different recording types (qualities)?
The correct recording quality **M1, M2, M2x, M3, M4, M6** will automatically be selected during playback.
For more information see the section on 'Selecting the recording type (quality)' in the chapter on 'Manual recording'.

Playing an audio CD

You can also use the DVD recorder to play audio CDs

- 1 Insert an audio CD. Playback starts automatically.
- Audio CD display**
If the TV is on, the audio CD screen appears automatically.
During playback, the current track number and its elapsed playing time will show on the TV screen and on the recorder display.
- 2 Stop playback using **STOP ■**. The number of tracks and the total time are displayed.



Tip

Playing an MP3 CD

MP3 (MPEG I Audio Layer-3) files are highly compressed music files. Using this technology the data volume can be compressed by a factor of 10. This means it is possible to record 10 hours of music in CD quality on a single CD-ROM.

When creating MP3 CDs please note the following:

- File system: ISO%60
- Directory structure: maximum of 8 levels
- Format: *.mp3
- Filenames: maximum of 12 characters (8+3)
- Maximum of 32 albums, 999 titles
- Supported sampling frequencies: 32, 44.1, 48 (kHz). Music with sampling frequencies other than these will be skipped.
- Supported bit rates: 32, 64, 96, 128, 192, 256 (kbit/s)
- ID3 Tag: Version 1, 1.1. In later versions the directory name is displayed as the album and the filename as the title.

Important notes for playback:

Only the first session of a multi-session CD will play back.

- 1 Insert an MP3 CD. Playback starts automatically.

MP3 CD display

If the TV is on, the MP3 CD screen appears automatically.
During playback, the current track number and its elapsed playing time will show on the TV screen and on the recorder display.
During stopped playback (**STOP ■** button) the numbers of the albums will show on the TV screen and on the display.
Further information on the album, track and artist will also be displayed if included in the ID tag.



Tip

- 2 Stop playback using **STOP ■**. The number of albums is displayed in the display.

Additional playback features

You can also use the **TIC** button to select titles and albums.
1 Press the **TIC** button and use the **▶** or **◀** button to select the **T** symbol for title or **C** for chapter.
2 Use the **CH- ▾** or **CH+ ▲** buttons or the number buttons **0, 1, 9** on the remote control to select the number of the title/chapter.
You can also use the repeat functions (**PLAY MODE** button).



Tip






7

Additional playback features

Playing a (Super) Video CD

(Super) Video CDs may be equipped with PBC (Play Back Control). This means that special playback functions (menus) can be directly selected. The video CD must be PBC compatible (see CD case).

*PBC is active in the default settings.

- 1 Insert a (Super) Video CD.
If the  symbol appears in the display, start playback by pressing **PLAY** .
- 2 If a menu appears on the screen, use the remote control buttons indicated on the screen to select the menu option you want (PREV= , NEXT= ) or with the number buttons **0-9**.
If a PBC menu consists of a list of titles, you can select a title directly.
- 3 Use **RETURN** to go back to the previous menu.
- 4 Stop playback using **STOP** .

ENGLISH

Changing to another title/chapter

If there is more than one title or chapter on a disc you can change to another title or chapter as follows. However if there are several chapters within a title, these will be selected. The title can then still be selected via the menu bar.

- 1 During playback, press **▶▶** to go to the next title/chapter. Press **◀◀** to return to the start of the current title/chapter. Press **◀◀** twice to return to the start of the previous title/chapter.




Tip

Use the TIC (title/chapter) button

- 1 Press TIC (title/chapter) and then use **CH+▲** or **CH-▼** to select the appropriate title.
Make sure the symbol **T** (title) is selected in the menu bar.
- 2 Use TIC to select chapters within a title. Press TIC and use **▶** to select the **C** symbol (chapter).
Now select the appropriate chapter with **CH+▲** or **CH-▼**.

Searching a disc

You can search the disc for a recording at 4x, 8x or 32x playback speed. Other speeds can only be selected via the menu bar (**▶▶**).

- 1 During playback, press and hold **◀◀** (reverse) or **▶▶** (forwards) to switch to the search feature. You can switch between the playback speeds using **◀◀/▶▶**.
- 2 To continue playback, press **PLAY**  twice at your chosen location.




Problem

*No sound

✓ The sound is switched off in search mode. This is not a fault in your machine.

Search feature via menu bar

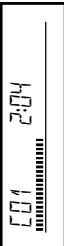
- 1 During playback press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
- 2 Select the **▶▶** symbol using **▶** or **◀** and confirm with **CH-▼**.
- 3 You can now use the **◀** or **▶** button to select different forward and backward search speeds.
- 4 If necessary, switch the menu bar off with the **SYSTEM-MENU** button.
- 5 To continue playback, press **PLAY**  twice.



Tip

Still picture

- 1 During playback, press **PAUSE II** to stop playback and display a still picture.



Frame advance via menu bar

- 1 During a still picture press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
- 2 Select the **[D]** symbol using **▶** or **◀** and confirm with **CH-▶**.
- 3 You can now use the **◀** or **▶** button to go forwards or backwards one frame at a time.
- 4 If necessary, switch the menu bar off with the **SYSTEM-MENU** button.

Tip

- 2 To continue playback, press **PLAY▶**.

Slow motion

- 1 During playback press **PAUSE II** on the remote control. Now hold down **◀◀** or **▶▶** to switch to slow motion.
- 2 You can switch between different speeds using **◀◀** or **▶▶**.

Slow motion via menu bar

- 1 During playback, press **PAUSE II** and then **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
- 2 Select the **[D]** symbol using **▶** or **◀** and confirm with **CH-▶**.
- 3 You can now use the **◀** or **▶** button to select different forward and backward slow motion speeds.
- 4 If necessary, switch the menu bar off with the **SYSTEM-MENU** button.

Tip

- 3 To continue playback, press **PLAY▶** twice.

Search by time

Using this feature you can select where playback should start (select elapsed time).

- 1 During playback press **SYSTEM-MENU** on the remote control. The menu bar will appear at the top of the screen.
- 2 Select the **[D]** symbol using **▶** or **◀** and confirm with **CH-▶**. Playback is stopped and a box appears on the screen showing the elapsed time.

- 3 Enter the start time with the digit keys **0-9** from where playback should start.
- 4 Confirm with **OK**.



* The time entered will flash on the screen
 ✓ The selected title is shorter than the time entered. Enter a new time or cancel the function by pressing **SYSTEM-MENU**.

Problem

- 5 Playback starts at the time you entered.

Repeat/Shuffle play

You can mark entire sections or the whole disc for endless playback. Depending on the type of disc (DVD video, DVD+RW, video CD) you can select a chapter, title or the entire disc.

- 1 Select the desired chapter, title or the entire disc and start playback.
- 2 During playback, press **PLAY MODE**. By pressing **PLAY MODE** again you can choose from the following options:
 - ▶ **[REPEAT]**: repeat chapter (DVD only)
 - ▶ **[TITLE]**: repeat track/title
 - ▶ **[DISC]**: repeat entire disc (Video CD, Audio CD only)
 - ▶ **[SHUFFLE]**: Shuffle
 - ▶ Display disappears: no repeat
- 3 To end the repeat, press the **STOP ■** button. You can also keep pressing the **PLAY MODE** button until the displays disappear.

Repeating a passage (A-B)

You can repeat a particular passage within a title/chapter. You need to indicate the start and end of the passage.

- 1 During playback press **PAUSE II** at the start point. You will see a still picture.
- 2 Keep pressing **PLAY MODE** until **[A-B]** appears on the screen. The start point is now saved. Press **PLAY▶** to start playback.
- 3 When the end point is reached press **OK**. **[A-B]** appears on the TV screen. Playback now takes place within these points.
- 4 To end the repeat, press the **STOP ■** button. You can also keep pressing the **PLAY MODE** button until the displays disappear.

- 6 Confirm with **OK**.
- 7 To stop the feature, press **PLAY▶** and then **SYSTEM-MENU**.


Select the audio language

Many pre-recorded DVD discs have more than one audio language. The language initially selected for playback will be the one you selected when you first set up the DVD recorder. However you can change the audio language of the inserted disc at any time. You can change the audio language either using the menu of the inserted disc (**DISC-MENU** button) or the **AUDIO** button. The audio languages for DVD playback in the two menus may be different. Please note that with some DVDs the audio language and/or subtitle language can be changed only via the DVD menu.

- 1 During playback press **AUDIO**.
- 2 Select the required audio language using **CH-▼** or **CH+▲**. You can also enter the number directly using the number buttons **0-9**.
- 3 Play continues in the new audio language.


Subtitles

Many pre-recorded DVD discs have more than one subtitle language. The language initially selected for playback will be the one you selected when you first set up the DVD recorder. However you can change the subtitle language of the inserted disc at any time. You can change the subtitle language either using the menu of the inserted disc (**DISC-MENU** button) or the menu bar (**SYSTEM-MENU** button). The subtitle languages in the menus may differ.

- 1 During playback, press **SYSTEM-MENU** and select the  icon using **▶**.
- 2 Select the required subtitle language using **CH-▼** or **CH+▲**. You can also enter the number directly using the number buttons **0-9**. You can switch off subtitles again with **0** or by pressing **off**.
- 3 Playback continues in the new subtitle language.

Scan feature


This feature plays back the first 10 seconds of each chapter (DVD) or track (CD).



- 1 During playback, press **PLAY MODE**. Select  using **PLAY MODE**.
- 2 After 10 seconds the DVD recorder switches to the next chapter/index. To start playback at the relevant chapter/index, press **STOP■** and then **PLAY▶**.

Camera angle

If a DVD contains scenes that have been shot from different camera angles you can select these camera angles for playback.




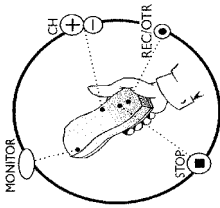
Problem
 *The  symbol will be hidden
 ✓ The selected scene has been shot from only one camera angle. This feature is therefore not available. For more information please read the cover of your DVD disc.

- 1 During playback, press **PAUSE II**. You will see a still picture.
- 2 Press **SYSTEM-MENU** and select the  icon using **▶**.
- 3 Select the required camera angle with **CH-▼** or **CH+▲**. You can also directly enter the number with the number buttons **0-9**.
- 4 After a short time, playback will resume from the new camera angle. The  symbol will remain visible until a scene starts for which there is only one camera angle.

Zoom feature

The Zoom feature allows you to enlarge the video image and pan through the enlarged image.

- 1 During playback, press **PAUSE II**. The DVD recorder switches to 'PAUSE'. You will see a still picture.
- 2 Press **SYSTEM-MENU** and select the  icon using **▶**.
- 3 Select the required zoom factor using **CH-▼** or **CH+▲**.
- 4 When 'press **OK to pari**' appears on the screen, the zoom process is complete.
- 5 Press **OK**. Using **CH+▲**, **CH-▼**, **▶**, **◀** select the part of the image you wish to view.



General

Which discs can I use for recording?

With this DVD recorder, you can record on two types of DVD:
DVD+RW
 This disc can be written to and then the contents deleted.

DVD+R

This type of disc can only be recorded once.
 If you want to play this DVD in a DVD player, it must be finalized using the 'Finalise disc' function. It is not possible to make further recordings using this disc.
 If this disc is to be played in a DVD recorder, it must not be finalised. Recordings can be added and deleted. The disc space (playback time) from the deleted recording cannot be recovered for further recordings.

Use the 'Manual recording' function to spontaneously start recording (e.g. to record a TV show already in progress).

In the index display select the title to be overwritten or 'Empty title' with **CH-▼**, **CH+▲**. If you insert recordings between existing recordings, check the lengths of the old and new recordings. If the new recording is too long the subsequent recording (title/chapter) will be overwritten.

ENGLISH



Insert new recordings at the end of all existing recordings (Safe Record)

To add a new recording at the end of the last recording on the disc, hold down the **REC/OTR** button until the message 'SAFE REC.' appears on the display.

For DVD+R discs each new recording is always added at the end of all previous recordings as existing recordings cannot be overwritten.

End of disc is reached

If the end of a disc is reached during recording, recording will stop and the Recorder will turn itself off automatically.



Tip

Please refer to section 'Recording without automatic switch-off', if you want to manually start and stop your own recording.

If you want to start a recording manually but have it stopped automatically, read the section 'Recording with automatic switch-off' (e.g. not to record to the end of the disc)

Read the section 'Automatic recording from a satellite receiver', if you want a recording to be controlled automatically by a satellite receiver.

Read the section 'Direct record' if you want to record a programme currently being shown.

Recording without automatic switch-off

1 Switch on the TV set and select the programme number for the DVD recorder.

2 Insert a disc on which the recording is to be made. This disc is then checked for content and system. **REC/OTR** will appear on the display.

* Index display

✓ A DVD+RW disc has been inserted that already contains recordings. Use the **CH+▲** or **CH-▼** button to select the point where the recording is to start.

x The message 'EMPTY DISC' appears in the display

✓ The disc inserted is a blank DVD disc.

* A dialog box appears asking you whether you want to delete the contents or eject the disc

✓ The disc inserted is a DVD+RW but its contents are not DVD video-compatible (e.g. a data disc). Recordings on this disc can only be made if the entire disc is first deleted with the **REC/OTR** button.

x The message 'Title limit' appears on the screen if a recording is to be made

✓ A disc may contain a maximum of 48 titles (including blank titles). Delete titles or change the disc.



Problem

3 If necessary, use the **MONITOR** button on the remote control to switch to the internal tuner in the DVD recorder.

4 Use **CH+▲** or **CH-▼** to select the programme number (station name) you want to record. This will appear on the display.



Programme numbers of the external inputs:

'EXT 1' Start socket at the back EXT 1 TO TV-I/O

'EXT 2' Start socket at the back EXT 2 AUX-I/O

'FM1' Front S-VIDEO sockets S-VIDEO / left AUDIO right

'FM2' Front video/audio sockets AV S-VIDEO / left AUDIO right

Switching between the S-VIDEO and VIDEO sockets takes place automatically. If both sockets are in use, the signal at the S-VIDEO socket has priority.

'FM3' Digital Video (Link) front socket DV IN

'FM4'

'FM5'

'FM6'

'FM7'

'FM8'

'FM9'

'FM10'

'FM11'

'FM12'

'FM13'

'FM14'

'FM15'

'FM16'

'FM17'

'FM18'

'FM19'

'FM20'

'FM21'

'FM22'

'FM23'

'FM24'

'FM25'

'FM26'

'FM27'

'FM28'

'FM29'

'FM30'

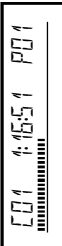


Tip

5 To start recording, press **REC/OTR** on the remote control or **RECORD** on the DVD recorder.

If you want to start the recording at the end of the existing recordings, hold down the **REC/OTR** button until the message 'SAFE REC.' appears on the display.

For DVD+R discs each new recording is always added at the end of all previous recordings as existing recordings cannot be overwritten. This will, for example, appear in the display.



Insert chapter markers
 During recording you can mark scenes so you can find them or hide them later.
 During recording, press **FSS** \times at the start point. 'Inserting marker' appears on the TV screen. In the display, the number of the 'CHAPTER' increases by one.
 For further information on titles and chapters, see the section on 'Changing to another title/chapter' in 'Playback'.

Tip

Use the **STOP** button on the remote control or **■** on the machine to stop the recording. 'RECORDING' will appear on the display. The DVD recorder is writing the list of contents. Wait until the message disappears from the display. The recording is then complete.

6

***The display will read 'DISC ERROR'**
 ✓ Recording could not be completed correctly because of a disc error. Check the disc and clean it, if necessary.

Problem

Making recordings on DVD-R discs compatible
 If you want to play back the recording on a DVD player, you need to finalise the disc in the DVD recorder. You can prepare your DVD for use in a DVD player using the 'Finalising' feature. See 'Finalising DVD-R discs' in 'Managing the disc contents'.

Tip

Interrupt recording (Pause)

- 1 During recording, press **PAUSE** , for example to avoid recording the commercials.
- 2 To continue recording, press **REC/OVR** .

End recording
 To end the recording, press the **STOP** button. 'RECORDING' disappears from the display.

Tip

ENGLISH

Recording with automatic switch-off (OTR one-touch-recording)

- 1 Insert a disc.
- 2 If necessary, use the **MONITOR** button on the remote control to switch to the internal tuner in the DVD recorder.
- 3 Use **CH+▲** or **CH-▼** to select the programme number (channel name) you want to record.
- 4 Press **REC/OVR** on the remote control.
- 5 Each time you press **REC/OVR** you will add 30 minutes to the recording time.



How can I cancel the recording time I have just entered?
 To delete an entry, press **CLEAR** while the display shows the recording time.

Preventing accidental erasing of discs

To ensure you don't accidentally delete a recording you can protect the entire disc. You can only ever protect the entire disc. You cannot protect individual recordings.



What happens with DVD-R discs?
 As long as these discs are not finalised, they can be protected against accidental erasure in the same way as DVD+RW discs.

- 1 Insert the disc to be protected.
- 2 While the index screen is displayed, press **STOP** on the remote control. The first title is highlighted.
- 3 Press **CH+▲**. This takes you to the disc info screen.
- 4 Press the **▶** button. Select the 'Protection' line. Confirm with **▶**.
- 5 Select 'Protected' with the **CH-▼** button and confirm with **OK**.
- 6 Press **◀** and then **DISC-MENU** to terminate.

Selecting the recording type (Quality)

You can select the picture quality of the recording using the recording quality feature and hence the maximum recording time per disc. You can check the quality by changing the recording mode and then watching the picture from the built-in tuner (MONITOR button). During playback, the correct picture quality will automatically be selected.

- Switch on the TV set. If required, select the programme number for the DVD recorder.
- Select the record mode with the button **REC MODE** on the remote control.

Which recording types can I choose?

- 'M1': High Quality offers the best picture quality and a recording time of 1 hour.
- 'M2': Standard Play (pre-recorded DVD quality) offers standard picture quality and a recording time of 2 hours.
- 'M2X': Standard Play plus (better than S-VHS quality) offers standard picture quality and a recording time of 2.5 hours.
- 'M3': Long Play (S-VHS picture quality). Recording time of 3 hours.
- 'M4': Extended Play (better than VHS picture quality). Recording time of 4 hours.
- 'M6': Super Long Play (VHS picture quality). Recording time of 6 hours.

Can I select the recording type via a menu as well?

- Press the **SYSTEM-MENU** button.
- Select **▶** symbol with **◀** or **▶**.
- Select **'Record settings'** using **CH** or **CH+▲** and confirm with **▶**.
- In the line **'Record mode'** select the recording type with **◀** or **▶**.
- Confirm using **OK** and **SYSTEM-MENU**.
- If you have selected the recording mode **M3**, **M4** or **M6**, you can select the settings **'Stand'** (Standard) or **'Sport'** (for rapid movements) in the **'Filter mode'** line.



Tip

The entire disc is now protected. If an attempt is made to record on a protected disc, **DISC LOCK** will appear on the display and **'Disc locked'** will appear on the screen.

Lining up recordings within a title (assemble cut)

On a recorded DVD+RW disc you can add another recording to an existing title. This recording is added to the title as a 'chapter'. The existing information will be overwritten starting from this point. Titles will also be overwritten that follow the current title depending on the length of the new recording. The recording type (Quality) will be taken from the current title. To play back this recording, press **SYSTEM-MENU** and use the **▶** button to select the 'C' (Chapter) symbol. You can also use the **TIC** key.

For further information, see 'Changing to another title/chapter' in 'Playback'.



What happens with DVD+R discs?

New recordings on 'DVD+R' discs can only be added after existing recordings. It is not possible to overwrite existing recordings on 'DVD+R' discs.

- In the index display, find the title to which the new recording is to be added.
- Look at the last minute of the old recording (playback)
- Press **PAUSE||** on the remote control at the position where the new recording is to go. **'||'** will appear on the screen.
- To monitor the recording you can press **MONITOR** to switch to the internal tuner.
- Now start recording as usual by pressing **REC/OTR** on the remote control. The new recording will be inserted.
- Stop recording with **STOP**.

Automatic recording from a satellite receiver (Sat recording)

You can use this function if you own a satellite receiver that can control other devices via a start cable and a programming function (timer). For more information, please see the operating instructions for the satellite receiver.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 3 Select **T_H** symbol with **◀** or **▶**.
- 4 Select **'Record settings'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 5 Select **'Sat record'** using **CH-▼** or **CH+▲**.
- 6 Select **'EXT2'** with **◀** or **▶**.



Tip

Switching off 'Sat Recording'
To switch off the function, select **Off** using **▶** or **◀**.

- 7 Confirm with **OK**.
- 8 Use a start cable to connect start socket **EXT 2 AUX-IO** on the DVD recorder to the corresponding start socket on the satellite receiver.
- 9 To end, press **SYSTEM-MENU**.
- 10 Insert a disc you want to use for recording.
- 11 Programme the satellite receiver with the required information (programme number of the TV channel, start time, end time). If necessary, please see the operating instructions for your satellite receiver.
- 12 Switch off the DVD recorder using **STANDBY** **⏻**. 'SAT' also appears in the display to indicate that the function is active.

The DVD recorder is now ready to record. The start and end of the recording is controlled via start cable **EXT 2 AUX-IO**.

Direct Record

Can you record the right TV channel in seconds when the DVD recorder is switched off? No problem. If recording is started manually, the **switched-off** DVD recorder takes the current TV channel from the TV set via the start cable. You will find more information on how to switch 'Direct record' on or off in the next section 'Direct record'.

How does Direct Record work?

The DVD recorder compares the TV channel selected on the TV set with its stored TV channels via the start cable. If the same TV channel is found, it switches the DVD recorder to the corresponding programme number and starts recording.

Please do not change channel on the TV during the search. This could affect the tuning of the DVD recorder.



- 1 On the TV set, select the programme number you want make the recording from.
- 2 Press **REC/OTR** with the DVD recorder **switched off**.

* The display will read 'WRT' *

✓ The DVD recorder is comparing its saved TV channels with those of the TV set. Please do not change the TV channel on the TV set while 'WRT' is shown in the display.

* 'WRT' appears in the display

✓ This TV channel could not be found in the DVD recorder's memory. Check that all TV channels saved on the TV set are available on the DVD recorder. If required, save any missing channels. Please read 'Manual TV channel search' in 'Installing your DVD recorder'.

✓ Check the connectors at both ends of the start cable.

✓ Check your TV's operating instructions to see which start socket is used for video signals.

✓ If the problem persists, you won't be able to use this feature.

Problem

- 3 Stop recording with **STOP**.

9

Managing the disc contents

Switching 'Direct Record' on or off

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 3 Select **TR** symbol with **◀** or **▶**.
- 4 Select **'Record settings'** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 5 Select **'Direct Record'** using **CH-▼** or **CH+▲**.
- 6 Select **'On'** (Direct Record on) or **'Off'** (Direct Record off) using **◀** or **▶**.
- 7 Confirm with **OK**.
- 8 To end, press **SYSTEM-MENU**.
- 9 Switch off with **STANDBY** **⏻**.

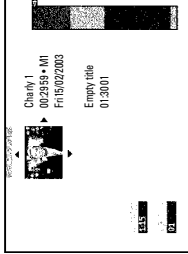
ENGLISH

General

When a recording is made to disc, the following additional information is also stored at the beginning of the recording:

- ▶ Name of the recording
- ▶ If the TV station does not transmit a name, only the channel number and time will be stored as the name
- ▶ Length of the recording
- ▶ Record type (Quality)
- ▶ Date of the recording
- ▶ Index picture of the recording

A marker will be set every 5-6 minutes if the **'Auto chapters'** function is activated in the **'Record settings'** menu. This marker is known as a 'chapter'. These markers can be changed when the recording has finished.



Can markers be set on a DVD-R disc?

Markers can be set on these discs if they have not been finalised.

It is also possible to add 'chapters' later. This means that scenes you do not want to see during playback, such as commercials, can be hidden or skipped. During playback you can watch your recording as a continuous sequence without the hidden chapters.

Select from the following chapters:

'Favorite Scene Selection', to divide the title into chapters or to manage the chapters.

'Editing recording titles (name)', to change the recording names.

'Play complete title', to play the entire title including the hidden chapters.

'Delete recording/title' to delete the relevant title and therefore also the recording.

'Disc settings' to change the general settings of the disc.

Favorite Scene Selection

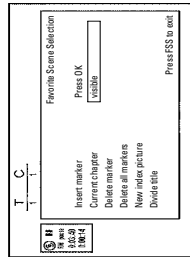
In this menu you can adapt a title to suit your particular needs. You can insert/delete chapter markers, hide chapters, select a new index, or split up a title. Press **FSS** on the remote control during recording to open this menu.

ENGLISH

Insert chapter markers

During recording, you can set or delete chapter markers within a title. The maximum number of chapters per disc is 124 and 99 per title. If one of these limits is reached the following message will appear on the screen: **Chapter limit**. You need to delete some markers before you can insert new ones or make recordings.

- 1 During playback, press **FSS** on the remote control at the appropriate point. The **'Favorite Scene Selection'** menu appears on the TV screen.



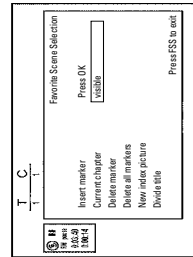
Tip

'X' will appear on the screen: This DVD is write-protected or the disc is a finalised DVD-R. Subsequent changes cannot be made.

- 3 To stop this function, press **FSS**.

Hiding chapters

Initially, all the chapters are visible. You can hide chapters for playback (e.g. advertisements) or make them visible again. In editing mode, hidden chapters are shown as dimmed.



Tip

How can I select different chapters?

- 1 Press the **T/C** button on the remote control. Titles and chapters are displayed at the top of the screen.
- 2 Select title (T) or chapter (C) with **▶** or **◀**.
- 3 Use **CH+▲** or **CH-▼** to select the title/chapter channel you want to edit.

- 2 Select **Current chapter** using **CH-▼**.

- 3 Using **▶** select **'hidden'**. The picture is shown darker.



Tip

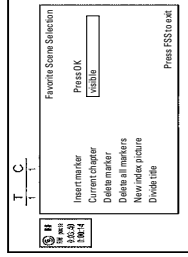
Switching quickly
You can switch between show chapters (**Visible**) and hide chapters (**hidden**) quickly and easily using **SELECT**.

- 4 To end, press **FSS**.

During playback this chapter will be skipped. If the chapter is not visible, select **'Visible'** in step 3 with **▶**.

Deleting chapter markers

Within a title you can delete either all markers or individual markers.



Tip

How can I select different chapters?

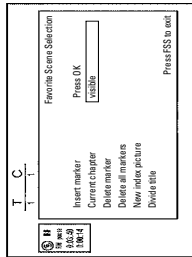
- 1 Press the **T/C** button on the remote control. Titles and chapters are displayed at the top of the screen.
- 2 Select title (T) or chapter (C) with **▶** or **◀**.
- 3 Use **CH+▲** or **CH-▼** to select the title/chapter channel you want to edit.

- 2 Use **CH-▼** to select either **'Delete marker'** for this chapter or **'Delete all markers'** for all chapters within the selected title.
- 3 Confirm with **OK**.
- 4 To end, press **FSS**.

Changing the index picture

Normally the first picture of a recording is used as the index picture. You can however choose any picture from the recording as the index picture.

- 1 During playback, search for location of the new index picture. Press the **PAUSE II** button.
- 2 Press the **FSS** <> button. The **'Favorite Scene Selection'** menu appears on the TV screen.
- 3 Select line **'New index picture'** and confirm with **OK**.
- 4 Start the change with **OK**. **'Updating menu'** appears on the TV screen.



Once the revision has been completed successfully the DVD recorder reverts to the index overview.

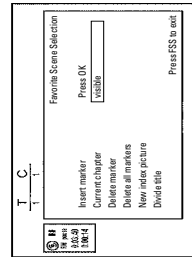
Splitting titles

You can split a title into several sections (titles) of any size. Each of these sections (titles) is identified by its own index.

Note: This split cannot be undone.

Can I split titles on DVD+R discs?
As recordings on DVD+R discs cannot be overwritten, it is not possible to split titles.

- 1 While the relevant title is playing, press **FSS** <> on the remote control. The **'Favorite Scene Selection'** menu appears on the TV screen.
- 2 Select **'Divide title'** and confirm with the **OK** button.
- 3 If you are sure, press **OK** to start the process. **'Dividing title'** appears on the TV screen.
- 4 Wait until the new title is displayed with an index picture in the index picture overview.

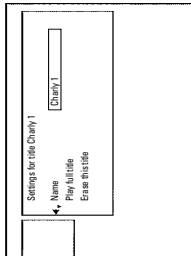


The process of splitting the title is now complete.

Editing recording titles (name)

Some TV stations transmit the title (name) of a programme. In this case, the name will be included automatically (eg. 'ROCKY'). Otherwise, the only the programme number (programme name) and the time are stored as the name of the recording. The name of the recording can only be changed after the recording has been completed.

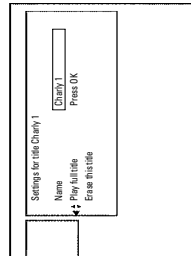
- 1 Press the **STOP** button or during playback press **DISC-MENU**.
- 2 Using **CH+▲** or **CH-▼** select the title whose name you want to edit and confirm with **▶**. The menu for editing names appears.
- 3 Select **'Name'** using **CH+▲** or **CH-▼** and confirm with **▶**.
- 4 Using **▶** or **◀** select the position where the letter/number/icon is to be changed/re-entered.
- 5 Change the icon using **CH+▲** or **CH-▼**. You can switch between upper and lowercase using **SELECT**. You can delete the character using **CLEAR**.
- 6 Repeat 4 and 5 until you have made the changes you want.
- 7 Save the new name with **OK**. **'Storing name'** appears on the TV screen for confirmation.
- 8 To end, press **◀**.



Playing the entire title

If you have hidden certain sections (chapters) of a title, this setting lets you watch the entire title including the hidden sections. To do this, proceed as follows:

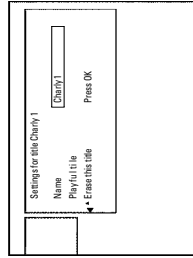
- 1 Press the **STOP** button or during playback press **DISC-MENU**.
- 2 Using **CH+▲** or **CH-▼** select the title you want to play all of and confirm with **▶**. The title editing menu will appear.
- 3 Select **'Play full title'** using **CH+▲** or **CH-▼** and confirm with **OK**.
- 4 Playback starts automatically. The title is played in its entirety - including the hidden chapters.



Deleting recordings/titles

You can delete specific recordings from a disc. To do this, proceed as follows:

- 1 Press the **STOP** button or during playback press **DISC-MENU**.
- 2 Using **CH+▲** or **CH-▼** select the title you want to delete and confirm with **▶**. The title editing menu will appear.
- 3 Select **Erase this title** using **CH+▲** or **CH-▼** and confirm with **OK**. **This will completely erase this title** appears on the TV screen.. **Press OK to confirm**.
- 4 If you want to delete this title, press **OK** to confirm. Otherwise press **◀**.
- 5 **'Erasing title'** appears on the TV screen.
- 6 At this point **'Empty title'** appears in the 'index picture display'. A new recording can now be made here. If the deleted title was very short (less than 1 minute) **'Empty title'** will not appear at this point.



Can titles be deleted from a DVD+R disc?

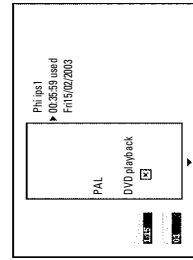
Titles on DVD+R discs are only marked as deleted. **Deleted title** will appear in the display instead of **'Empty title'**. During playback the 'deleted' title is skipped. The space used for this title cannot be used again as the title has not been physically deleted. Once the disc has been finalised no further changes can be made.

Disc settings

This screen appears before the first title and contains general information about the current disc.

You can:

- change the name of the disc
- activate or deactivate write protection on the disc
- Finish editing (make the disc DVD compatible)
- finalise a DVD+R
- delete a DVD+RW

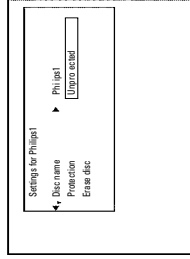


To get to this display, proceed as follows:

- 1 Press the **STOP** button or during playback press **DISC-MENU**.
- 2 Select the first title with **CH+▲** or press **STOP**.
- 3 Press the **CH+▲** button. The disc info display will appear.

Changing the disc name

- 1 In the 'Disc info display' press **▶**. The **'Settings for'** menu appears on the TV screen.
- 2 Select **'Disc name'** using **CH+▲** or **CH-▼** and confirm with **▶**.
- 3 Using **▶** or **◀** select the position where the letter/number/icon is to be changed/re-entered.
- 4 Change the icon using **CH+▲** or **CH-▼**. You can switch between upper and lowercase using **SELECT**. You can delete the character using **CLEAR**.
- 5 Repeat **3** and **4** until you have made the changes you want.
- 6 Save the new title with **OK**. **'Storing name'** appears on the TV screen for confirmation.
- 7 To end, press **◀**.



Finishing editing

If one or more titles have been edited a DVD player may still display the original titles. You can prepare your disc in such a way that a DVD player will be able to play the edited version.

- 1 In the 'Disc info display' press **▶**. The **'Settings for'** menu appears on the TV screen.
- 2 Select **'Make edits compatible'** using **CH+▲** or **CH-▼** and confirm with **OK**.



'Make edits compatible' does not appear

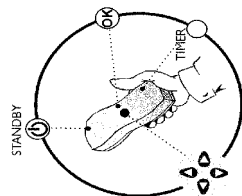
✓ Your disc is already compatible. There is no need for conversion. To end, press **SYSTEM-MENU**.

Problem

The screen displays **'This will take'** to show how long the process will last.

- 3 To confirm press **OK**. **'Working'** appears on the TV screen. A bar will move from left to right indicating progress.

10 Programming a recording (TIMER)



General

Use Programming a recording (TIMER)¹, to automatically start and stop a recording at a later date.

The DVD recorder will switch to the right programme number and begin recording at the correct time.

With this DVD recorder, you can pre-programme up to six recordings within a period of one month.

To make a programmed recording, your DVD recorder needs to know:

- * the date you want to make the recording
- * the programme number of the TV channel
- * the start and stop time of the recording
- * VPS or PDC on or off
- * the recording mode (M1/M2/M3/M4/M6)

This information is saved in a 'TIMER block'.

What is VPS/PDC?

VPS (Video Programming System)/PDC (Programme Delivery Control) are used to control the start and duration of TV channel recordings. If a TV programme starts earlier or ends later than was scheduled, the DVD recorder will then turn on and off at the correct time.

What do I need to know about VPS/PDC?

- * Usually the start time is the same as the VPS or PDC time. If a different VPS/PDC time is indicated, eg.: 20.15 (VPS/PDC 20.14), the VPS/PDC time 20.14* must be entered exactly to the minute during programming. If you want to programme a time that is different from the VPS or PDC time, you must switch off VPS or PDC.

- * Only one TV program of a TV channel can be controlled using VPS/PDC at a time. If you want to record two or more TV programmes on a TV channel using VPS/PDC, you will need to programme these as two separate recordings.

- * Since the DVD recorder requires a certain lead time (for getting the disc up to speed and positioning the laser) before recording can start, it is possible that the recorder will miss the first few seconds of a TV show recorded with VPS/PDC. In this case, disable VPS/PDC and enter a start time one minute earlier.



Finalising DVD+R discs

This feature is required to play back a DVD+R disc in a DVD player. Once the disc has been finalised no further recordings or changes can be made.

- 1 In the 'Disc info display' press ►. The 'Settings for' menu appears on the TV screen.
- 2 Select 'Finalise disc' using CH+▲ or CH-▼ and confirm with OK.

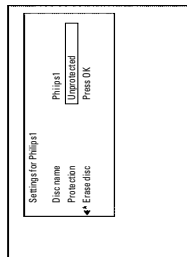
* 'Finalise disc' does not appear.
 ✓ Either there is no DVD+R disc inserted or the disc is already finalised.
 To end, press SYSTEM-MENU.

* The 'Settings for' menu does not appear.
 ✓ The menu may not appear if the disc has been recorded on another DVD recorder. In this case, use the 'Finalise disc' feature in the 'Ti' menu, under 'Features'.

- 3 The screen displays 'This will take...' to show how long the process will take.
- 4 To confirm press OK. 'Working' appears on the TV screen. A bar will move from left to right indicating progress.

Delete DVD+RW disks

- 1 In the 'Disc info display' press ►. The 'Settings for' menu appears on the TV screen.
- 2 Select 'Erase disc' using CH+▲ or CH-▼ and confirm with OK. 'This will erase all titles' appears on the TV screen. Press OK to confirm.
- 3 If you want to delete all the titles, press OK to confirm. Otherwise press ◀.
- 4 'Erasing disc' appears on the TV screen.
- 5 After deletion, the index picture display shows the free space on the disc.



ENGLISH



Problem

Programming recordings with the ShowView® System

SHOWVIEW®

Thanks to this programming system, you no longer need to tediously enter the date, programme number, start and end times. All the information needed by the DVD recorder for programming is contained in the ShowView® programming number. This 9-digit ShowView® number is found in most TV listings magazine.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **TIMER** on the remote control. The programming method selected last is marked.
- 3 Select **ShowView system** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 4 Enter the entire ShowView number. This number is up to 9 digits long and can be found next to the start time of the TV programme in your TV listings magazine.
e.g.: 53124 or 53124
Enter 53124 for the ShowView-number.
If you make a mistake, you can clear your instructions with **CLEAR**.

Timer ShowView system	Rec Mode M2
ShowView number	To store Press OK
Mo-Fr/Weekly Press SELECT	

Selecting daily/weekly recordings

Using **SELECT**, select from the following options:
Mo-Fr: Repeated daily recordings (Monday to Friday)
Weekly: Repeated weekly recordings (every week on the same day)

- 5 Confirm with **OK**.

x The following message appears on the screen: 'Please enter programme number'

✓ The programme number of the TV channel has not yet been assigned to the ShowView number. Use **▶**, **◀** or the number buttons **0-9** on the remote control to select the appropriate programme number (name) of the TV channel and confirm with **OK**.

x The following message appears on the screen: 'ShowView number wrong'

✓ The entered ShowView number is incorrect. Correct your entry or cancel using the **SYSTEM-MENU** button.
✓ Check the timetable (see 'Setting the time & date' in 'Installing your DVD recorder').

x The following message appears on the screen: 'Weekend programming not possible'

✓ A daily recording was entered for the wrong day. Daily programming can only be used for recordings to be made from Monday to Friday.

Problem

Timer ShowView system	VPS Start PDC End 21:30 Date BBC1 20:15	Rec Mode M2
Mo-Fr/Weekly Press SELECT		To store Press OK

6 The decoded data appears after confirmation. You can go back and change the data. Select the appropriate input field with **▶** or **◀**. If required, make changes using **CH+▲**, **CH-▼** or the number buttons **0-9**.

'Switching on VPS/PDC' in the 'Start' input field

Select the **'Start'** input field using **▶**. Using **SELECT** switch on VPS/PDC (* lights up). If you press **SELECT** again, you will switch VPS/PDC off (* goes out).

Changing the recording mode in input field 'End'

Select the **'End'** input field using **▶**.
Use **SELECT** to select the recording mode **M1, M2, M2x, M3, M4, M6**.

Tip

7 If all information is correct, press the **OK** button. The programming information is stored in a **TIMER** block.

8 To end, press **TIMER**.

9 Insert a recordable disc (one without write protection). The disk you have inserted will be checked.

10 Switch the DVD recorder off with **STANDBY**.

The programmed recording will only function properly if the DVD recorder has been **switched off** using the **STANDBY** button.

If any of the **TIMER** blocks are in use, **TIMER** will light up on the recorder display.



Tip

Programming recordings without the ShowView® System

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **TIMER** on the remote control. The programming method selected last is marked.
- 3 Select line **'Timer programming'** with **CH+ ▸** or **CH- ▾** . and confirm with the **▸** button. The information will appear on the screen.
- 4 Select the input field with **◀** or **▶** .
- 5 Enter information with **CH- ▾** or **CH+ ▸** or with the number buttons **0..9** .

Timer programming	VPS	Rec
Date	Prog. Start PDC	End
01	BBCT 2015	21:30
		M1

To store Press OK

Selecting daily/weekly recordings
 In **'Date'** use **SELECT** to select from the following options:
Mo-Fr: Repeated daily recordings from Monday to Friday
Mo-Fr: Repeated weekly recordings (every week on the same day, e.g. Monday).

Programme numbers of the 'EXT1' and 'EXT2' start socket
 You can also programme recordings from external sources via start socket **EXT 1 TO TV-IO (EXT1)** or **EXT 2 AUX-IO (EXT2)**.

'Switching on 'VPS/PDC' in the 'Start' input field
 Select the **'Start'** input field using **TIMER** . Using **SELECT** switch on **VPS/PDC** (* lights up). If you press **SELECT** again, you will switch **VPS/PDC** off (* goes out).

Changing the recording quality in input field 'End'
 Select the **'End'** input field using **▶** .
 Use **SELECT** to select the recording mode.

- 6 If all information is correct, press the **OK** button. The programming information is stored in a **TIMER** block.
- 7 To end, press **TIMER** .
- 8 Insert a DVD (one without write protection).
The disk you have inserted will be checked.
- 9 Switch off with **STANDBY** ⏻ .
The programmed recording will only function properly if the DVD recorder has been **switched off** using the **STANDBY** ⏻ button.

If any of the **TIMER** blocks are in use, **TIMER** will light up on the recorder display.

How to change or delete a programmed recording (TIMER)

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **TIMER** on the remote control. The programming mode selected last is marked.
- 3 Select **'Timer List'** using **CH- ▾** or **CH+ ▸** and confirm with **▶** .
- 4 Select the programmed recording (**TIMER**) you want to check, change or delete with **CH- ▾** or **CH+ ▸** .

Timer List	VPS	Rec
Date	Prog. Start PDC	End
01	BBCT 2015	21:30
		M2

Total record time: 01:15
 To change Press ▶
 To exit Press TIMER

Delete programmed recording
 1 Press the **CLEAR** button.
 2 Confirm with **OK** . **'Timer Cleared'** will briefly appear on the TV screen.
 3 To end, press **TIMER** .
 *... appears rather than the displayed values



Tip

- 5 Press **▶** .
Select the input field with **◀** or **▶** .
If required, change the information with **CH+ ▸** . **CH- ▾** or the number buttons **0..9** .
- 6 Confirm with **OK** .
- 7 To end, press **TIMER** .
- 8 Switch off with **STANDBY** ⏻ .

'NexTVView Link'

This DVD recorder is equipped with the 'NexTVView Link' feature. If your television is also equipped with this function, you can mark TV programmes on the television for programming. These TV programmes will automatically be transmitted to a **TIMER** block on the DVD recorder. If you clear the marking of the TV programme on the television, the corresponding **TIMER** block on the DVD recorder will also be cleared.
 For more information, read the instruction manual of your TV set.

11 User preferences

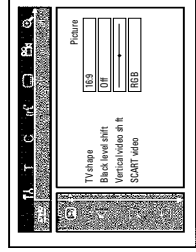
In this section you will learn how to set your user preferences on the DVD recorder. The symbols have the following meanings:

- Picture setting
- Sound setting
- Language setting
- Additional settings
- Remote control settings
- Disc settings
- Recording settings
- Installation

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Press **SYSTEM-MENU** on the remote control. The menu bar appears.
- 3 Select **TV** using **◀** or **▶** and confirm with **CH-▼**.
- 4 Select the appropriate function with **CH-▼** or **CH+▲** and confirm with **▶**.
- 5 Select the appropriate line using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Select the appropriate function using **CH-▼** or **CH+▲** or the setting with **◀** or **▶**.
- 7 Confirm the new setting by pressing **OK**.
- 8 To close the menu item, press **◀**.

Picture settings

You can choose the following features in this menu:



'TV shape'

The picture signal from your DVD Recorder can be set to match your TV screen.
'4:3 letterbox': for a 'wide-screen' picture with black bars at the top and bottom
'4:3 panscan': for a full-height picture, with the sides trimmed.
'16:9': for a wide-screen TV set (screen edge ratio 16:9)

'Black level shift'

Adapts the colour dynamics for NTSC playback

Problem solving for programmed recordings

ENGLISH	
PROBLEM	SOLUTION
The DVD recorder is not responding	<ul style="list-style-type: none"> ✓While a programmed recording is being made, you cannot operate your DVD recorder manually. If you want to cancel the programmed recording, press STANDBY.
'Switch off, timer recording' flashes on the TV screen.	<ul style="list-style-type: none"> ✓The DVD recorder was switched on several minutes before the start of a programmed recording. Switch off the DVD recorder using STANDBY. A programmed recording (timer) will only function if the DVD recorder is switched off (STANDBY button).
Error message: 'Insert recordable disc'	<ul style="list-style-type: none"> ✓Either a disc has not been inserted or the disc cannot be used for recording. Insert a disc on which recordings can be made. Switch off the DVD recorder using STANDBY.
The error message 'Disc locked' appears briefly on the screen.	<ul style="list-style-type: none"> ✓A write-protected disc has been inserted. Undo the write protection (see 'Preventing accidental erasing of discs' in 'Manual recording') or insert a different disc.
Error message: 'Memory full'	<ul style="list-style-type: none"> ✓If this error message appears after pressing TIMER, then all TIMER blocks are already programmed. No more recordings can be programmed. Press the ▶ button. If you want to clear or check a programmed recording (TIMER block), select it with CH+▲ or CH-▼.
The 'Data error' message appears on the screen.	<ul style="list-style-type: none"> ✓The data for the recording could not be transferred. Please check date, start time and end time of the programmed recording.
The 'Collision' message appears on the screen.	<ul style="list-style-type: none"> ✓Two programmed recordings overlap. ✓If you ignore this error message the show with the earlier start time will be recorded first. The start of the second show will not be recorded. ✓Change the setting for either of the two recordings. ✓Clear either of the two recordings

'Vertical video shift'

Use this feature to adjust the position of the picture on your TV left or right using ◀, ▶ to suit your TV set.

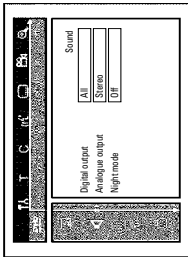
ENGLISH

'SCART video'

By default the recorder is set to 'RGB'. Select 'S-Video' if you want to connect an S-VHS recorder.

Sound settings

Depending on which audio outputs are used, you can select the settings in this menu. If you only use the analogue audio output (OUT L AUDIO R), select the settings 'Off' in the 'Digital output' menu.



'Digital output'

For devices connected to the DIGITAL AUDIO OUT socket, you can select from the following settings.

'All': Dolby Digital and DTS signals are fed unaltered to the digital output. MPEG-2 multi-channel signals are converted to PCM (Pulse Code Modulation).

For receivers/amplifiers with digital multi-channel sound decoders.

'PCM only': Dolby Digital and MPEG-2 multi-channel signals are converted to PCM (Pulse Code Modulation).

For receivers/amplifiers without digital multi-channel sound decoders.

'Off': Digital output switched off.

For devices with analogue audio input.

'Analogue output'

For devices connected to the analogue audio output (OUT L AUDIO R), you can select from the following settings.

'Stereo': For devices without DolbySurround or TruSurround. Use this setting if the DVD recorder is only connected to a stereo TV set.

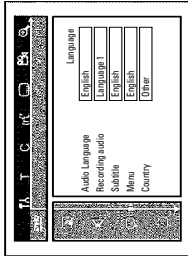
'Surround': Dolby Digital and MPEG-2 multi-channel are mixed down to a DOLBY surround-compatible two-channel output signal. For devices with Dolby Surround Pro Logic decoder.

'Night mode'

Night mode optimises the sound for playback at low volume. You are therefore less likely to disturb your neighbours. This only works for Dolby Digital audio on DVD video discs.

Language settings

You can choose the following settings in this menu:



'Audio Language'

Playback audio language

'Recording audio'

Audio recording

'Subtitle'

Subtitle language

'Menu'

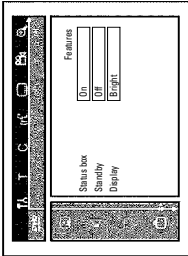
Screen menu language

'Country'

Country

Additional settings

You can select the following functions in this menu:



'Status box'

Along with the on screen menu, the OSD (On Screen Display) also displays information on the current operating status (counter, playback, recording, TV channel, etc.) on the TV screen. You can switch off the information about the operating status so that the on screen display (OSD) is not recorded during copying.

'On': The OSD information appears in every selected mode for a few seconds and disappears again.

'Off': The OSD information is switched off. It is no longer displayed on the screen.

'Standby'

To save power, you can switch off the clock display on the DVD recorder. Programmed (TIMER) recordings will still take place. In addition, you can present the most important features of the DVD recorder in scrolling text in the display (demo).

'Low power': If the DVD-Recorder is switched off (button **STANDBY** \odot), the clock display is also switched off.

'Off': If the DVD-Recorder is switched off (button **STANDBY** \odot), the clock display is visible.

'Demo mode': If the DVD recorder is switched off with the **STANDBY** \odot button, a list of the most important features is shown in the display.

'Display'

You can change the brightness of the display on the DVD recorder. This setting only affects the DVD recorder when it is switched on.

'Bright': The display appear with normal brightness. The disc tray light is switched on.

'Dimmed': The display appears less bright. The disc tray light is switched off.

'Off': The display and the disc tray light are switched off.

Remote Control settings

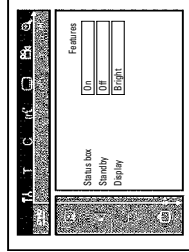
In this menu you can set the remote control type to which your DVD recorder should respond.

'DVD player': The DVD recorder responds to a DVD player remote control. The DVD recorder also responds to the remote control of a DVD player (remote control code RC-6). Choose this setting if your Philips TV remote supports DVD functions.

'DVD recorder': The DVD recorder only responds to the supplied remote control.

Disk feature menu

In this menu you can make the changes that relate to the disc:



'Access control'

Please read the next chapter on 'Access control (child lock)'.

'Auto resume'

If playback of a pre-recorded DVD video disc or video CD is interrupted (button **STOP** \blacksquare or **OPEN/CLOSE** \blacktriangle) when the disc is reloaded (disc is started) playback starts at the precise location where it stopped. This applies not only to the current disc but to the last 20 discs played.

This feature can be switched off if not required.

'PBC'

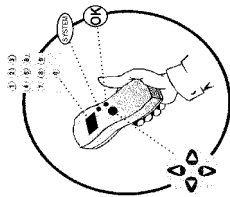
This line appears only if a VCD is loaded. This function lets you activate or deactivate the PBC menu (Playback Control) for video CDs. See 'Playing a (Super) Video CD'.

'Finalise disc'

This feature allows you to finalise DVD+R discs. If the disc has already been finalised this line will appear darker.

'Adapt disc format'

If a DVD-RW has been recorded in a computer drive or in another DVD recorder the index screen may not be displayed correctly. This feature allows you to change the format of the disc. It is therefore only visible if the disc format is different.



Child lock (DVD and VCD)

This feature enables discs to be locked for children. When Child Lock is on, a 4-digit code (PIN) needs to be entered before a disc can be played. You can also decide whether the inserted disc should always be played or should be played only once, despite the child lock.

•)Play always:

This disc is stored in a memory with space for 50 child-safe discs. If more than 50 discs are stored, the last disc in the list is removed and the new disc is added. The screen shows 'Child safe' at the start of playback.

•)Play once:

This disc is only authorised for single playback. If the recorder is switched off, the PIN code must be re-entered.

ENGLISH

Authorising a disc

- 1 Insert a disc. The access control box will appear after a short delay.
- 2 Using **CH+ ▲** or **CH- ▼** select **'Play once'** or **'Play always'**.
- 3 Enter your PIN code using the number buttons **0..9**.

Double-sided DVDs may have a different ID for each side. For these discs, each side must be authorised. Multi-volume video CDs may have a different ID for each volume. For these CDs, each volume must be authorised.

Locking unlocked discs

To lock a disc that was formerly authorised follow the instructions below

- 1 Insert a disc. Playback starts automatically. If the playback does not start automatically, press **PLAY ▶**.
- 2 Press the **STOP ■** button while the **'Parental Control'** icon is visible. The icon changes to **'LOCKED' ⓧ**. The disc is now locked.

Parental level control (DVD video only)

Films on pre-recorded DVD discs may contain scenes not suitable for children. Therefore, some discs may contain 'Parental Control' rating information that applies to the entire disc or to certain scenes on the disc.

The appropriate scenes have filter values that range from 1-8. If such a scene is detected during playback, the filter value set on the DVD recorder is compared to the scene. If the filter value is higher than the setting, an alternative scene will be played (if available).

Most DVDs apply the rating to an entire DVD. Therefore, if certain scenes exceed the rating you select, the entire disc will be blocked from viewing.

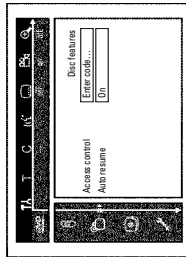
Activating/deactivating child lock

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON ⏻**.
- 3 Press **SYSTEM-MENU**. The menu bar appears.
- 4 Select the **TL** icon using **◀** or **▶**.
- 5 Select **'(Disc features)'** using **CH- ▼** or **CH+ ▲** and confirm with **▶**.
- 6 Confirm **'Access control'** using **▶**.
- 7 Enter a 4-digit code of your choice. If the code is new, you may have to enter the code a second time as confirmation.
- 8 Select **'Child lock'** using **CH+ ▲** or **CH- ▼** and confirm with **▶**.
- 9 Select the **ⓧ** icon using **CH- ▼** or **CH+ ▲**.
- 10 Confirm with **OK**.
- 11 Quit the feature using **◀** and **SYSTEM-MENU**.

Unauthorised discs can only be played by entering the four-digit PIN code. To deactivate the child lock, select the **ⓧ** icon in **9**.

Activating/deactivating parental level control

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU**. The menu bar appears.
- 4 Select the **TH** icon using **◀** or **▶**.
- 5 Select line **(Disc features)** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Confirm **Access control** using **▶**.
- 7 Enter a 4-digit code of your choice. If the code is new, you may have to enter the code a second time as confirmation.
- 8 Select the **Parental level** using **CH+▲** or **CH-▼** and confirm with **▶**. A bar appears to select the parental level.
- 9 Select the appropriate rating using **CH-▼**, **CH+▲** or the number buttons **0-9**.



Tip

What do the ratings mean?
 Rating 0 (displayed as -) parental control not active.
 Rating 1 (suitable for children)
 Rating 8 (only suitable for adults)

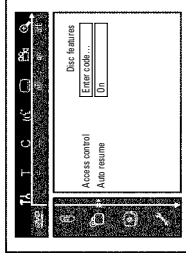
What happens if a DVD scene contains a higher level than the rating set?
 If the recorder does not find a suitable alternative, playback will stop and you must enter the four-digit code.

- 10 Confirm with **OK**. Quit using **◀** and **SYSTEM-MENU**.

Changing the country

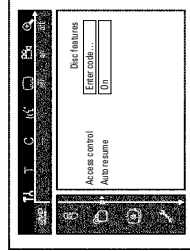
The set filter values depend on the respective country. It is therefore necessary to enter the country to which these filter values apply.

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON**.
- 3 Press **SYSTEM-MENU**. The menu bar appears.
- 4 Select the **TH** icon using **◀** or **▶**.
- 5 Select line **(Disc features)** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 6 Confirm the line **Access control** using **▶**.
- 7 Enter your four-digit code. If the code is new, you may have to enter the code a second time as confirmation.
- 8 Select **Change country** using **CH-▼** or **CH+▲** and confirm with **▶**.
- 9 Select the corresponding country using **CH+▲** or **CH-▼** and confirm with **OK**.
- 10 To end, press **◀** and then **SYSTEM-MENU**.



Changing the PIN code

- 1 Switch on the TV set. If required, select the programme number for the DVD recorder.
- 2 Switch on the DVD recorder using **STANDBY/ON** \odot .
- 3 Press **SYSTEM-MENU**. The menu bar appears.
- 4 Select the **TA** icon using \blacktriangleleft or \blacktriangleright .
- 5 Select **(Disc features)** using **CH- ∇** or **CH+ \blacktriangle** and confirm with \blacktriangleright .
- 6 Confirm **Access control** using \blacktriangleright .
- 7 Enter your four-digit PIN code. If the code is new, you may have to enter the code a second time as confirmation.
- 8 Select **Change code** using **CH+ \blacktriangle** or **CH- ∇** and confirm with \blacktriangleright .
- 9 Enter the new code using the number buttons **0..9**. Enter the same code again as confirmation.
- 10 Quit using \blacktriangleleft and **SYSTEM-MENU**.



Tip

I have forgotten my code

Press **STOP** \blacksquare four times (step 7), then press **OK**. Access control is now switched off. You can now enter a new code as described above.

4. Mechanical Instructions

4.1 Dismantling and Assembly of the Set

For item numbers please see the exploded views in chapter 10.

4.1.1 Manually opening the tray

- In case the loader is defective or cannot be opened electrically you can open the tray manually.
- Through a slot at the underside of the cabinet a slider that unlocks the tray can be accessed.
However in sets with drive VAD8031 (AV3) the slot is covered by an adhesive tape on the cabinet of the drive to prevent dust coming into the drive. Push through this adhesive tape by means of a thin screwdriver and move the slider to the left, see picture 4-1.
- **Make sure that an adhesive tape has been reapplied to the AV3 drive when repair is finished!**

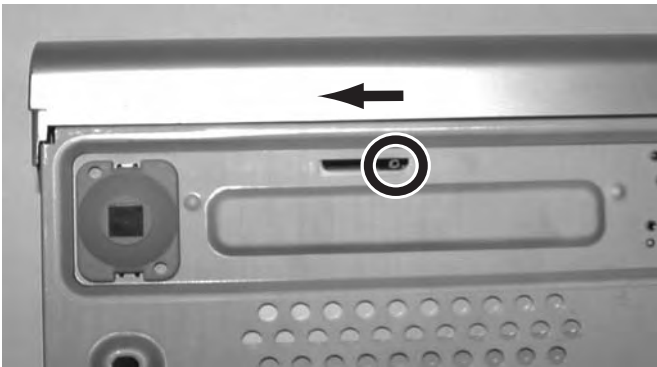


Figure 4-1

4.1.2 Front

- After removing the top cover, remove tray front (1), see picture 4-2
- Remove the three screws (2) that fix the front panel
- Release the two snap hooks on the sides (3) and remove the front (4)
- Remove the 9 screws (5) to remove the front plate (6), see picture 4-3

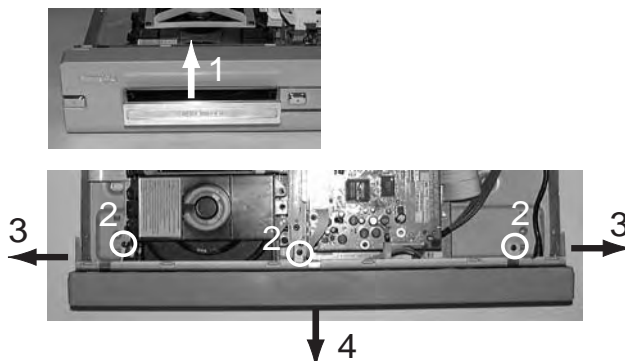


Figure 4-2

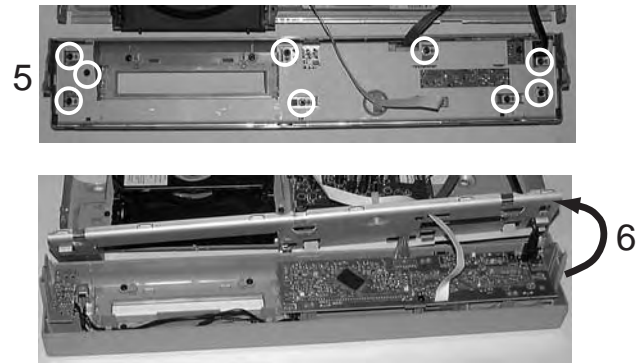


Figure 4-3

4.1.3 DVIO Board, only for sets with DV input and Digital Board 1.5

To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

- After removal of the EPG board (if present) the DVIO board can be reached
- Remove the two screws (1), see picture 4-4
- Release the snaps of the two board spacers 125
- Put the DVIO board in the service position with the extender board 3104 128 07770.

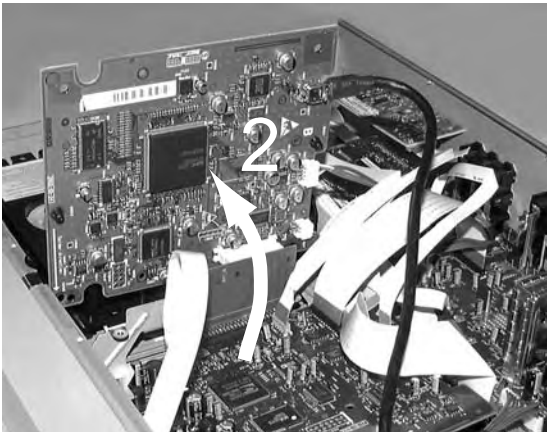
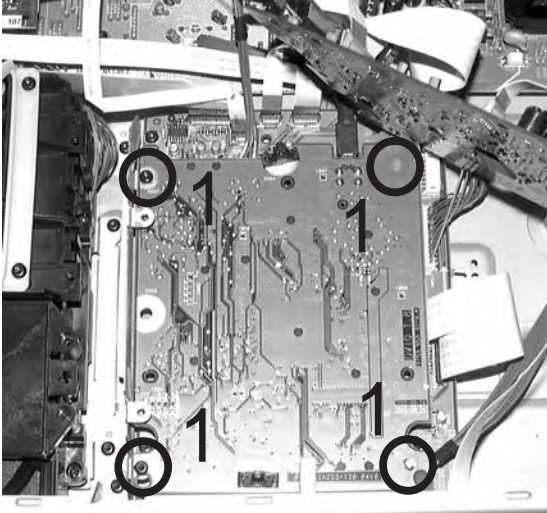


Figure 4-4

4.1.4 Digital Board

- After removal of EPG board (if present) and DVIO board (if present) the digital board can be reached
- Remove screws (1)
- Turn the PCB in the service position

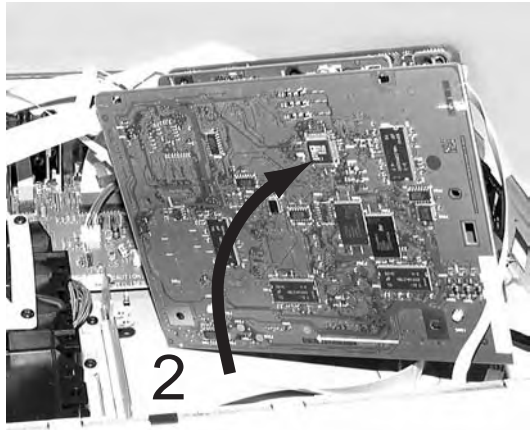
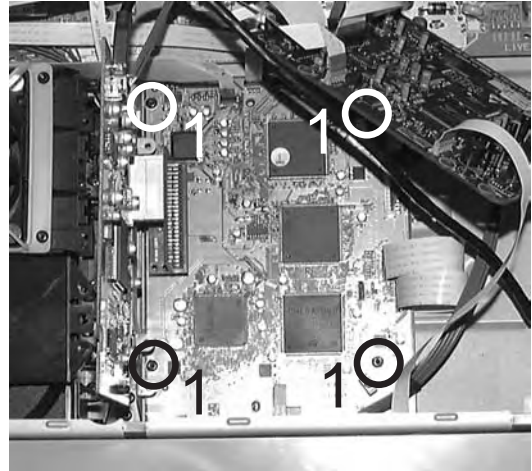


Figure 4-5

4.1.5 Basic Engine

- Remove the tray (1)
- Remove the four screws that fix the drive, see figure 4-6 or 4-7

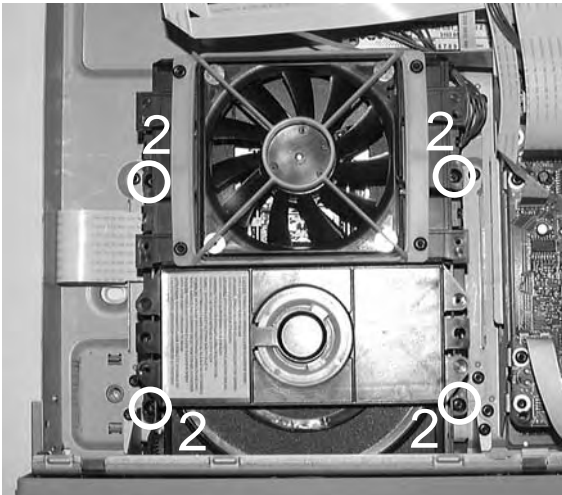
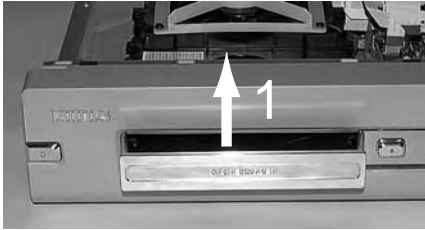


Figure 4-6

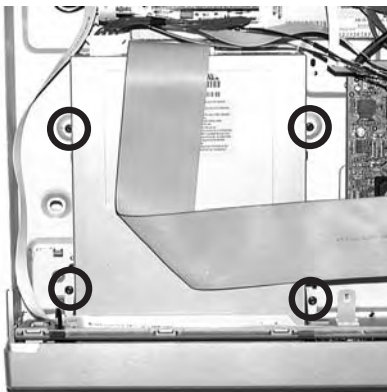


Figure 4-7

4.1.6 Analog Board

- Remove the 3 screws (1) that fix the back plate to the bottom plate, see picture 4-8
- Remove the 4 screws (2) that fix the Analog Board to the bottom plate
- In sets with fan remove the Fan assy by releasing the fixing screw (3)
- Remove screw safety holder (4)
- Unlock the two snaps hooks at the left and right (5), see picture 4-9, and pull the board and backplate out gently (6)
- Turn the PCB in the service position (7), see picture 4-10

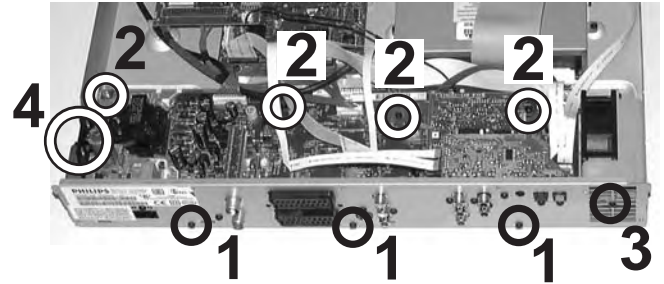


Figure 4-8

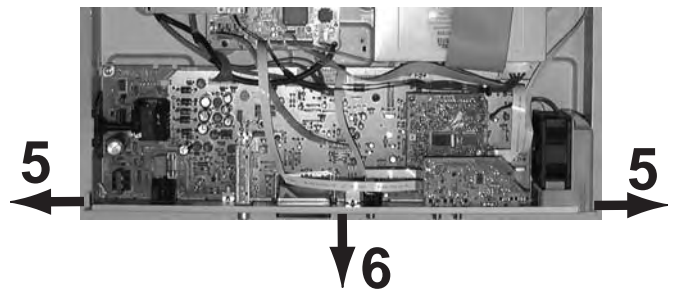


Figure 4-9

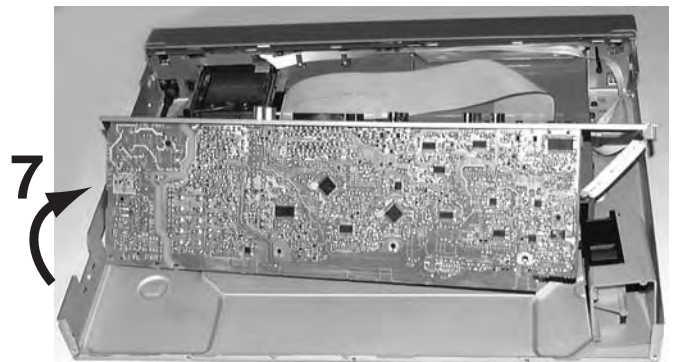
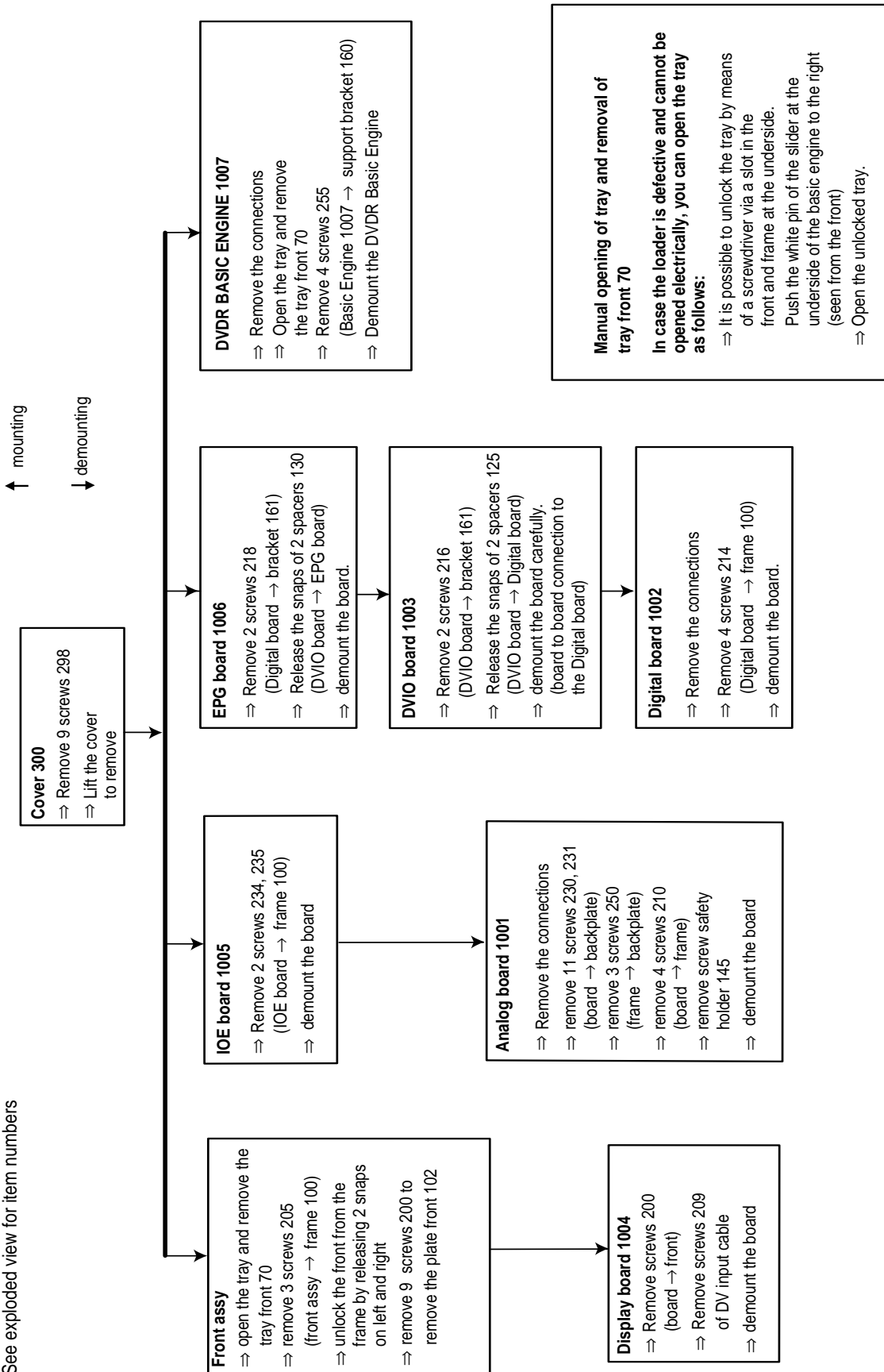


Figure 4-10

4.2 Dismantling Instructions

DISMANTLING INSTRUCTIONS

See exploded view for item numbers



Manual opening of tray and removal of tray front 70

In case the loader is defective and cannot be opened electrically, you can open the tray as follows:

- ⇒ It is possible to unlock the tray by means of a screwdriver via a slot in the front and frame at the underside.
- ⇒ Push the white pin of the slider at the underside of the basic engine to the right (seen from the front)
- ⇒ Open the unlocked tray.

Figure 4-11

5. Diagnostic Software

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

1. End user/Dealer script interface
2. Command Interface
3. Player script interface for sets with Digital Board 1.5, Empress
4. Menu interface for sets with Digital Board 1.5, Empress

5.1 End User/Dealer Script Interface

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

5.1.2 Structure

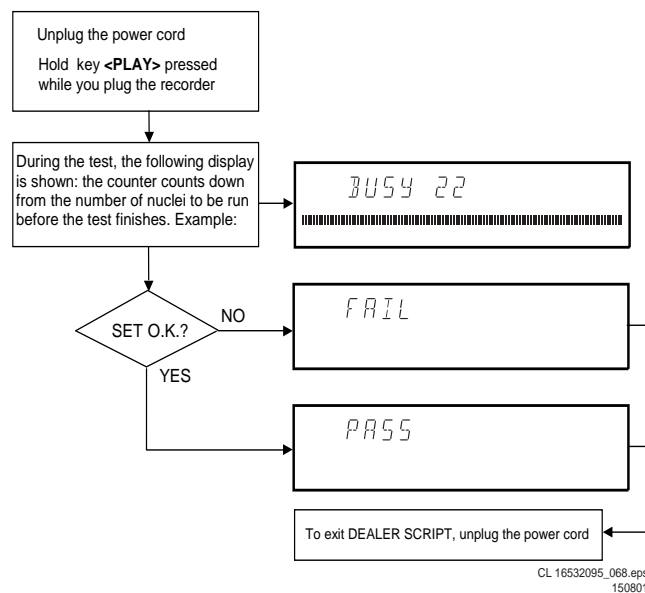


Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder.

5.1.3 Contents for sets with Digital Board 1.5, Empress

The nuclei called in the End user/Dealer script are the following:

Counter	Nucleus	Name	Description
22	104	HostdSdramWrR	checks all memory locations of the 4MB SDRAM
21	106	HostdDramWrR	checks all the DRAM connected to the microprocessor of the digital board
20	123	Hostdl2cNvram	checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM
19	202	SAA7118I2c	checks the interface between the Host I2C controller and the AVENC SAA7118 Video Input Processor
18	200	VideoEncl2c	checks the interface between the host I2C controller and Empress SAA6752
17	207	AudioEncl2c	checks the I2C connection between the host decoder and Empress SAA6752
16	204	AudioEncAccess	tests the HIO8 interface lines between the host decoder and the audio encoder
15	203	AudioEncSramAccess	checks the access of the SRAM by the audio encoder (address and data lines).
14	205	AudioEncSramWrR	tests the SRAM connected to the audio encoder
13	206	AudioEncInterrupt	tests the interrupt line between the host decoder and the audio encoder
12	300	VsmAccess	checks whether the VSM interrupt controllers and DRAM are accessible
11	303	VsmInterrupt	checks both interrupt lines between the VSM and the host decoder
10	302	VsmSdramWrR	tests the entire SDRAM of the VSM
9	1400	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	1401	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	601	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	500	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	700	AnalogueEcho	checks the interface between the host processor and the microprocessor on the analogue board
4	711	AnalogueNvram	checks the NVRAM on the analogue board
3	706	AnalogueTuner	checks whether the tuner on the analogue board is accessible

Counter	Nucleus	Name	Description
2	901	LoopAudioUserDealer	This nucleus tests the components on the audio signal path The host decoder - The analogue board - The audio encoder - The VSM Attention: the rear cinch audio out has to be connected to the front cinch audio in.
1	906	LoopVideoUserDealer	Nucleus for testing the components on the video signal system path: - The VIP - The video encoder - The VSM - The host decoder - The analogue board Attention: the rear cinch video out has to be connected to the front cinch video in.

5.1.4 Contents for sets with Digital Board Chrysalis

Included tests:	1.DS_ANAB_COMMUNICATIONECHO_NUC 2.DS_DCB_COMMUNICATIONECHO_NUC 3. DS_BROM_COMMUNICATION_NUC 4. DS_SYS_SETTINGSDISPLAY_NUC 5. DS_CHR_DEVTYPEGET_NUC 6. DS_CHR_INT_PIC_NUC 7. DS_CHR_DMA_NUC 8. DS_BROM_WRITEREAD_NUC 9. DS_NVRAM_COMMUNICATION_NUC 10. DS_NVRAM_WRITEREAD_NUC 11. DS_SDRAM_WRITEREADFAST_NUC 12. DS_FLASH_WRITEREAD_NUC 13.DS_FLASH_CHECKSUMPROGRAM_NUC 14.DS_SYS_HARDWAREVERSIONGET_NUC 15. DS_VIP_DEVTYPEGET_NUC 16. DS_VIP_COMMUNICATION_NUC 17. DS_DVIO_LINKDEVTYPEGET_NUC 18. DS_DVIO_PHYDEVTYPEGET_NUC 19. DS_DVIO_LINKCOMMUNICATION_NUC 20. DS_DVIO_PHYCOMMUNICATION_NUC 21.DS_PSCAN_COMMUNICATIONDENC_NUC 22.DS_PSCAN_COMMUNICATIONDEINTERLACER_NUC 23. DS_BE_COMMUNICATIONECHO_NUC 24.DS_ANAB_COMMUNICATIONIICNVRAM_NUC 25.DS_ANAB_COMMUNICATIONIICTUNER_NUC 26.DS_ANAB_COMMUNICATIONIICSOUNDPROCESSOR_NUC 27.DS_ANAB_COMMUNICATIONIICAVSELECTOR_NUC 28. DS_ANAB_CHECKSUMPROGRAM_NUC
-----------------	---

5.2 Player Script Interface only for sets with Digital Board 1.5 Empress

5.2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD recorder's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.

To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the DVDR module) require that a DVD+RW disc is inserted.

Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

STEP	DESCRIPTION	NUCLEUS
1	Press OPEN/CLOSE and PLAY at the same time and POWER ON the recorder to start the playerscript	2
2	The local display shows FPSEGMENTS . Press PLAY to start the test. First the <i>starburst pattern</i> is lit, then the <i>horizontal segments</i> are lit, followed by the <i>vertical segments</i> and the last test is <i>light all segments</i> test. After each of the 4 tests the user has to confirm that the correct pattern was lit. Press PLAY to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press RECORD to indicate that the correct pattern was not successfully lit. Press STOP to skip this nucleus.	502

5.2.2 Structure of the Player Script

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module. Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

- Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP	DESCRIPTION	NUCLEUS
3	The local display shows FPLABELS . Press PLAY to start the test. Press PLAY to confirm that all labels are lit. Press RECORD to indicate that not all labels are lit. Press STOP to skip this nucleus.	503
4	The local display shows FPLIGHT ALL . Press PLAY to start the test. Press PLAY to confirm that everything was lit. Press RECORD to indicate that not all patterns are lit. Press STOP to skip this nucleus.	520
5	The local display shows FPLED . Press PLAY to start the test. Press PLAY to confirm that the led is lit. Press RECORD to indicate that the led is not lit. Press STOP to skip this nucleus.	504
6	The local display shows FPKEYBOARD . Press PLAY to start the test. Attention all keys have to be pressed to get a positive result! Press PLAY for more than one second to confirm that all the keys were pressed and shown on the local display. If not all the keys were pressed, a FAIL message will appear on the local display. Press RECORD for more than one second to indicate that not all keys were pressed and shown on the local display. Press STOP for more than one second to skip this nucleus.	505
7	The local display shows FPREMOTE CONTROL . Press PLAY to start the test. Press PLAY to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result. Press RECORD to indicate that the key on the remote control was pressed but not shown on the local display. Press STOP to skip this nucleus.	506
8	The local display shows FPDIMMER . Press PLAY to start the test. Press PLAY to confirm that the text on the local display was dimmed. Press RECORD to indicate that the text on the local display was not dimmed. Press STOP to skip this nucleus.	518
9	The local display shows ROUTE VIDEO . Press PLAY to start the test. Press STOP to skip this nucleus.	712
10	The local display shows ROUTE AUDIO . Press PLAY to start the test. Press STOP to skip this nucleus.	713
11	The local display shows COLOUR-BAR ON . Press PLAY to start the test. Press STOP to skip this nucleus.	120
12	The local display shows PINK NOISE ON . Press PLAY to start the test. Press STOP to skip this nucleus.	115
13	The local display shows PINK NOISE OFF . Press PLAY to start the test. Press STOP to skip this nucleus.	116
14	The local display shows SINE ON . Press PLAY to start the test. Press STOP to stop the sine. Press STOP to skip this nucleus.	117
15	The local display shows COLOUR-BAR OFF . Press PLAY to start the test. Press STOP to skip this nucleus.	121
16	The local display shows BERESET . Press PLAY to start the test. Press STOP to skip this nucleus.	603
17	The local display shows BETRAY OPEN . Press PLAY to start the test. Press STOP to skip this nucleus.	616
18	The local display shows BETRAY CLOSE . Press PLAY to start the test. Press STOP to skip this nucleus.	615
19	The local display shows BEWRITE READ . Press PLAY to start the test. Press STOP to skip this nucleus.	617
20	The local display shows BETRAY OPEN . Press PLAY to start the test. Press STOP to skip this nucleus.	616
21	The local display shows BETRAY CLOSE . Press PLAY to start the test. Press STOP to skip this nucleus.	615
22	The local display shows READ ERRORLOG . Press PLAY to start the test. Press STOP to skip this nucleus. If the player test succeeded, the user/dealer script will start in an endless loop. If the player test failed, the local display will display FAIL and the error code	633

Remark

In case of failure, the display shows " FAIL XXXXXX ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.

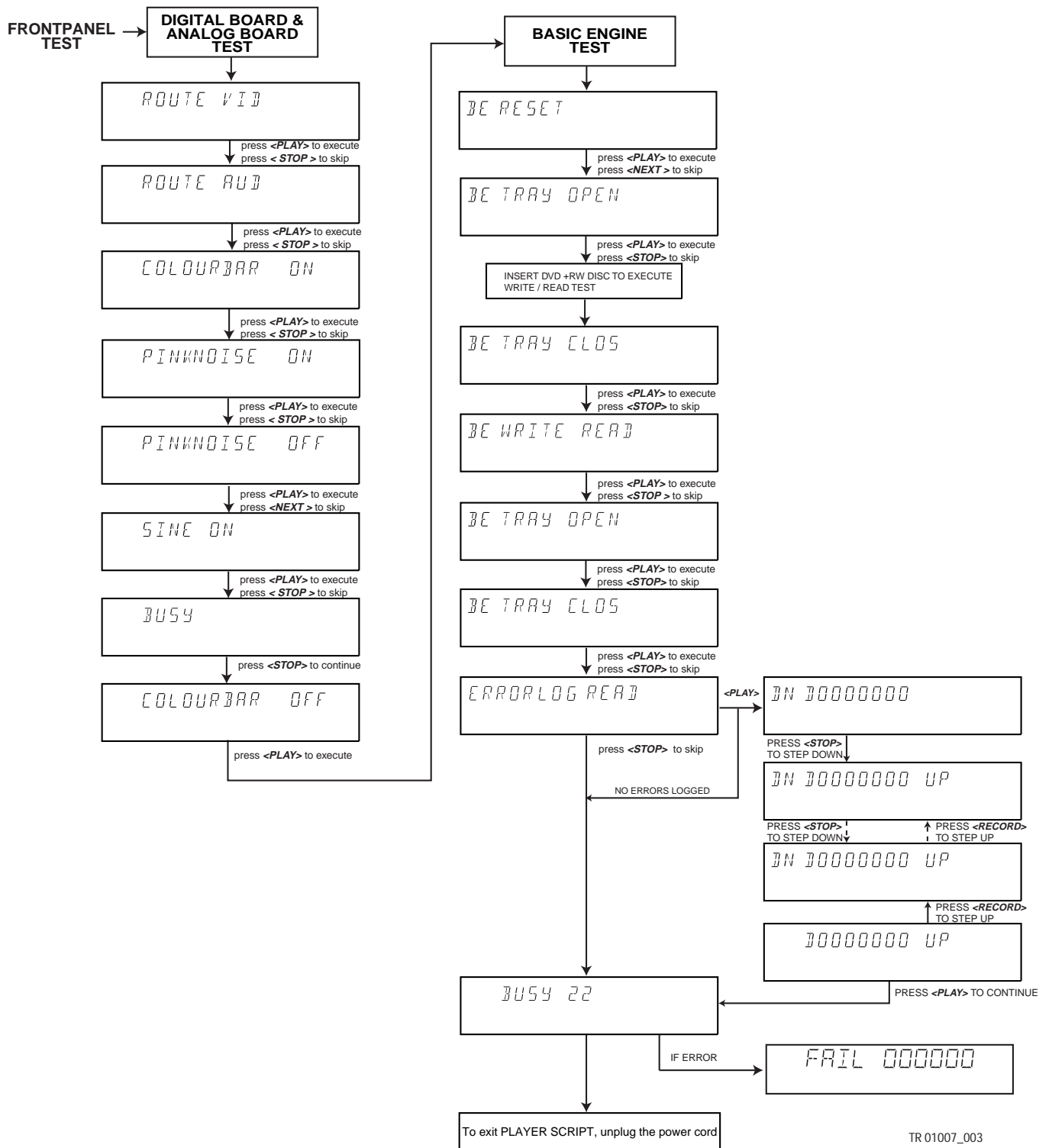


Figure 5-3

5.2.3 Error Log

Explanation:

The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown error codes are identical to the Nuclei Error Codes (paragraph 5.4).

5.2.4 Trade Mode

TRADE MODE

When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.

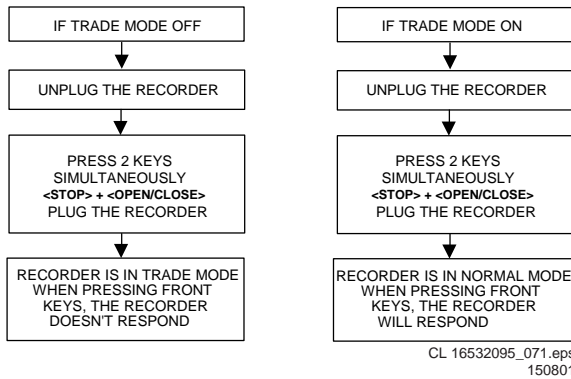


Figure 5-4

5.2.5 Virgin mode

If you want that the recorder starts up in Virgin mode, follow this procedure:

- Unplug the recorder
- plug the recorder again while you keep the STAND BY/ON key pressed
- the set starts up in Virgin mode.

5.3 Menu and Command Mode Interface

5.3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.

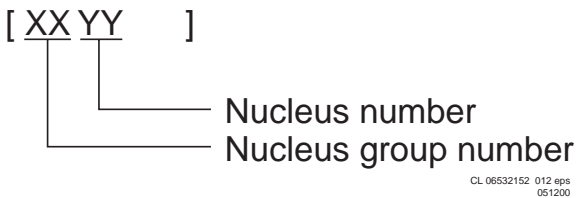


Figure 5-5

The following groups are defined for Digital Board 1.5, Empress:

Group number	Group name
0	Basic / Scripts
1	Host decoder (Sti5505 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel

Group number	Group name
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)

The following groups are defined for Digital Board Chrysalis:

Group number	Group name
0	Basic / Scripts
1	Chrysalis
2	Boot EEPROM
3	NVRAM
4	SDRAM
5	Flash
6	Video Input Processor
7	DVIO
8	Progressive Scan
9	Basic Engine
10	Display and Control Board
11	Analogue Board
12	System

5.3.2 Error Handling

Each nucleus returns an error code. This code contains six numerals, which means:

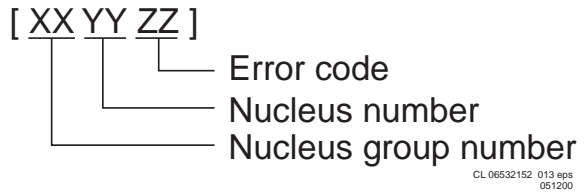


Figure 5-6

The nucleus group numbers and nucleus numbers are the same as above.

5.3.3 Command Mode Interface

Set-Up Physical Interface Components

Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD recorder to Service PC

The service PC must have a terminal emulation program (e.g. Hyperterminal) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Code number of PC interface cable: 3122 785 90017

Activation Digital Board 1.5 Empress

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```

DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface? [M] : @ c
DD:>

```

CL 16532095 073 eps
150801

Figure 5-7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Activation Digital Board Chrysalis

1. Pull the mains cord from the recorder and reconnect it again (reboot).
2. The next welcome message will appear on the PC:

Welcome screen D&S program

```

Factory Diagnostics and Service Software
DVD Video Recorder
Version 6 (Jan 9 2003, 11:11:15)

DS:>

```

Figure 5-8

Now, the prompt 'DS:>' will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei. If you see above shown screen, continue with paragraph 'Nuclei Codes'.

3. It is possible that the next messages will appear when starting the DVD+RW for the first time

Error messages D&S program

```

[MIS_DIV.WARNING,Digital Board Hardware Information is corrupt,]
Factory Diagnostics and Service Software
DVD Video Recorder
Version 6 (Jan 9 2003, 11:11:15)

WARNING,Digital Board Hardware Information is corrupt
DS:>

```

Figure 5-9a

Error messages D&S program

```

System error: Diversity string UnAccessible!! Eeprom problem!

Factory Diagnostics and Service Software
DVD Video Recorder
Version 8 (May 12 2003, 16:44:35)

WARNING,Digital Board Hardware Information is corrupt
DS:>

```

Figure 5-9b

In these cases, the boot EEPROM of the Chrysalis Digital Board does not contain the required string with the hardware information. To update the Digital Board with the correct string, nucleus 1226 must be executed.

See next section 'Diversity String Input'.

There can also be the next error message.

```

System error: Due to a setting in the Digital Board Diversity
Settings, the Recorder is unable to function properly.
Please change the hardware diversity settings by using the
proper nuclei BEFORE proceeding to the application!

The next Hardware Settings can be safely programmed:
Board name: FAILSAFE
Hardware ID: 21

Codec IC: PNK7100_MF3
Video Input Processor IC: SAA7118
Progressive Scan Deinterlacer IC: None
Progressive Scan Denc IC: ADV7196
I-Link physical layer circuit IC: PDI1394P25
I-Link link layer circuit IC: PDI1394P40
Audio clock: Clock scheme 1
Bit engine connector: available
IDE connector 1: available
IDE connector 2: not available
PCI connector: not available
RAM size: 32MByte
ROM size (NOR FLASH bank 1): 8MByte
ROM size (NOR FLASH bank 2): Not available
ROM size (NAND FLASH): Not available
Settings ID: 4641494C5341464521030300010101020101000020080000
Program these settings? [Y/N]
Programming the settings values...

Factory Diagnostics and Service Software
DVD Video Recorder
Version 8 (May 1 2003, 18:38:27)

DS:>_

```

Figure 5-9c

Enter "Y" to program a safe string. With this automatically generated string the board will work in principle but it has to be checked if all board settings were detected correctly.

Diversity String Input

- Execute nucleus 1226 to enter the string. Please see chapter 8.5 for details

Nucleus 1226 execution with string

```

D&S - HyperTerminal
File Edit View Call Transfer Help

DS:> 1226 4E310000000000022030300010101020100000020080000
122600:
Test OK @
DS:> _

Connected 0:01:41  Auto detect  19200 8-N-1  SCROLL  CAPS  NUM  Capture

```

Figure 5-10

- To check if the hardware info is filled correctly, you can execute nucleus 1228.

Nucleus 1228 info example

```

D&S - HyperTerminal
File Edit View Call Transfer Help

DS:> 1228

Settings ID: 4E310000000000022030300010101020100000020080000
Board name: N1
Hardware ID: 34
Codec IC: PMX7100_MF3
Video Input Processor IC: SAR7118
Progressive Scan Deinterlacer IC: None
Progressive Scan Denc IC: ADU7196
I-Link physical layer circuit IC: PDI1394P25
I-Link link layer circuit IC: PDI1394P40
Audio clock: Clock scheme 1
Bit engine connector: available
IDE connector 1: not available
IDE connector 2: not available
PCI connector: not available
RAM size 32MByte
ROM size (NOR FLASH bank 1) 8MByte
ROM size (NOR FLASH bank 2) Not available
ROM size (NAND FLASH) Not available
Bit Engine:

122800:
Test OK @
DS:> _

Connected 0:02:26  Auto detect  19200 8-N-1  SCROLL  CAPS  NUM  Capture  Print

```

Figure 5-11

- Exit the 'Terminal' program.
- Reboot the DVD recorder to allow the software to start.

Command Overview Digital Board 1.5 Empress

We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xx yy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On Note: Use nuclus 712 with parameter 07 to route the signals to the analogue board output
121	Colour-bar Off
122	NvramWrR
123	NvramI2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board
135	Video Test Signal OnNote: Use nuclus 712 with parameter 07 to route the signals to the analogue board output. Input: 135 [a] [b] a: Number of test image, 0. Horizontal colour-bar 1. White 2. Yellow 3. Light blue 4. Green 5. Magenta 6. Red 7. Blue 8. Black 9. Colour triangle (execution time is 12 seconds) 10. Test image for progressive scan (execution time is 6 seconds) b: Video standard, 0. PAL BDGHI 1. NTSC
136	Video Test Signal Off
137	Macrovision Off

Audio Video Decoder [02]

[xx yy] Number	Nuclei
200	Video Encoder I2C
202	SAA7118 I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts

[xx yy] Number	Nuclei
207	Audio Encoder I2C
208	SAA7118 select input
209	Empress Version

VSM [03]

[xx yy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xx yy] Number	Nuclei
400	Reset
401	Read
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xx yy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Disbar
516	Disbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xx yy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On

[xx yy] Number	Nuclei
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information
633	BE Read Error Log
634	BE Reset Error Log
638	Get Self Test Result
639	Radial Initialisation
640	Get OPU info

Analog Board [07]

[xx yy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
720	Bargraph Level Adjustment
721	Clock correction
722	Clock reference
723	Re-virginise Recorder
724	Flash Checksum
725	Tuner frequency selection Europe: To make video and audio signals from the tuner available on Scart2, send command "712 08". For Nafta/Apac: To make the black/white Video available on Y/C Rear Out connector, send command "712 08" Input: 725 [frequency in MHz*16] [system] System: NTSC=16, PAL BG=16, PAL I=32, PAL DK=48, SEC L=64, SEC LS=80, SEC BG=96, SEC DK=112
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board

[xx yy] Number	Nuclei
730	Store external presets
731	Get slash version
732	AFC Reference Voltage Tuner
736	Get EPG Version
737	Get operating hours in Tuner Mode

DVIO [08]

[xx yy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids
805	Execute DVIO module SelfTestInput: 805 [a] [b]Parameters: a=1/0...full Ram test, b=1/0...cable connected
806	Set DVIO led on.
807	Set DVIO led off.

Loop Nuclei [09]

[xx yy] Number	Nuclei
900	Digital Audio Loop(no function in Gen. 1.5 and Lead)
901	User / Dealer Audio Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop
906	User / Dealer Video Loop
907	User / Dealer Video VBI Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop
911	System Video Vip

Miscellaneous [14]

[xx yy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off
1415	Progressive Scan Route Enable
1416	Progressive Scan Route Disable

Scripts [00]

[xx yy] Number	Nuclei
1	UserDealer Script
2	Player Script

Routing Audio and Video*Route Video*

Nucleus Number: 712

Description

This nucleus routes the video signals on the analogue board to the destination determined by the input parameters

The paths that are available for video routing and their description (Euro region):

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	No Routing.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	No Routing.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	Input Signal is CVBS from Digital Board and it will be routed to Scart1 and Scart2.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART2.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	Signal path is routed Fast Blank from Scart2 pin16 and will be routed Scart1 pin16
12	Input Signal is YC from Digital Board and it will be routed to Scart1.
13	
14	No Routing.
15	Input Signal is CVBS from TUNER and it will be routed to Digital .
16	No Routing.
17	Input Signal is routed from digital board YC to REAR S-VIDEO(YC) OUT
18	Signal path is routed from digital board RGB to RGB SCART1 and from digital board CVBS to digital board CVBS.
19	No Routing.
20	Input RGB Signal is routed from Digital Board to SCART1(RGB),Input CVBS Signal from Digital Board to Digital Board and Fast Blanking Signal from Scart 2 to Scart1.
21	Input Y/C Signal from Digital Board is routed to Rear Y/C Connector and Input Y/c Signal from Front Y/C connector is routed to Digital Board.

Example

DD:> 712 01

71200: Video routing on the Analogue Board OK.

Test OK @

Route Audio

Nucleus Number: 713

Description

This nucleus routes the audio on the analogue board to the destination determined by the input parameters

The paths that are available for audio routing and their description (Europe version)

Path ID	Description
00	Input signal is from FRONT AUDIO IN and will be routed to the digital board.(This is done so that nucleus 901 works)
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	No Routing.
03	Input signal is AUDIO from SCART1 and will be routed to the digital board.
04	Input signal is AUDIO from SCART2 and will be routed to the digital board.
05	No routing.
06	No routing.
07	Input Audio signal is from the digital Board and it will be routed to the Scart 1 and Scart2
08	Input AUDIO signal from TUNER and will be routed to SCART2.
09	Input signal is AUDIO from SCART1 and will be routed to SCART2.
10	Input audio signal from Scart2 is routed to Scart1.
11	Input Audio signal is routed from DVIO to Scart2.
12	
13	No Routing.
14	Input is Audio Signal from DVIO and it will be routed to Digital Board.
15	Input is Audio Signal from TUNER and it will be routed to Digital Board..
16	No routing.
17	No Routing.
18	Input signal is from FRONT AUDIO IN and will be routed to SCART2.
21	Input signal is from FRONT AUDIO IN and will be routed to the digital board.(This is done so that nucleus 909.1 works)

EXAMPLE

DD:> 713 00

71300: Audio routing on the Analogue Board OK.

Test OK @

Below you will find an overview of the nuclei, their numbers, and their error codes. This overview is preliminary and subject to modifications.

Command overview Digital Board Chrysalis*Chrysalis (CHR)*

Nucleus Name	DS_CHR_DevTypeGet
Nucleus Number	100
Description	Sends the device ID and the module ids and revisions of the PNX7100 (Chrysalis) to the stdout port.
User Input	None
Example	<pre>DS:> 100 Device ID 7100 Codec ID PNX7100_MF2 F-BCU (0x0102) 1.0 INTC (0x011d) 1.0 PCI-XIO(0x0113) 1.0 SIF(0x013b) 1.0 EJTAG (0x0104) 0.0 S-BCU (0x0102) 1.0 BOOT (0x010a) 1.0 CONFIG (0x013f) 1.0 RESET (0x0123) 1.0 DEBUG (0x0116) 0.0 UART0 (0x0107) 0.1 UART1 (0x0107) 0.1 UART2 (0x0107) 0.1 UART3 (0x0107) 0.1 I2C0 (0x0105) 0.1 I2C1 (0x0105) 0.1 GPIO (0x013c) 1.0 SYNC (0x013a) 1.0 DISP0 (0xa015) 0.1 DISP1 (0xa00f) 0.0 OSD (0x0136) 0.1 SPU (0xa00e) 0.0 MIXER (0x0137) 1.0 DENC (0x0138) 0.1 CCIR (0x0139) 1.0 VDEC (0x0133) 0.1 PARSER (0xa00d) 0.0 DV (0xa00c) 0.0 BEI (0xa00a) 0.0 IDE (0xa009) 0.0 SGDX (0xa008) 0.0 BYTE (0xa00b) 0.0 OUTPUT (0xa003) 0.0 ACOMP (0xa000) 0.0 VFE (0xa001) 0.0 VCOMP (0xa002) 0.0 SCR (0x0000) 0.0 SIFF (0xa011) 0.0 WMD (0xa010) 0.0 AUDIO0 (0xa015) 0.1 AUDIO1 (0xa00f) 0.0 PSCAN (0xa018) 0.0 010000: Test OK @</pre>

Nucleus Name	DS_CHR_TestImageOn
Nucleus Number	101
Description	Generates a test-image of a selected video standard on selected video output on the digital board. When no input is given, the default values will be used. Use nucleus DS_ANAB_VideoRouting to route the video signal on the analogue board output
User Input	<p>The user has to decide which test image, video standard and video output must be used:</p> <p>Test image id:</p> <ul style="list-style-type: none"> 0 VERTICAL_COLOURBAR (default) 1 HORIZONTAL_COLOURBAR 2 WHITE 3 YELLOW 4 CYAN 5 GREEN 6 MAGENTA 7 RED 8 BLUE 9 BLACK 10 GRAY <p>Video standard:</p> <ul style="list-style-type: none"> PAL (default) NTSC <p>Video output:</p> <ul style="list-style-type: none"> ALL CVBS and YC and RGB (default) CVBS YC RGB YUV PSCAN progressive scan
Example	<pre>DS:> 101 010100: Test OK @ DS:> 101 0 pal cvbs 010100: Test OK @ DS:> 101 4 ntsc yc 010100: Test OK @</pre>

Nucleus Name	DS_CHR_TestImageOff
Nucleus Number	102
Description	Switches the test-image off.
User Input	None
Example	DS:> 102 010200: Test OK @

Nucleus Name	DS_CHR_SineOn
Nucleus Number	103
Description	Generate an audio sine signal on the audio output of the digital board. Note: Left channel 6kHz, right channel 12 kHz sine. Make sure to route the signal first.
User Input	None
Example	DS:> 103 010300: Test OK @

Nucleus Name	DS_CHR_SineOff
Nucleus Number	104
Description	Stop generating the audio sine signal
User Input	None
Example	DS:> 104 010400: Test OK @

Nucleus Name	DS_CHR_SineBurst
Nucleus Number	105
Description	Generate an audio sine signal on the audio output of the digital board for 4 seconds. Note: Left channel 6kHz, right channel 12 kHz sine with some known hick-ups
User Input	None
Example	DS:> 105 010500: Test OK @

Nucleus Name	DS_CHR_MuteOn
Nucleus Number	106
Description	Mute the audio outputs of the digital board
User Input	None
Example	DS:> 106 010600: Test OK @

Nucleus Name	DS_CHR_MuteOff
Nucleus Number	107
Description	De-mute the audio outputs of the digital board
User Input	None
Example	DS:> 107 010700: Test OK @

Nucleus Name	DS_CHR_DvLedOn
Nucleus Number	108
Description	Check the connection to the DV-LED on the digital board by switching it on
User Input	None
Example	DS:> 108 010800: Test OK @

Nucleus Name	DS_CHR_DvLedOff
Nucleus Number	109
Description	Switch off the DV-LED on the digital board
User Input	None

Example	DS:> 109 010900: Test OK @
---------	----------------------------------

Nucleus Name	DS_CHR_MacroVisionOn
Nucleus Number	110
Description	Turn on MacroVision.
User Input	None
Example	DS:> 110 011000: Test OK @

Nucleus Name	DS_CHR_MacroVisionOff
Nucleus Number	111
Description	Turn off MacroVision.
User Input	None
Example	DS:> 111 011100: Test OK @

Nucleus Name	DS_CHR_Peek
Nucleus Number	112
Description	Peek a value on a specified address
User Input	The address to peek on
Example	DS:> 112 0xa0700000 011200: Value read = 0x000001BD Test OK @

Nucleus Name	DS_CHR_Poke
Nucleus Number	113
Description	Poke a value on a specified address
User Input	The address to poke and the value: <address><value>
Example	DS:> 113 0xa0700000 0xaabbccdd 011300: Test OK @

Nucleus Name	DS_CHR_INT_PICInterrupts
Nucleus Number	114
Description	Test all interrupts of the priority interrupt controller
User Input	-
Example	DS:> 114 011400: Test OK @

Nucleus Name	DS_CHR_DMA_TestDMA
Nucleus Number	115
Description	Test the memory to memory DMA transfer
User Input	-
Example	DS:> 115 011500: Test OK @

Boot EEPROM (BROM)

Nucleus Name	DS_BROM_Communication
Nucleus Number	200
Description	Check the communication between the IIC controller of the Chrysalis and the boot EEPROM
User Input	None
Example	DS:> 200 020000: Test OK @

Nucleus Name	DS_BROM_WriteRead
Nucleus Number	201

Description	Check whether the Boot EEPROM can be written to and read from
User Input	None
Example	DS:> 201 020100: Test OK @

NVRAM

Nucleus Name	DS_NVRAM_Communication
Nucleus Number	300
Description	Check the communication between the IIC controller of the Chrysalis and the EEPROM
User Input	None
Example	DS:> 300 030000: Test OK @

Nucleus Name	DS_NVRAM_WriteRead
Nucleus Number	301
Description	Check whether the EEPROM can be written to and read from
User Input	None
Example	DS:> 301 030100: Test OK @

Nucleus Name	DS_NVRAM_Clear
Nucleus Number	302
Description	Make the EEPROM empty, containing all zeroes.
User Input	None
Example	DS:> 302 030200: Test OK @

Nucleus Name	DS_NVRAM_Modify
Nucleus Number	303
Description	Modifies one or more locations in NVRAM and updates the checksum of the section modified
User Input	1. The location that must be modified i.e. "ALL" "BOOT" "DIAGNOSTICS" "DOWNLOAD" "CONFIG" "RECORDER" or no string if an offset from the base address of the NVRAM is required 2. The offset and data which to put on the selected location <offset> <length> <data>
Example	DS:> 303 DIAGNOSTICS 5 1 0x5a 030300: Section is modified successfully Test OK @

Nucleus Name	DS_NVRAM_Read
Nucleus Number	304
Description	Read out one or more locations in the NVRAM
User Input	1. The location which must be read i.e. "ALL" "BOOT" "DIAGNOSTICS" "DOWN LOAD" "CONFIG" "RECORDER" or no string if an offset from the base address of the NVRAM is required 2. The offset and number of bytes to read <offset> <length>
Example	304 DIAGNOSTICS 0 6 030400: Value read = 0x00 0x00 0x00 0x00 0x00 0x5A Test OK @

SDRAM

Nucleus Name	DS_SDRAM_WriteRead
Nucleus Number	400
Description	Check all data lines, address lines and memory locations of the SDRAM
User Input	None
Example	DS:> 400 040000: Test OK @

Nucleus Name	DS_SDRAM_WriteReadFast
Nucleus Number	401
Description	Check all data lines and address lines of the SDRAM
User Input	None
Example	DS:> 401 040100: Test OK @

Nucleus Name	DS_SDRAM_Write
Nucleus Number	402
Description	Write to a specific memory address
User Input	1. The location that must be modified (SDRAM starts at address 0xA0000000) 2. The value to put on the selected location
Example	DS:> 402 0xa1000010 0xad112222 040200: Test OK @

Nucleus Name	DS_SDRAM_Read
Nucleus Number	403
Description	Read from a specific memory address
User Input	The location from which the data must be read (SDRAM starts at address 0xA0000000)
Example	DS:> 403 0xa1000010 040300: Value read = 0xAD112222 Test OK @

FLASH

Nucleus Name	DS_FLASH_DevTypeGet
Nucleus Number	500
Description	Get the device (revision) type information of the FLASH IC. (manufacturer and device ID)
User Input	None
Example	DS:> 500 050000: Found FLASH memory: Manufacturer ID: 0x01 Device ID : 0x01 Test OK @

Nucleus Name	DS_FLASH_WriteRead
Nucleus Number	501
Description	Check whether the FLASH can be written to and read from
User Input	None
Example	DS:> 501 050100: Test OK @

Nucleus Name	DS_FLASH_Read
Nucleus Number	502
Description	Read from a specific memory address in FLASH
User Input	The location from which data must be read (FLASH starts at address 0xB8000000)
Example	DS:> 502 0xb8000000 050200: Value read = 0x3C08A000 Test OK @

Nucleus Name	DS_FLASH_ChecksumProgram
Nucleus Number	503
Description	Check the checksum of the application partitions by recalculating and comparing partition checksums
User Input	None

Example	DS:> 503 050300: BootCode checksum is: 0xBABE5B6F, which is correct Diagnostics checksum is : 0xBABEBAFF, which is correct Download checksum is: 0xBABEEDBF, which is correct Application checksum is : 0xBABE8EEC, which is correct Test OK @
---------	--

Nucleus Name	DS_FLASH_CalculateChecksum
Nucleus Number	504
Description	Calculate the checksum over all memory addresses. Used to check entire FLASH contents
User Input	None
Example	DS:> 504 050400: The Checksum = 0xBABE30A4 Test OK @

Nucleus Name	DS_FLASH_CalculateChecksumFast
Nucleus Number	505
Description	Calculate a checksum over a selected number of address locations
User Input	None
Example	DS:> 505 050500: The Checksum = 0xBABEB064 Test OK @

Video Input Processor (VIP)

Nucleus Name	DS_VIP_DevTypeGet
Nucleus Number	600
Description	Get the device (revision) type information of the VIP IC
User Input	None
Example	DS:> 600 060000: Found SAA7118 Test OK @

Nucleus Name	DS_VIP_Communication
Nucleus Number	601
Description	Check the communication between the IIC controller of the chrysalis and the VIP IC
User Input	None
Example	DS:> 601 060100: Test OK @

Nucleus Name	DS_VIP_ClockOutputOn
Nucleus Number	602
Description	Switch the clock output on
User Input	None
Example	DS:> 602 060200: Test OK @

Nucleus Name	DS_VIP_ClockOutputOff
Nucleus Number	603
Description	Switch the clock output off
User Input	None
Example	DS:> 603 060300: Test OK @

Nucleus Name	DS_VIP_SelectInput
Nucleus Number	604
Description	Select an input video path to be switched to the analogue output pin (AOUT) of the VIP

User Input	The input to select, see table below. 1 CVBS_Y_IN_A 2 CVBS_OUT_B 3 CVBS_Y_IN_B 4 CVBS_Y_IN_C 6 C_IN 8 G_IN 9 Y_IN 13 B_IN 14 U_IN 18 R_IN 19 V_IN
Example	DS:> 604 1 060400: Test OK @

Digital Video Input Output (DVIO)

Nucleus Name	DS_DVIO_LinkDevTypeGet
Nucleus Number	700
Description	Get the device (revision) type information of the 1394 Link layer IC
User Input	None
Example	DS:> 700 070000: Device type of the link layer IC: ffc00301 Test OK @

Nucleus Name	DS_DVIO_PhyDevTypeGet
Nucleus Number	701
Description	Get the device (revision) type information of the 1394 Physical layer IC
User Input	None
Example	DS:> 701 070100: Device type of the phy layer IC: 0 Test OK @

Nucleus Name	DS_DVIO_LinkCommunication
Nucleus Number	702
Description	Check the accessibility of the 1394 Link layer IC by writing to and reading from a specific address
User Input	None
Example	DS:> 702 070200: Test OK @

Nucleus Name	DS_DVIO_PhyCommunication
Nucleus Number	703
Description	Check the accessibility of the 1394 Physical layer IC by writing to and reading from a specific address
User Input	None
Example	DS:> 703 070300: Test OK @

Nucleus Name	DS_DVIO_Routing
Nucleus Number	704
Description	Route a DV stream containing an audio and video signal through the physical and link layer ICs to the Chrysalis
User Input	None, test works for both NTSC and PAL
Example	DS:> 704 070400: Test OK @

Nucleus Name	DS_DVIO_DetectNode
Nucleus Number	705
Description	Check whether a DV node can be detected by the hardware
User Input	None, test works for both NTSC and PAL

Example	DS:> 705 070500: Test OK @
---------	----------------------------------

Nucleus Name	DS_DVIO_DetectStream
Nucleus Number	706
Description	Check whether a DV stream can be detected by the hardware
User Input	None, test works for both NTSC and PAL
Example	DS:> 706 070600: Test OK @

Progressive Scan (PSCAN)

Nucleus Name	DS_PSCAN_CommunicationDenc
Nucleus Number	801
Description	Check the communication between the IIC controller of the chrysalis and the progressive scan DENC-IC
User Input	None
Example	DS:> 801 080100: Test OK @

Nucleus Name	DS_PSCAN_TestImageOn
Nucleus Number	802
Description	Generate the test images that are present on the progressive scan IC.
User Input	In case of ADV7196: When no input is given "HATCH" is the default -"HATCH" -"FRAME" Remark: "HATCH" is a crosshatch test pattern (horizontal and vertical white lines are displayed against a black background) "FRAME" is a uniform coloured frame/field test pattern (default white). In case of FLI2300: Nothing.
Example	DS:> 802 HATCH 080200: Test OK @

Nucleus Name	DS_PSCAN_TestImageOff
Nucleus Number	803
Description	Switch off the generated test image
User Input	None
Example	DS:> 803 080300: Test OK @

Nucleus Name	DS_PSCAN_TestImageColourSettingsSet
Nucleus Number	804
Description	Set the colour of the hatch- or the frame- field to a different value than the default white
User Input	A colour string of one of the next non-case sensitive strings (WHITE, BLACK, RED, GREEN, BLUE, YELLOW, CYAN, MAGENTA) or Y Cr Cb (hexa-) decimal values.
Example	DS:> 804 yellow 080400: Test OK @ DS:> 804 0x6a 0xde 0xca 080400: Test OK @

Nucleus Name	DS_PSCAN_TestImageColourSettingsGet
Nucleus Number	805
Description	Get the colour settings of the hatch- or the frame- field.
User Input	None
Example	DS:> 805 080500: Colour Y Cr Cb values: 0xD2 0x92 0x10 Test OK @

Nucleus Name	DS_PSCAN_Routing
Nucleus Number	806
Description	Route a video signal from the host processor through the progressive scan ICs to the progressive scan output of the set. Note: to route the progressive scan to the output of the set, first call nucleus 1112 with parameter 0 (video routing on analogue board).
User Input	None
Example	DS:> 806 080600: Test OK @

Nucleus Name	DS_PSCAN_DevTypeGetDeinterlacer
Nucleus Number	807
Description	Get the device (revision) type information of the progressive scan deinterlacer.
User Input	None
Example	DS:> 807 080700: Chip name : 2300 Chip version : 1 Test OK @

Nucleus Name	DS_PSCAN_CommunicationDeinterlacer
Nucleus Number	808
Description	Check the communication between the IIC controller of the chrysalis and the progressive scan Deinterlacer-IC
User Input	None
Example	DS:> 808 080800: Test OK @

Basic Engine (BE)

Nucleus Name	DS_BE_CommunicationEcho
Nucleus Number	900
Description	Check the communication between the digital board and the basic engine by issuing an echo command over the S2B interface
User Input	None
Example	DS:> 900 090000: Test OK @

Nucleus Name	DS_BE_Reset
Nucleus Number	901
Description	Reset the basic engine
User Input	None
Example	DS:> 901 090100: Test OK @

Nucleus Name	DS_BE_VersionGet
Nucleus Number	903
Description	Get the version of the basic engine and that of the optical unit
User Input	None
Example	DS:> 903 090300: BE version = 20.09.18 Optical unit version = 3C.00.09.41.08 Test OK @

Nucleus Name	DS_BE_GetSelftestResult
Nucleus Number	902
Description	Return the self-test results through the service port
User Input	None
Example	DS:> 902 090200: Test OK @

Nucleus Name	DS_BE_TrayOut
Nucleus Number	904
Description	Open the tray of the basic engine
User Input	None
Example	DS:> 904 090400: Test OK @

Nucleus Name	DS_BE_TrayIn
Nucleus Number	905
Description	Close the tray of the basic engine
User Input	None
Example	DS:> 905 090500: Test OK @

Nucleus Name	DS_BE_WriteReadDvdRw
Nucleus Number	906
Description	Write data to and read data from a DVD+RW disc through the basic engine for verification of the writing
User Input	None
Example	DS:> 906 090600: Testing on sector 0x5dbe0: OK Test OK @

Nucleus Name	DS_BE_WriteReadDvdR
Nucleus Number	907
Description	Write data to and read data from a DVD+R disc through the basic engine for verification of the writing
User Input	None
Example	DS:> 907 090700: Testing on sector 0x36210: OK Test OK @

Nucleus Name	DS_BE_StatisticalInformationGet
Nucleus Number	908
Description	Retrieve the statistical information from the basic engine
User Input	None
Example	DS:> 908 Number of times Tray went Open/Closed : 4 Total minutes the CD laser was on : 0 Total minutes the DVD laser was on : 0 Total minutes the write laser was on : 0 090800: Test OK @

Nucleus Name	DS_BE_StatisticalInformationReSet
Nucleus Number	909
Description	Reset the statistical information in the basic engine
User Input	None
Example	DS:> 909 090900: Test OK @

Nucleus Name	DS_BE_ErrorLogGet
Nucleus Number	910
Description	Get the error log from the basic engine
User Input	None
Example	DS:> 910 Momentary errors (0-9): 0x21 0x00 0x00 0x20 0x00 0x00 0x00 0x00 0x00 0x00 Cumulative errors (1-9): 0x00 0x80 0x20 0x00 0x00 0x00 0x00 0x00 0x00 Software fatal assert : 256 cpowermanager.cpp 091000: Test OK @

Nucleus Name	DS_BE_ErrorLogReset
Nucleus Number	911
Description	Reset the error log in the basic engine
User Input	None
Example	DS:> 911 091100: Test OK @

Nucleus Name	DS_BE_JitterOptimise
Nucleus Number	912
Description	Perform jitter optimisation: A formatted DVD must be loaded into the engine before executing this nucleus
User Input	none
Example	DS:> 912 Test OK @

Nucleus Name	DS_BE_FocusOn
Nucleus Number	913
Description	Put the laser of the BE into focus
User Input	None
Example	DS:> 913 091300: Test OK @

Nucleus Name	DS_BE_FocusOff
Nucleus Number	914
Description	Turn off putting the laser of the BE into focus
User Input	None
Example	DS:> 914 091400: Test OK @

Nucleus Name	DS_BE_MotorOn
Nucleus Number	915
Description	Turn on the turntable motor
User Input	None
Example	DS:> 915 091500: Test OK @

Nucleus Name	DS_BE_MotorOff
Nucleus Number	916
Description	Turn off the turntable motor
User Input	None
Example	DS:> 916 091600: Test OK @

Nucleus Name	DS_BE_RadialOn
Nucleus Number	917
Description	Close the radial loop
User Input	A formatted DVD must be loaded into the engine before executing this nucleus
Example	DS:> 917 091700: Test OK @

Nucleus Name	DS_BE_RadialOff
Nucleus Number	918
Description	Open the radial loop
User Input	None
Example	DS:> 918 091800: Test OK @

Nucleus Name	DS_BE_RadialCalibration
Nucleus Number	919
Description	Calibrate the radial loop
User Input	A formatted DVD must be loaded into the engine before executing this nucleus
Example	DS:> 919 091900: Test OK @

Nucleus Name	DS_BE_Tilt
Nucleus Number	920
Description	Test the tilt mechanism control loop, or allow its proper functioning to be measured. Before executing this nucleus a disc must be loaded into the recorder
User Input	None
Example	DS:> 920 092000: Tilt sensor bathtub: (71,-12,145)(68,-12,135)(62,-10,120)(56,-92,97)(50,-75,86) (44,-59,80)(41,-52,80)(35,-37,86)(29,-22,86) (23,-7,92)(17,8,111)(11,23,135)(8,31,138)(5,39,158) Test OK @

Nucleus Name	DS_BE_CheckDisc
Nucleus Number	921
Description	Check whether there is a disc inside the BE
User Input	None
Example	DS:> 921 092100: A DVD+Rewritable is loaded (disc is empty or partially recorded) Test OK @ DS:> 921 092100: No Disc is loaded Test OK @

Nucleus Name	DS_BE_SledgeMotor
Nucleus Number	922
Description	Send the sledge to its home position, then to the middle of the disc, and then to the end.
User Input	None
Example	DS:> 922 092200: Test OK @

Nucleus Name	DS_BE_ReadTocInfo
Nucleus Number	924
Description	Read the TOC from the disc. This gives a good indication if the BE works properly..
User Input	None
Example	DS:> 924 092400: TOC info [hex] = 91 3A 0C Test OK@ DS:> 924 092403: The BE returned: 0x10 #{no_disc_error} No disc is detected Error@ DS:> 924 092403: The BE returned: 0x1e #{illegal_medium_error} Engine unable to handle current disc. Probably illegal medium. Error @

Nucleus Name	DS_BE_DiscErase
Nucleus Number	925
Description	Perform a DC-erase on a DVD+RW disc.
User Input	None

Example	DS:> 925 The entirely disc will be erased. Are you sure you want this?[y/n] 092500: Test OK @
---------	---

Nucleus Name	DS_BE_RegionCodeSet
Nucleus Number	928
Description	Set the region code in the AV3.
User Input	Region code
Example	DS:> 928 1 092800: Test OK @ DS:> 928 This nucleus is not supported by the engine 092800: Test OK @

Nucleus Name	DS_BE_RegionCodeGet
Nucleus Number	929
Description	Read the region code from the AV3.
User Input	None
Example	DS:> 929 092900: DVD region 1 Test OK @ DS:> 929This nucleus is not supported by the engine 092900: Test OK @

Nucleus Name	DS_BE_RegionCounterReset
Nucleus Number	930
Description	Reset the region counter in the AV3.
User Input	None
Example	DS:> 930 093000: Test OK @ DS:> 930 This nucleus is not supported by the engine 093000: Test OK @

Display and Control Board (DCB)

Nucleus Name	DS_DCB_CommunicationEcho
Nucleus Number	1000
Description	Check the communication between the digital board and the DCB by issuing an echo command
User Input	None
Example	DS:> 1000 100000: Test OK @

Nucleus Name	DS_DCB_VersionGet
Nucleus Number	1001
Description	Get the version of the DCB
User Input	None
Example	DS:> 1001 100100: DCB version: 13 Test OK @

Nucleus Name	DS_DCB_LightDisplay
Nucleus Number	1002
Description	Light the entire display of the DCB, and clear the display after confirmation. User confirmation is necessary.
User Input	None

Example	DS:> 1002 100200: Test OK @
---------	-----------------------------------

Nucleus Name	DS_DCB_Keyboard
Nucleus Number	1004
Description	Check all keys of the keyboard by confirming the key-code displayed of each key.
User Input	None
Example	DS:> 1004 100400: Test OK @

Nucleus Name	DS_DCB_RemoteControl
Nucleus Number	1005
Description	Check the interface between the remote control and the DCB by checking the key-code displayed
User Input	None
Example	DS:> 1005 100500: Test OK @

Nucleus Name	DS_DCB_Led
Nucleus Number	1006
Description	Switch the record LED on, and after confirmation off. The user confirms by pressing the REC key, STOP key, or the PLAY key on the local keyboard. The PLAY key confirms that the LED is on and the REC key
User Input	None
Example	DS:> 1006 100600: Test OK @

Analogue Board (ANAB)

Nucleus Name	DS_ANAB_CommunicationEcho
Nucleus Number	1100
Description	Check the communication between the digital board and the analogue board by issuing some echo string.
User Input	None
Example	DS:> 1100 110000: Hello Analogue Board Test OK @

Nucleus Name	DS_ANAB_CommunicationIcNvram
Nucleus Number	1101
Description	Check the communication between the digital board and the NVRAM on the analogue board.
User Input	None
Example	DS:> 1101 110100: Test OK @

Nucleus Name	DS_ANAB_CommunicationIcTuner
Nucleus Number	1102
Description	Check the communication between the digital board and the tuner on the analogue board
User Input	None
Example	DS:> 1102 110200: Test OK @

Nucleus Name	DS_ANAB_CommunicationIcDataSlicer
Nucleus Number	1103
Description	Check the communication between the digital board and the data slicer on the analogue board
User Input	None

Example	DS:> 1103 110300: Test OK @
---------	-----------------------------------

Nucleus Name	DS_ANAB_CommunicationIcSoundProcessor
Nucleus Number	1104
Description	Check the communication between the digital board and the sound processor on the analogue board
User Input	None
Example	DS:> 1104 110400: Test OK @

Nucleus Name	DS_ANAB_CommunicationIcAVSelector
Nucleus Number	1105
Description	Check the communication between the digital board and the A/V-selector on the analogue board
User Input	None
Example	DS:> 1105 110500: Test OK @

Nucleus Name	DS_ANAB_HardwareVersionGet
Nucleus Number	1106
Description	Get the hardware version of the analogue board
User Input	None
Example	DS:> 1106 110600: Analogue hardware version : 11 Test OK @

Nucleus Name	DS_ANAB_SoftwareVersionBootGet
Nucleus Number	1107
Description	Get the software version of the boot software of the analogue board
User Input	None
Example	DS:> 1107 110700: Bootcode application version : 11.00.11 Test OK @

Nucleus Name	DS_ANAB_SoftwareVersionDownloadGet
Nucleus Number	1108
Description	Get the software version of the download software of the analogue board
User Input	None
Example	DS:> 1108 110800: Download application version : 11.00.06 Test OK @

Nucleus Name	DS_ANAB_SoftwareVersionApplGet
Nucleus Number	1109
Description	Get the software version of the application software of the analogue board
User Input	None
Example	DS:> 1109 110900: Recorder application version : 11.00.23 Test OK @

Nucleus Name	DS_ANAB_SoftwareVersionDiagnosticsGet
Nucleus Number	1110
Description	Get the software version of the diagnostic software of the analogue board
User Input	None
Example	DS:> 1110 111000: Diagnostics application version : 11.00.13 Test OK @

Nucleus Name	DS_ANAB_ChecksumProgram
Nucleus Number	1111

Description	Check the checksum of the several partitions by recalculating and comparing partition checksums
User Input	None
Example	DS:> 1111 BootCode checksum is: 0xBABE6240, which is correct Diagnostics checksum is : 0xBABEBEAD, which is correct Download checksum is: 0xBABEA6B7, which is correct Application checksum is : 0xBABEB277, which is correct 111100: Test OK @

Nucleus Name	DS_ANAB_VideoRouting
Nucleus Number	1112
Description	Perform the routing of the video paths on the analogue board
User Input	The user has to input the correct parameter for the routing (see table 'video routing' below).
Example	DS:> 1112 00 111200: Test OK @

Video routing paths (Europe)

Path ID	Description
0	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
1	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
2	No Routing.
3	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
4	No Routing.
5	Input signal is CVBS from SCART1 and will be routed to the digital board.
6	Input signal is CVBS from SCART2 and will be routed to the digital board.
7	Input Signal is CVBS from Digital Board and it will be routed to Scart1 and Scart2.
8	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART2.
9	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	Signal path is routed Fast Blank from Scart2 pin16 and will be routed SCART1 pin16
12	Input Signal is YC from Digital Board and it will be routed to SCART1.
13	
14	No Routing.
15	Input Signal is CVBS from TUNER and it will be routed to Digital .
16	No Routing.
17	Input Signal is routed from digital board YC to REAR S-VIDEO(YC) OUT
18	Signal path is routed from digital board RGB to RGB SCART1 and from digital board CVBS to digital board CVBS.
19	No Routing.
20	Input RGB Signal is routed from Digital Board to SCART1(RGB),Input CVBS Signal from Digital Board to Digital Board and Fast Blanking Signal from SCART2 to SCART1.
21	Input Y/C Signal from Digital Board is routed to Rear Y/C Connector and Input Y/C Signal from Front Y/C connector is routed to Digital Board.

Video routing paths (NAFTA)

Path ID	Description
0	No Routing.
1	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.This routing is same as the above path id.
2	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
3	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.
4	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
5	No Routing.
6	No routing.
7	No routing.
8	Input signal is VIDEO(CVBS) from TUNER and will be routed to Y Pin of Rear Y/C Connector.This will give only black/White Picture .
9	Input signal is from YUV IN and will be routed to YUV OUT.This is possible only if Digital Board routes back YUV signal received back to the Analogue board(DENC)

10	No routing.
11	No routing.
12	No Routing.
13	No Routing.
14	No Routing.
15	Input CVBS Signal from Tuner is routed to Digital Board..
16	No Routing.
17	No Routing.
18	Input Signal from CVBS Rear In is routed to Digital Board. This is the same as path ID 02.
19	Input Y/C signal from Digital Board is routed to Y/C Rear Out Connector and Input signal from Y/C Front In Connector is routed to Y/C Digital Board.
20	Y/C signal from Digital Board is routed to Y/C Rear Out Connector and Input signal from Y/C Rear In Connector is routed to Y/C Digital Board.
23	The Video signal received from the Digital board will be output on Modulator channel 3.
24	The Video signal received from the Digital board will be output on Modulator channel 4.

Nucleus Name	DS_ANAB_AudioRouting
Nucleus Number	1113
Description	Perform the routing of the audio paths on the analogue board
User Input	The user has to input the correct parameter for the routing (see table 'audio routing' below)
Example	DS:> 1113 00 111300: Test OK @

Audio routing paths (Europe)

Path ID	Description
0	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
1	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
2	No Routing.
3	Input signal is AUDIO from SCART1 and will be routed to the digital board.
4	Input signal is AUDIO from SCART2 and will be routed to the digital board.
5	No routing.
6	No routing.
7	Input Audio signal is from the digital Board and it will be routed to the SCART1 and SCART2
8	Input AUDIO signal from TUNER and will be routed to SCART2.
9	Input signal is AUDIO from SCART1 and will be routed to SCART2.
10	Input audio signal from SCART2 is routed to SCART1.
11	Input Audio signal is routed from DVIO to SCART2.
12	
13	No Routing.
14	Input is Audio Signal from DVIO and it will be routed to Digital Board.
15	Input is Audio Signal from TUNER and it will be routed to Digital Board..
16	No routing.
17	No Routing.
18	Input signal is from FRONT AUDIO IN and will be routed to SCART2.
21	Input signal is from FRONT AUDIO IN and will be routed to the digital board.

Audio routing paths (NAFTA)

Path ID	Description
0	No Routing.
1	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
2	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
3	Input Audio Signal is routed from FRONT Cinch In to Digital Board.(This is same as path ID 01)
4	Input Signal is from Rear Cinch In1 and it will be routed to Digital Board..
5	No routing.
6	No routing.
7	No routing.
8	No Routing.
9	No routing.
10	No Routing.
11	No Routing.
12	No Routing.

13	Input Signal is from Digital Board and it will be routed to the digital board.
14	No routing.
15	Input is Audio Signal from TUNER and it will be routed to Digital Board.
16	Input signal is AUDIO from dvio board and will be routed to Digital Board.
17	No routing.
18	No routing.
19	No routing.
20	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
21	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
22	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
23	The Audio signal received from the Digital board will be outputted on Modulator channel 3.
24	The Audio signal received from the Digital board will be outputted on Modulator channel 4.

Nucleus Name	DS_ANAB_SelectTunerChannel																									
Nucleus Number	1114																									
Description	Set the tuner to receive a valid audio and video signal																									
User Input	<p><Frequency*16> <video standard id> Tuner frequency: to tune the tuner to e.g. 216 MHz, this parameter must be 3456. (Since 216*16 = 3456. This is to avoid the decimal points to the parameter list.) Video standard id: The table below shows which video standards are possible</p> <table border="1"> <thead> <tr> <th>Video standard id</th> <th>Europe</th> <th>NAFTA</th> </tr> </thead> <tbody> <tr><td>16</td><td>PAL_BG</td><td>NTSC</td></tr> <tr><td>32</td><td>PAL_I</td><td>Invalid</td></tr> <tr><td>48</td><td>PAL_DK</td><td>Invalid</td></tr> <tr><td>64</td><td>SEC_L</td><td>Invalid</td></tr> <tr><td>80</td><td>SEC_LS</td><td>Invalid</td></tr> <tr><td>96</td><td>SEC_BG</td><td>Invalid</td></tr> <tr><td>112</td><td>SEC_DK</td><td>Invalid</td></tr> </tbody> </table>		Video standard id	Europe	NAFTA	16	PAL_BG	NTSC	32	PAL_I	Invalid	48	PAL_DK	Invalid	64	SEC_L	Invalid	80	SEC_LS	Invalid	96	SEC_BG	Invalid	112	SEC_DK	Invalid
Video standard id	Europe	NAFTA																								
16	PAL_BG	NTSC																								
32	PAL_I	Invalid																								
48	PAL_DK	Invalid																								
64	SEC_L	Invalid																								
80	SEC_LS	Invalid																								
96	SEC_BG	Invalid																								
112	SEC_DK	Invalid																								
Example	DS:> 1114 3456 16 111400: Test OK @																									

Nucleus Name	DS_ANAB_IICWriteRead
Nucleus Number	1115
Description	Perform an IIC write and read action on the analogue board
User Input	Writing: [<W> <w>] [I2C address] [number of data bytes to write] with <data[0]...data[n]> Max 16 data bytes (n < 16). Reading: [<R> <r>] [I2C address] [number of data bytes to read] Max 16 data bytes (n < 16).
Example	DS:> 1115 w 0x94 2 0x06 0x02 111500: Test OK @

Nucleus Name	DS_ANAB_ClockAdjust
Nucleus Number	1116
Description	Set the clock to the value passed through in the YYYY MM DD HH MM SS format
User Input	<YYYY> <MM> <DD> <HH> <MM> <SS>
Example	DS:> 1116 2002 11 11 11 11 111600: Test OK @

Nucleus Name	DS_ANAB_ClockReference
Nucleus Number	1117
Description	Generate a 1 kHz signal on pin 7 (INT) of the clock IC
User Input	None
Example	DS:> 1117 111700: Test OK @

Nucleus Name	DS_ANAB_ClockCorrection
Nucleus Number	1118

Description	Store the clock IC correction value in NVRAM
User Input	The correction value for the clock
Example	DS:> 1118 1000023 111800: Test OK @

Nucleus Name	DS_ANAB_TunerAFCReferenceVoltage
Nucleus Number	1119
Description	Store the reference voltage for the tuner in NVRAM
User Input	The reference voltage, between 0 and 255
Example	DS:> 1119 5 111900: Test OK @

Nucleus Name	DS_ANAB_TunerFrequencyDownload
Nucleus Number	1120
Description	Store the frequency table in NVRAM. The frequency table is passed through the error-string provided to the nucleus.
User Input	See frequency table
Example	DS:> 1120 2233 00 02 4E45442031 112000: Test OK @

Frequency download string format

Format	description	remarks
X(XXX)	Preset number	
VVWW	VV: Channel number WW : Channel offset	
ZZ	Byte containing 8 bit fields for TRUE/FALSE : BIT 0: Decoder BIT 1: Modulation BIT 2: NICAM SAP BIT 3: Satpreset BIT 4: Presetdefined Channelpreferred BIT 5: ExtPreset BIT 6: NameManuallyChanged BIT 7: ChannelPreset	NICAM/stereo bit for Europe SAP/stereo bit for NAFTA Preset defined bit is only used for Europe. For NAFTA, it is renamed as channelpreferred to indicate if a channel is preferred or not. TRUE if preset is defined from P50 as extern [TGA]
HH	HfSystemFineTuning	HfS: 4 bit, FT: -4,...,4
IJJKLLMM	Netname	Range: A,...,Z,0,...,9,... Netname length exists for Europe only. 'II' is the HEX-value for the first character, 'JJ' for the second, Ö

The message string of (DS_MessageDef *msgString) should be in the format:

"X(XXX)_VVWW_ZZ_HH_IJJKLLMM".

Here will be 'X(XXX)' a decimal value in the range of 0 to 255.

V, W, Z, H, I, J, K, L, M are hex values with out the prefix '0x' (in the range 0... 9,A ... F)

"_" Denotes a space character.

Remarks:

CHANNEL_SYSTEM is for NAFTA.

PRESET_SYSTEM is for Europe.

Nucleus Name	DS_ANAB_StoreExternalPresets
Nucleus Number	1121
Description	Store the external presets in NVRAM
User Input	None
Example	DS:> 1121 112100: Test OK @

Nucleus Name	DS_ANAB_BargraphLevelAdjust
Nucleus Number	1122
Description	Measure the audio signal corresponding to 0dB per channel and store it as correction value in NVRAM

User Input	none
Example	DS:> 1122 112200: Test OK @

System (SYS)

Nucleus Name	DS_SYS_HardwareVersionGet
Nucleus Number	1200
Description	Get the hardware version and type of the digital board
User Input	None
Example	DS:> 1200 120000: Hardware ID = 00 The (PIO-pins) Digital Board ID = 2 Test OK @ DS:>

Nucleus Name	DS_SYS_SoftwareVersionBootGet
Nucleus Number	1201
Description	Get the version of the boot software on the digital board
User Input	None
Example	DS:> 1201 120100: Software Boot Version = 0001 Test OK @

Nucleus Name	DS_SYS_SoftwareVersionDownloadGet
Nucleus Number	1202
Description	Get the version of the download software on the digital board
User Input	None
Example	DS:> 1202 120200: Software Download Version = 0001 Test OK @

Nucleus Name	DS_SYS_SoftwareVersionApplGet
Nucleus Number	1203
Description	Get the version of the application software on the digital board
User Input	None
Example	DS:> 1203 120300: Software Application Version = 0001 Test OK @

Nucleus Name	DS_SYS_SoftwareVersionDiagnosticsGet	
Nucleus Number	1204	
Description	Get the version of the diagnostics software on the digital board	
User Input	None	
Example	DS:> 1204 120400: Software Diagnostics Version = 0001 Test OK @	
	120503	Something went wrong while transferring the data.
	120504	User cancelled the upload.
Example	DS:> 1205 1 120500: Test OK @	

Nucleus Name	DS_SYS_EepromUpload
Nucleus Number	1205
Description	Upload the contents of the NVRAM on the analogue board or the digital board to the service PC, by using the X-modem protocol
User Input	Choose one of the following parameters for the nucleus: 1. Upload the contents of the NVRAM of the digital board 2. Upload the contents of the NVRAM of the analogue board Choose in the terminal on the control PC -> transfer -> receive file. Select X-modem protocol. Then click receive in the dialogue and fill in the file name in which you want to store the data.

Nucleus Name	DS_SYS_EepromDownload
Nucleus Number	1206
Description	Download a file with the contents of the NVRAM for the analogue board or the digital board from the service PC to the recorder, by using the X-modem protocol
User Input	Choose one of the following parameters for the nucleus: 1. Download the contents of the NVRAM of the digital board 2. Download the contents of the NVRAM of the analogue board Choose in the terminal of the control PC -> transfer -> send file. Select X-modem protocol. Then choose a file with the Browse button in the dialogue and click on send.
Example	DS:> 1206 1 120600: Test OK @

Nucleus Name	DS_SYS_DvldNumberGet
Nucleus Number	1208
Description	Get the IEEE1394 ID
User Input	None
Example	DS:> 1208 120800: The DvldNumber is: 0x0C22384E5A Test OK @

Nucleus Name	DS_SYS_licWrite
Nucleus Number	1209
Description	Perform an IIC write action on the digital board
User Input	The user input the number of bytes to write followed by these bytes: <BusID><Slave address to write to><number of bytes to write><d1><d2><..><dx> Where the bus ID is either 0 (normally used) or 1
Example	DS:> 1209 0 0xa0 1 0x6 120900: 1 Bytes written Test OK @

Nucleus Name	DS_SYS_licRead
Nucleus Number	1210
Description	Perform an IIC read action on the digital board
User Input	The user inputs the number of bytes to read and the address to read them from: <BusID><Slave address to read from><Number of bytes to read> Where the bus ID is either 0 (normally used) or 1
Example	DS:> 1210 0 0xa0 1 121000: Value read =0x06 Test OK @

Nucleus Name	DS_SYS_UartWrite
Nucleus Number	1211
Description	Perform an UART write action on the digital board on a specified UART
User Input	The user inputs the UART to write to, the number of bytes and the bytes to be written to the UART. 1=UART port 1 : not used 2=UART port 2 : Bit Engine 3=UART port 3 : Analogue board <UartNr><Number of bytes to write><d1><d2><..><dx>
Example	DS:> 1211 2 2 0xd1 0x01 121100: Test OK @

Nucleus Name	DS_SYS_UartRead
Nucleus Number	1212
Description	Perform an UART read action on the digital board on a specified UART
User Input	The user inputs the UART to read from. 1=UART port 1 : not used 2=UART port 2 : Bit Engine 3=UART port 3 : Analogue board <UartNr >
Example	DS:> 1212 2 121200: The value that was read is: 0x50 0xD1 0x00 Test OK @

Nucleus Name	DS_SYS_VideoLoopThroughStart
Nucleus Number	1213
Description	The video signal, which is confirm the user input, is routed from the input to the output. Input is set with the routing nucleus 1112. All outputs are enabled.
User Input	<vipInput> <VideoOutput> <VideoStandard> 1. vipInput (CVBS, YC, YUV, RGB). 2. VideoOutput (YUV, RGB). 3. VideoStandard (PAL, NTSC).
Example	DS:> 1213 CVBS RGB PAL 121300: Test OK @

Nucleus Name	DS_SYS_VideoLoopThroughStop
Nucleus Number	1214
Description	Stop routing the video input to all the outputs.
User Input	-
Example	DS:> 1214 121400: Test OK @

Nucleus Name	DS_SYS_VideoLoop
Nucleus Number	1215
Description	Note: Before executing this nucleus the user must route the video signal on the analog board with nucleus DS_ANAB_VideoRouting(1112).
User Input	Video input of the digital board: - CVBS - YC - YUV - RGB - TEST (The video output will be routed to the video input on the digital board.) Video standard: - PAL - NTSC When no input is given, the nucleus will take TEST for video input and PAL for video standard.
Example	DS:> 1215 cvbs ntsc 121500: Test OK @ DS:> 1215 cvbs pal 121508: The VideoInputProcessor cannot detect a sync-signal. Error @ DS:> 1215 yuv ntsc 121511: Error in luminance signal(Y) Error in chrominance signal(U) Error in chrominance signal(V) Error @

Nucleus Name	DS_SYS_SlashVersionSet
Nucleus Number	1217
Description	Set the slash version of the system
User Input	The slash version
Example	DS:> 1217 82 121700: Test OK @

Nucleus Name	DS_SYS_SlashVersionGet
Nucleus Number	1218
Description	Get the slash version of the system
User Input	None
Example	DS:> 1218 121800: The slash version is: 82 Test OK @

Nucleus Name	DS_SYS_Virginize
Nucleus Number	1219

Description	(Re-) Virginize the recorder. User data in the NVRAM of the analogue board is cleared
Example	DS:> 1219 121900: Test OK @

Nucleus Name	DS_SYS_VirginModeOn
Nucleus Number	1220
Description	Turn on the virgin mode functionality (e.g. the auto channel search upon start-up)
User Input	None
Example	DS:> 1220 122000: Test OK @

Nucleus Name	DS_SYS_VirginModeOff
Nucleus Number	1221
Description	Turn off the virgin mode functionality (e.g. the auto channel search upon start-up)
User Input	None
Example	DS:> 1221 122100: Test OK @

Nucleus Name	DS_SYS_DisplayFatalOn
Nucleus Number	1223
Description	Turn on the display-fatal functionality which displays debug-information on the display when encountering a fatal error condition from which could not be recovered automatically
User Input	None
Example	DS:> 1223 122300: Test OK @

Nucleus Name	DS_SYS_DisplayFatalOff
Nucleus Number	1224
Description	Turn off the display-fatal functionality which displays debug-information on the display when encountering a fatal error condition from which could not be recovered automatically
User Input	None
Example	DS:> 1224 122400: Test OK @

Nucleus Name	DS_SYS_DisplayFatalGet
Nucleus Number	1225
Description	Get the display-fatal flag of the recorder
User Input	None
Example	DS:> 1225 122500: Test OK @

Nucleus Name	DS_SYS_SettingsSet
Nucleus Number	1226
Description	Programs the digital board settings into the boot EEPROM on the digital board.
User Input	A large hexadecimal value that represents the digital board settings obtained from the DbString.exe program or from a reference set.
Example	DS:> 1226 6469616774737462010102000101010101000020080000 122600: Test OK @

Nucleus Name	DS_SYS_SettingsDisplay
Nucleus Number	1228
Description	Show the settings that are programmed in the BROM on the digital board.
User Input	None.

Example	DS:> 1228 Settings ID: 6D7920626F61726400020300010101020101000020080000 Board name: my board Hardware ID: 0 Codec IC: PNX7100_MF2 Video Input Processor IC: SAA7118 Progressive Scan Deinterlacer IC: None Progressive Scan Denc IC: ADV7196 I-Link physical layer circuit IC: PDI1394P25 I-Link link layer circuit IC: PDI1394P40 Audio clock: Clock scheme 1 Bit engine connector: available IDE connector 1: available IDE connector 2: not available PCI connector: not available RAM size 32MByte ROM size (NOR FLASH bank 1) 8MByte ROM size (NOR FLASH bank 2) Not available ROM size (NAND FLASH) Not available Bit Engine: AV 2.0 122800: Test OK @
---------	---

Nucleus Name	DS_SYS_SettingsGet
Nucleus Number	1229
Description	Get the digital board diversity settings string that is programmed in the BROM on the digital board.
User Input	None.
Example	DS:> 1229 122900: 6D7920626F61726400020300010101020101000020080000 Test OK @

Nucleus Name	DS_SYS_AudioLoopThroughStart
Nucleus Number	1230
Description	Description: The audio input is routed from the an input to all outputs. Input is set with the routing nucleus 1113. All outputs are enabled.
User Input	None.
Example	DS:> 1230 123000: Test OK @

Nucleus Name	DS_SYS_AudioLoopThroughStop
Nucleus Number	1231
Description	Stop routing the audio input to all the outputs
User Input	-
Example	DS:> 1231 123100: Test OK @

Electronic Program Guide Board (EPGB)

Nucleus Name	DS_EPGB_VersionGet
Nucleus Number	1300
Description	Returns the version of the EPG board.
User Input	None
Example	DS:> 1300 130000: Version : 6.1.9 Test OK @

PCMCIA INTERFACE (PCMCIA)

Nucleus Name	DS_PCPCIA_Reset
Nucleus Number	1400
Description	Reset the PCMCIA device by sending a reset command through IDE
Example	DS:> 1400 140000: Test OK @

Nucleus Name	DS_PCMCIA_Inquiry
Nucleus Number	1401
Description	Get the vendor- and product identification and the product revision level of the media in the slot.
Example	DS:> 1401 140100: Test OK @

Nucleus Name	DS_PCMCIA_WriteRead
Nucleus Number	1402
Description	Perform a Write Read test to a random sector on the inserted medium in the PCMCIA device and check if the data read is equal to the data written.
Example	DS:> 1402 140200: Test OK @

Nucleus Name	DS_PCMCIA_Diagnostics
Nucleus Number	1403
Description	Shall perform the internal diagnostic tests implemented by the media in the slot.
Example	DS:> 1403 140300: Test OK @

Script

Nucleus Name	DS_IH_ScriptHandler
Nucleus Number	Script
Description	
Included tests:	<ol style="list-style-type: none"> 1. DS_ANAB_COMMUNICATIONECHO_NUC 2. DS_DCB_COMMUNICATIONECHO_NUC 3. DS_BROM_COMMUNICATION_NUC 4. DS_SYS_SETTINGSDISPLAY_NUC 5. DS_CHR_DEVTYPEGET_NUC 6. DS_CHR_INT_PIC_NUC 7. DS_CHR_DMA_NUC 8. DS_BROM_WRITEREAD_NUC 9. DS_NVRAM_COMMUNICATION_NUC 10. DS_NVRAM_WRITEREAD_NUC 11. DS_SDRAM_WRITEREADFAST_NUC 12. DS_FLASH_WRITEREAD_NUC 13. DS_FLASH_CHECKSUMPROGRAM_NUC 14. DS_SYS_HARDWAREVERSIONGET_NUC 15. DS_VIP_DEVTYPEGET_NUC 16. DS_VIP_COMMUNICATION_NUC 17. DS_DVIO_LINKDEVTYPEGET_NUC 18. DS_DVIO_PHYDEVTYPEGET_NUC 19. DS_DVIO_LINKCOMMUNICATION_NUC 20. DS_DVIO_PHYCOMMUNICATION_NUC 21. DS_PSCAN_COMMUNICATIONDENC_NUC 22. DS_PSCAN_COMMUNICATIONDEINTERLACER_NUC 23. DS_BE_COMMUNICATIONECHO_NUC 24. DS_ANAB_COMMUNICATIONIICNVRAM_NUC 25. DS_ANAB_COMMUNICATIONIICTUNER_NUC 26. DS_ANAB_COMMUNICATIONIICSOUNDPROCESSOR_NUC 27. DS_ANAB_COMMUNICATIONIICAVSELECTOR_NUC 28. DS_ANAB_CHECKSUMPROGRAM_NUC
User Input	None

Example	<pre> DS:> script Executing User/Dealer script. Busy executing NUC1100 1-28 Hello Analogue Board Busy executing NUC1000 2-28 Busy executing NUC200 3-28 Busy executing NUC1228 4-28 Settings ID: 4C4541440D00000000030300010101020101000020080000 Board name: LEAD Hardware ID: 0 Codec IC: PNX7100_MF3 Video Input Processor IC: SAA7118 Progressive Scan Deinterlacer IC: None Progressive Scan Denc IC: ADV7196 I-Link physical layer circuit IC: PDI1394P25 I-Link link layer circuit IC: PDI1394P40 Audio clock: Clock scheme 1 Bit engine connector: available IDE connector 1: available IDE connector 2: not available PCI connector: not available RAM size 32MByte ROM size (NOR FLASH bank 1) 8MByte ROM size (NOR FLASH bank 2) Not available ROM size (NAND FLASH) Not available Bit Engine: AV 2.0 Busy executing NUC100 5-28 Device ID 7100 Codec ID PNX7100_MF3 F-BCU (0x0102) 1.0 INTC (0x011d) 1.0 PCI-XIO(0x0113) 1.0 SIF (0x013b) 1.0 EJTAG (0x0104) 0.0 S-BCU (0x0102) 1.0 BOOT (0x010a) 1.0 CONFIG (0x013f) 1.0 RESET (0x0123) 1.0 DEBUG (0x0116) 0.0 UART0 (0x0107) 0.1 UART1 (0x0107) 0.1 UART2 (0x0107) 0.1 UART3 (0x0107) 0.1 I2C0 (0x0105) 0.1 I2C1 (0x0105) 0.1 GPIO (0x013c) 1.0 SYNC (0x013a) 1.0 DISP0 (0xa015) 0.2 DISP1 (0xa00f) 0.0 OSD (0x0136) 0.1 SPU (0xa00e) 0.0 MIXER (0x0137) 1.0 DENC (0x0138) 0.1 CCIR (0x0139) 1.0 VDEC (0x0133) 0.1 PARSER (0xa00d) 0.0 DV (0xa00c) 0.0 BEI (0xa00a) 0.0 IDE (0xa009) 0.0 SGDX (0xa008) 0.0 BYTE (0xa00b) 0.0 OUTPUT (0xa003) 0.0 ACOMP (0xa000) 0.0 VFE (0xa001) 0.0 VCOMP (0xa002) 0.0 SCR (0x0000) 0.0 SIFF (0xa011) 0.0 WMD (0xa010) 0.0 AUDIO0 (0xa015) 0.2 AUDIO1 (0xa00f) 0.0 PSCAN (0xa018) 0.0 Busy executing NUC114 6-28 Busy executing NUC115 7-28 Busy executing NUC201 8-28 Busy executing NUC300 9-28 Busy executing NUC301 10-28 Busy executing NUC401 11-28 Busy executing NUC501 12-28 Busy executing NUC503 13-28 BootCode checksum is: 0xBABEB432, which is correct Diagnostics checksum is: 0xBABED22B, which is correct Download checksum is: 0xBABE025F, which is correct Application checksum is: 0xBABE2825, which is correct Busy executing NUC1200 14-28 Hardware ID = 00 Busy executing NUC600 15-28 Found SAA7118 </pre>
---------	--

Example	Busy executing NUC601 16-28 Busy executing NUC700 17-28 Device type of the link layer IC: ffc00301 Busy executing NUC701 18-28 Device type of the phy layer IC: 0 Busy executing NUC702 19-28 Busy executing NUC703 20-28 Busy executing NUC801 21-28 Busy executing NUC808 22-28 The IIC acknowledge was not received, which is correct Busy executing NUC900 23-28 Busy executing NUC1101 24-28 Busy executing NUC1102 25-28 Busy executing NUC1104 26-28 Busy executing NUC1105 27-28 Busy executing NUC1111 28-28 BootCode checksum is: 0xBABE6240, which is correct Diagnostics checksum is: 0xBABEDC9A, which is correct Download checksum is: 0xBABEA6B7, which is correct Application checksum is: 0xBABE5968, which is correct PASS DS:>
---------	--

5.3.4 Menu Mode Interface Digital Board 1.5, Empress

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```

DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?   [M] : @ M ↵

Main Menu

1.  Digital Board           ->
2.  Analogue Board         ->
3.  Front Panel            ->
4.  Basic Engine           ->
5.  DVIO                   ->
6.  Progressive Scan Board ->
7.  Loop tests             ->
8.  Log                    ->
9.  Scripts                ->

Select>

```

Figure 5-12

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

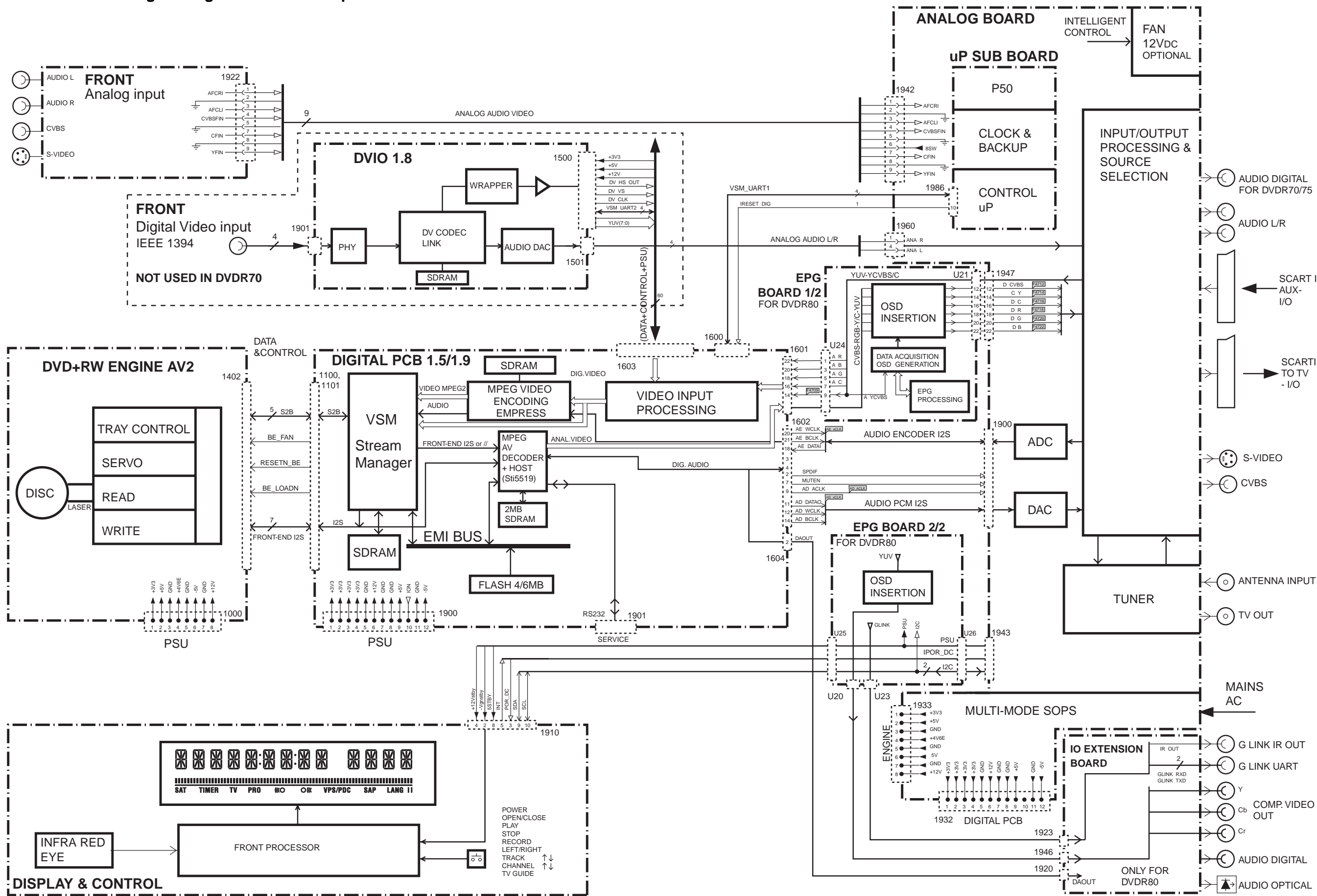
5.4 Nuclei Error Codes

DVIO 1.8 Error Codes

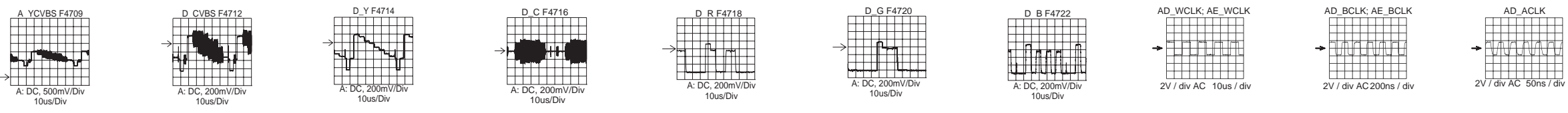
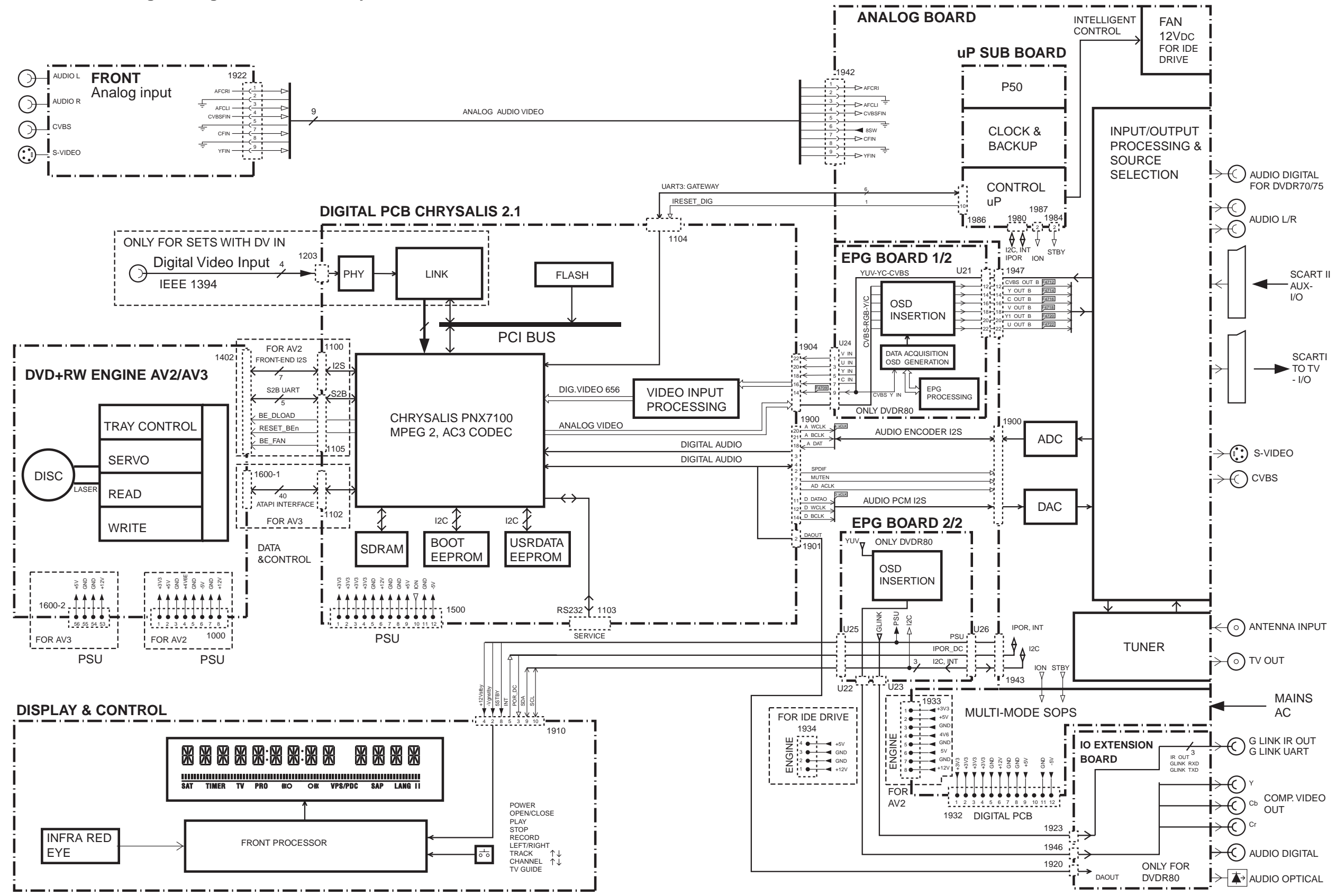
Error Code	Id	Description	Hardware	
0	0x00	DVIOC_ERR_DDS_OK	No Error	
6	0x06	DVIOC_ERR_DDS_UNKNOWN	Unknown Error(including UART communication error)	
17	0x11	DVIOC_ERR_DDS_TNF_1	Link chip incorrect responding	μPD72893, Link
18	0x12	DVIOC_ERR_DDS_TNF_2	No link register access or link reset failed	μPD72893, Link
23	0x17	DVIOC_ERR_DDS_TNF_7	Link reset failed	μPD72893, Link
38	0x26	DVIOC_ERR_DDS_TNF_16	Expecting no 1394 node with GUID connectivity, while detecting connection	
39	0x27	DVIOC_ERR_DDS_TNF_17	Expecting 1394 node with GUID connectivity, while not detecting connection	
48	0x30	DVIOC_ERR_DDS_UPINTRAM A	Internal ram problem in address lines	μPD78F0988, Wrapper
50	0x32	DVIOC_ERR_DDS_UPEXTRA MA	External ram problem in address lines	μPD4564163G5, SDRAM
51	0x33	DVIOC_ERR_DDS_UPEXTRA MD	External ram problem in data lines	μPD4564163G5, SDRAM
58	0x3A	DVIOC_ERR_DDS_ROMCHK	Checksum of codespace 0x0000-0x1f80, 0x2000-0xeffd is not correct	μPD78F0988, Wrapper
244	0xF4	DVIOC_ERR_LINK_HWPHY	PHY chip not responding(PHY down report received)	μPD72852, Phy
245	0xF5	DVIOC_ERR_LINK_HWLINK	LINK chip not responding	μPD72893, Link

6. Block Diagrams, Waveforms, Wiring Diagram.

Overall Block Diagram Digital Board 1.5 Empress

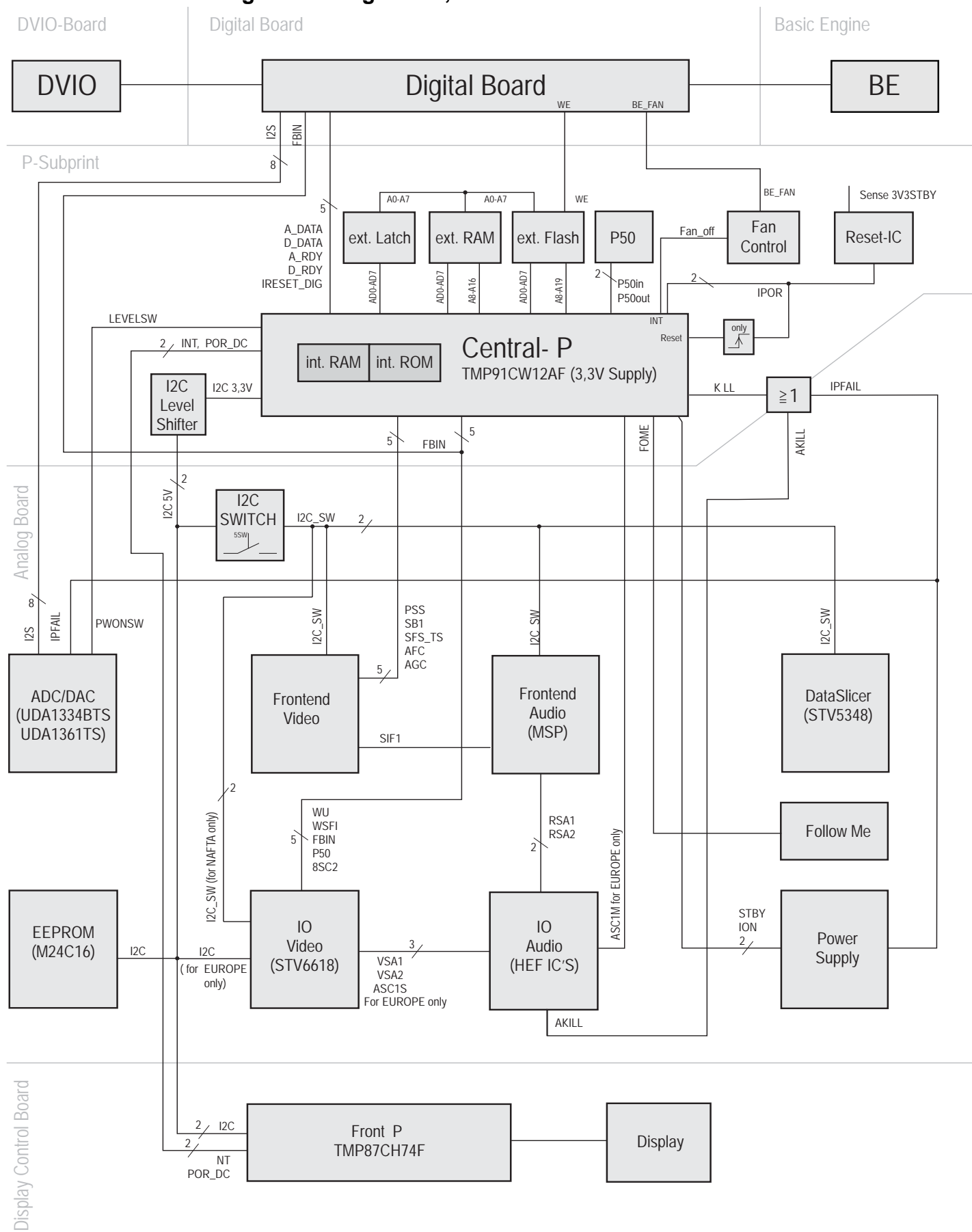


Overall Block Diagram Digital Board 2.1 Chrysalis

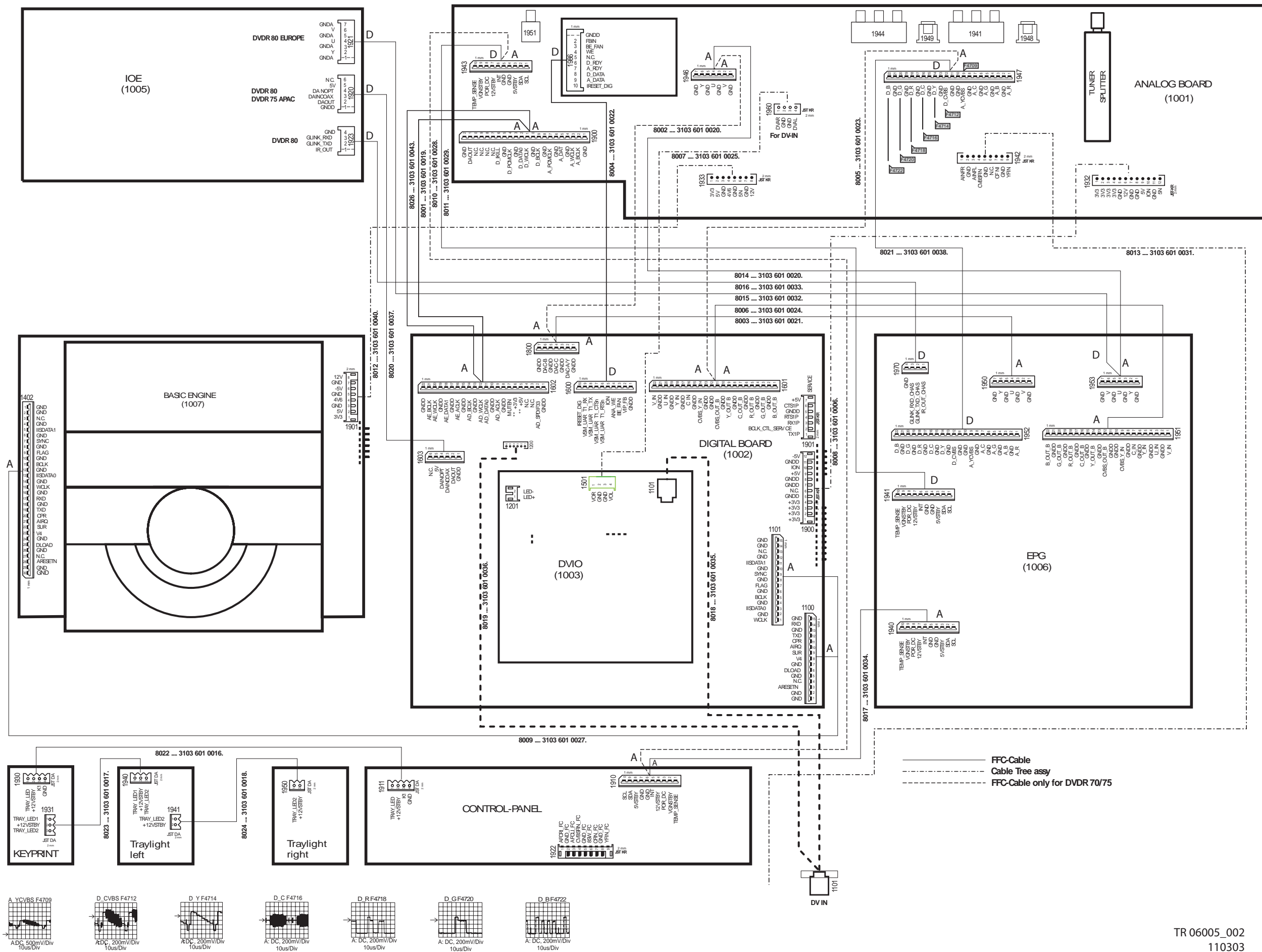


TR 10002_001
050503

Control Block Diagram Analog Board, uP Board



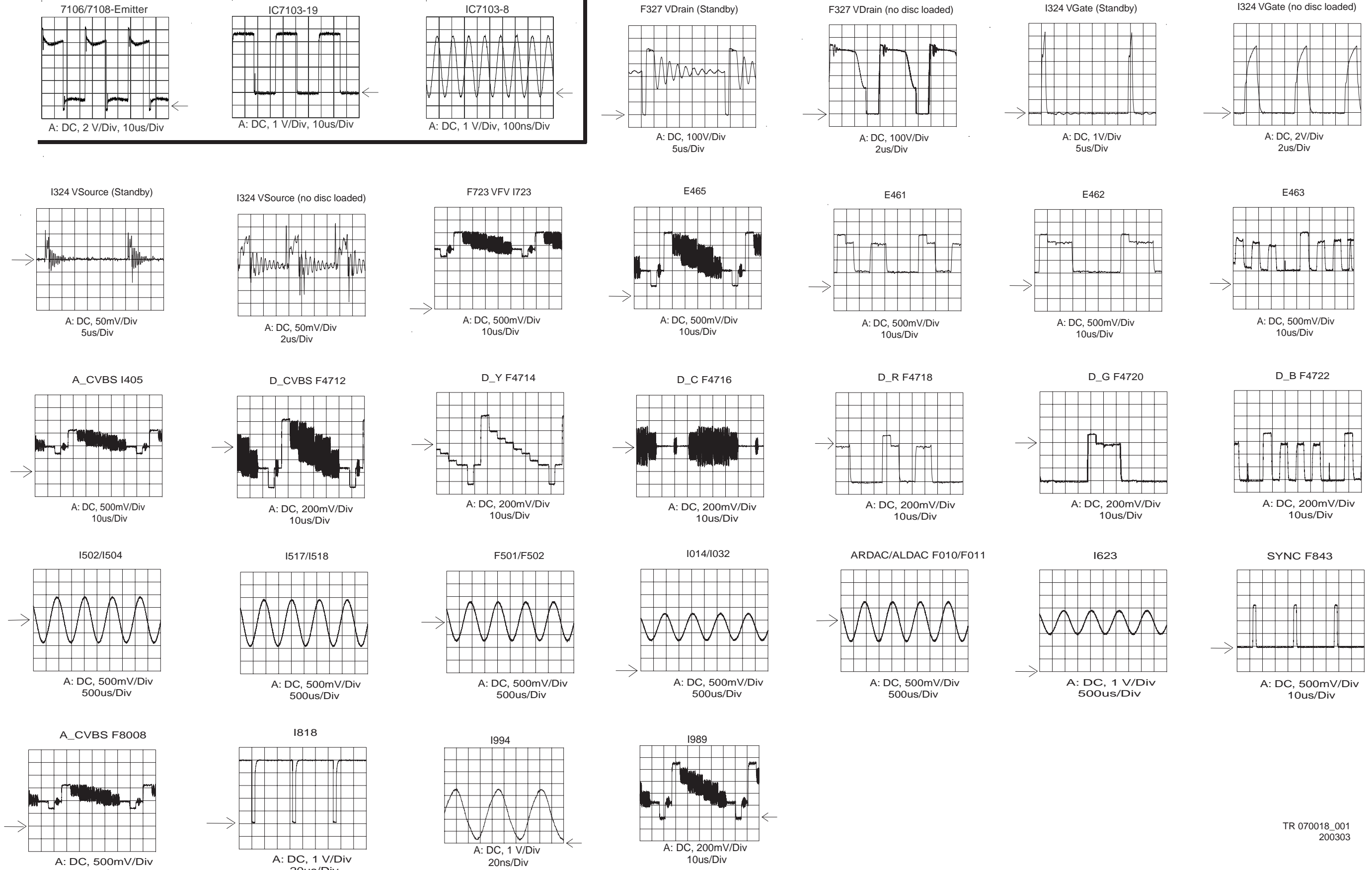
Wiring Diagram



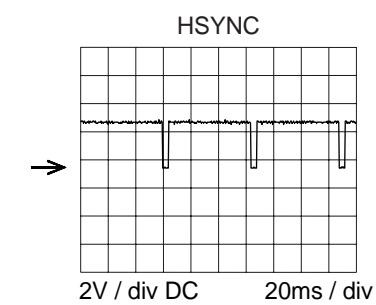
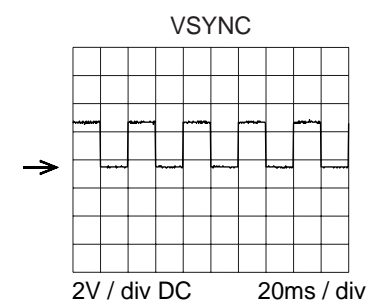
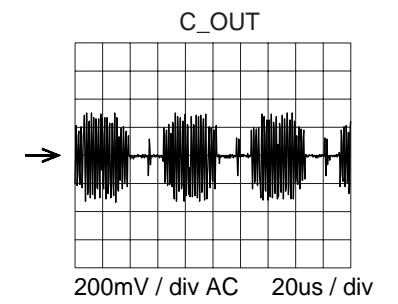
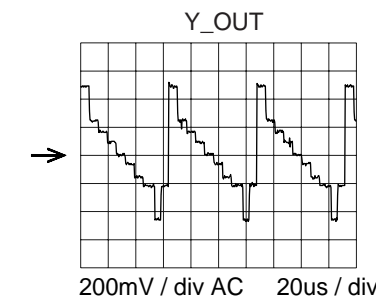
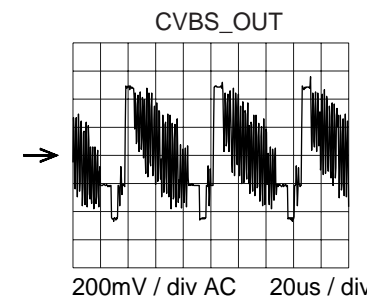
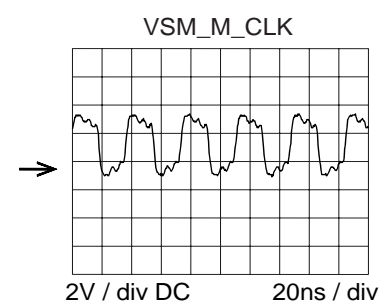
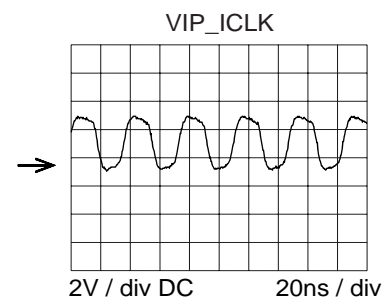
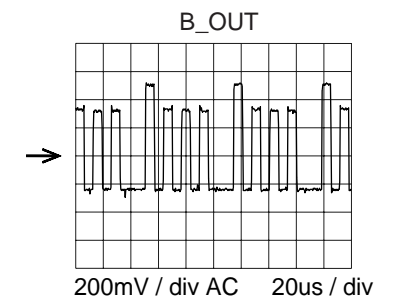
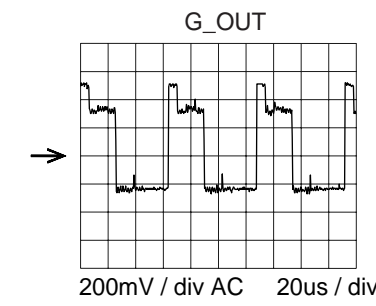
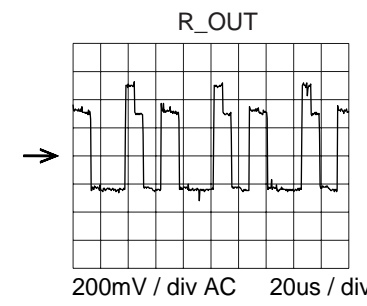
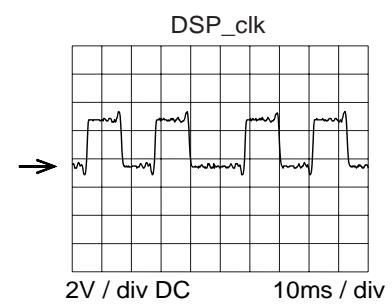
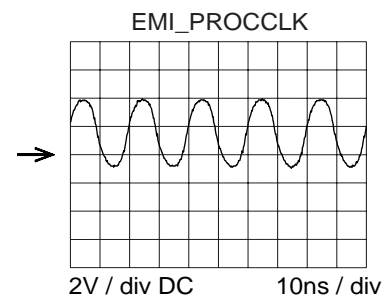
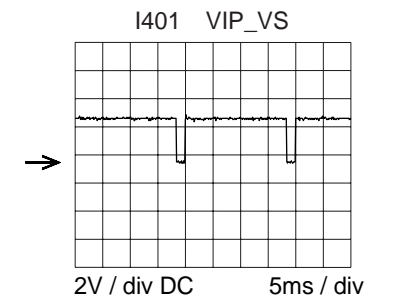
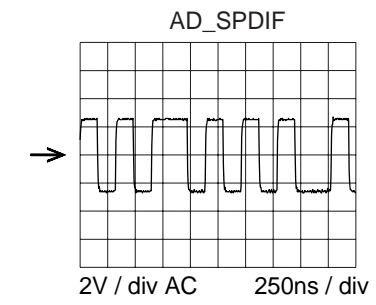
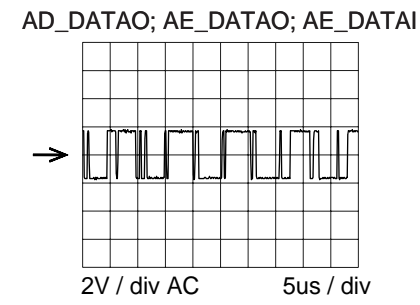
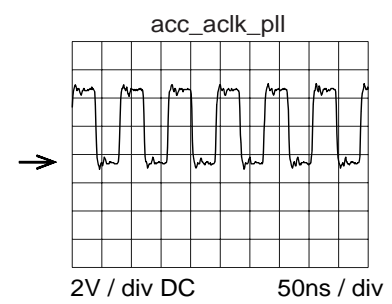
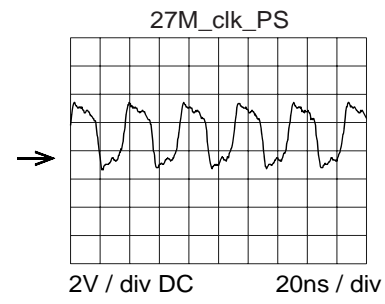
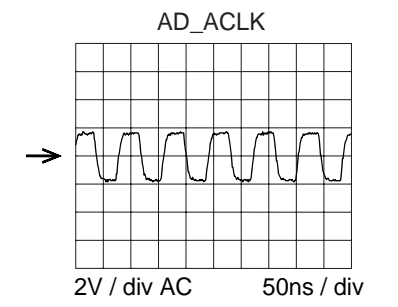
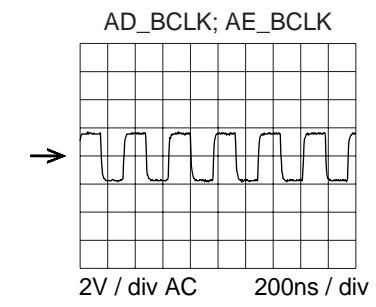
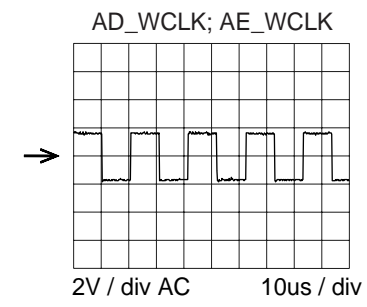
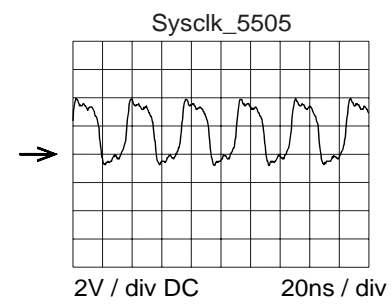
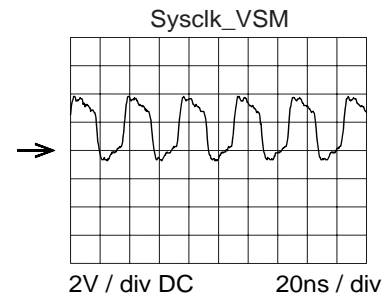
Waveforms

Waveforms Analog Board

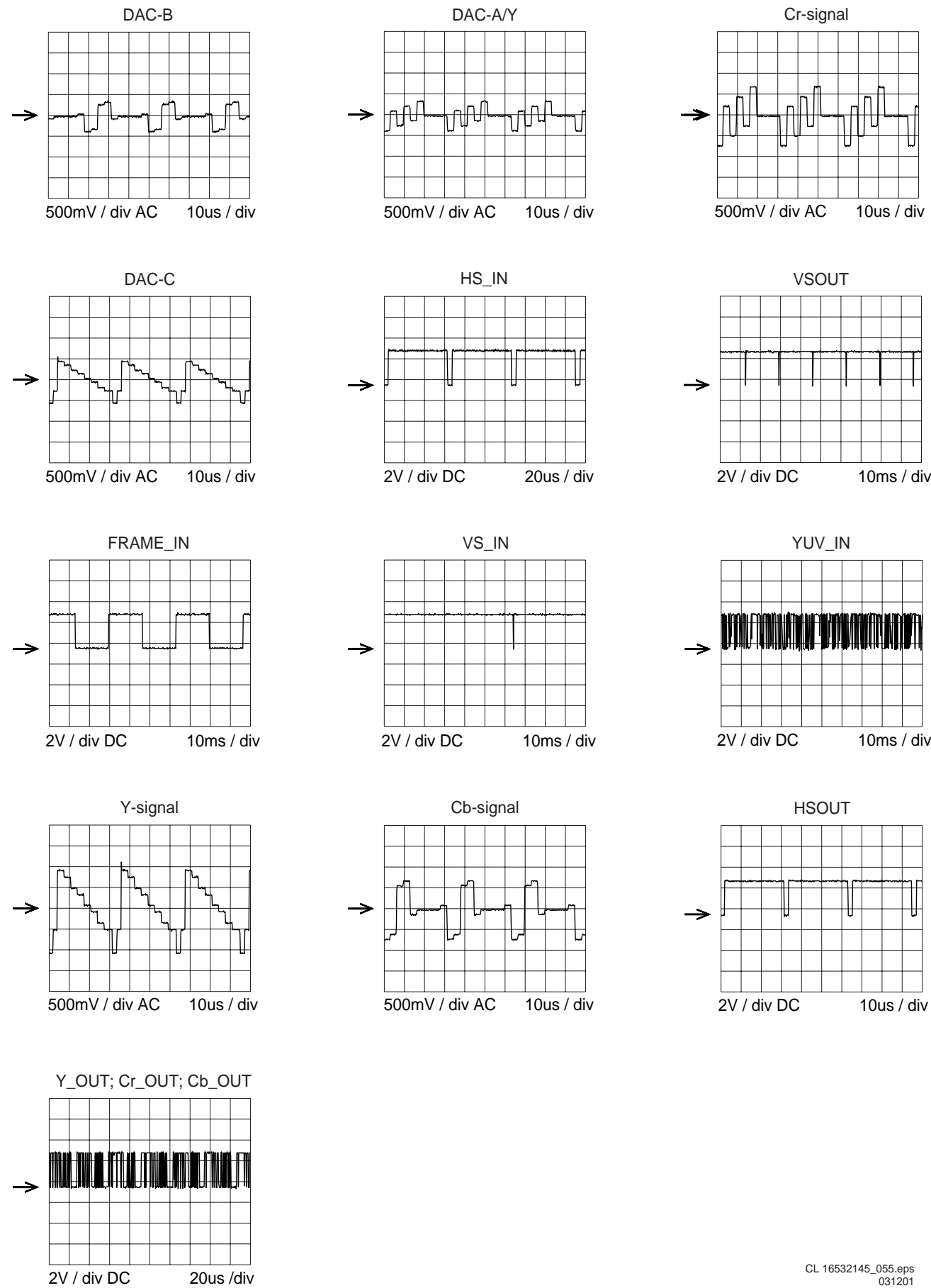
Waveforms Display Board



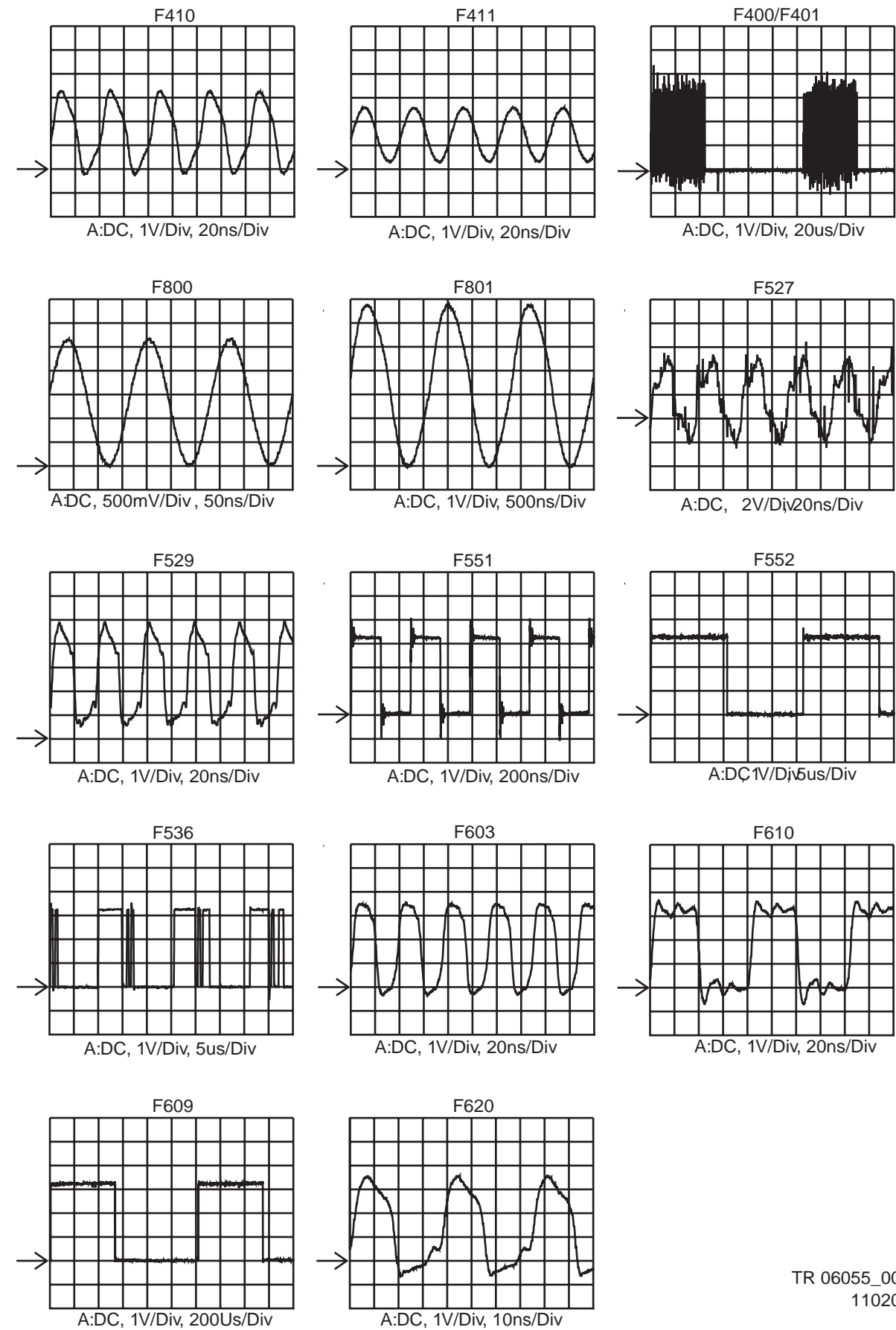
Waveforms Digital Board 1.5



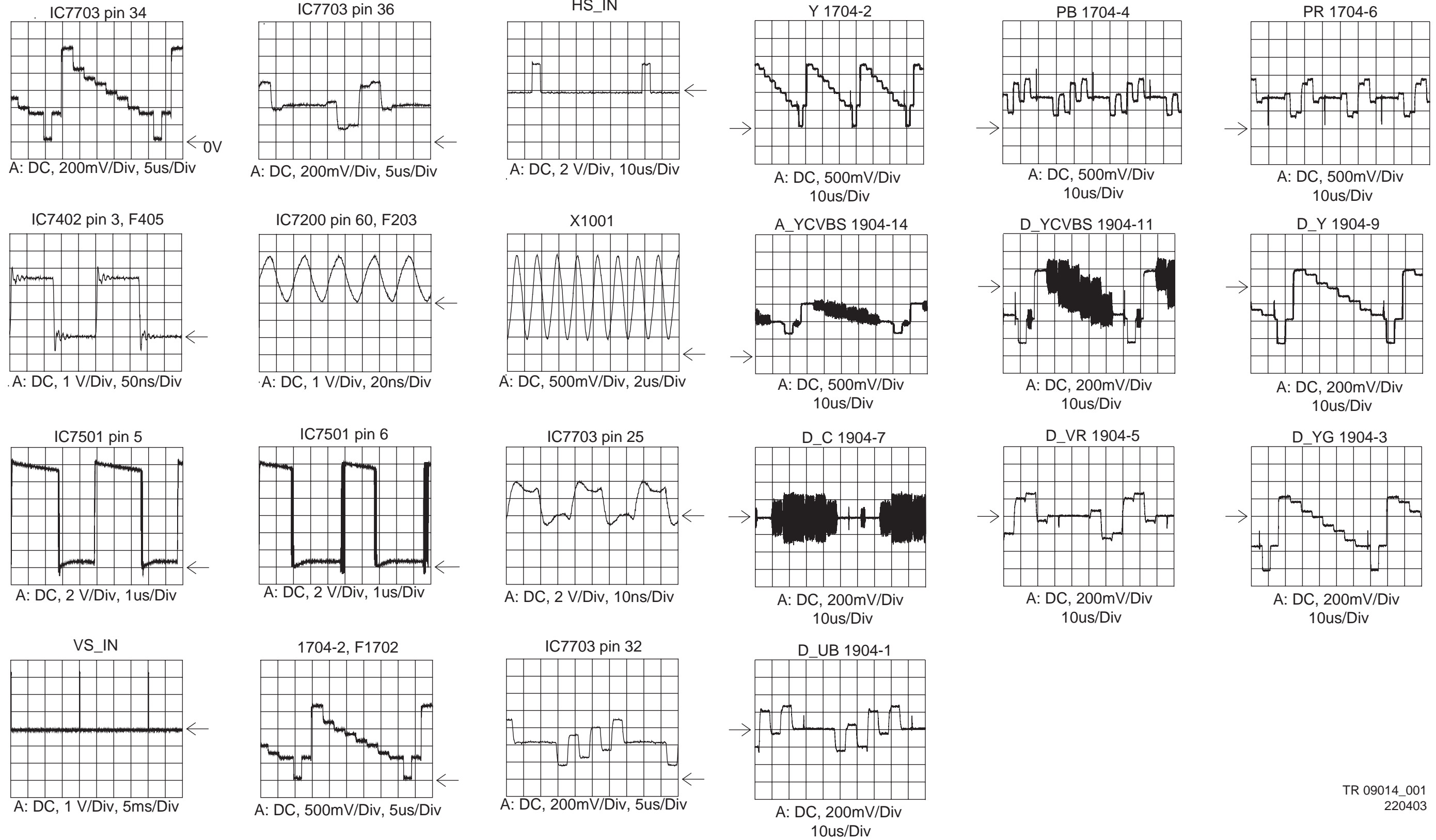
Waveforms Digital Board 1.5



Waveforms DVIO

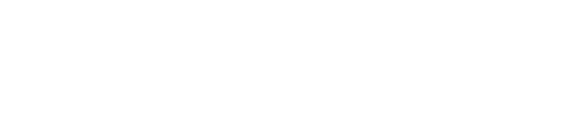
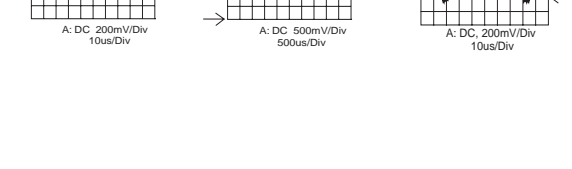
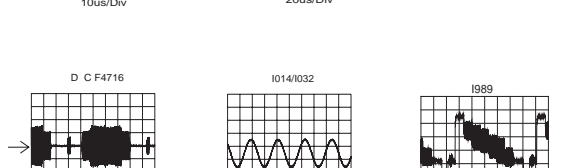
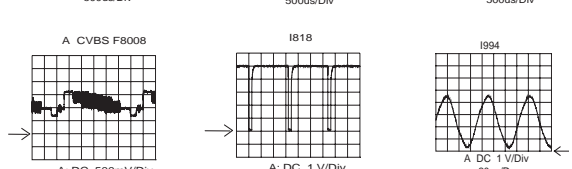
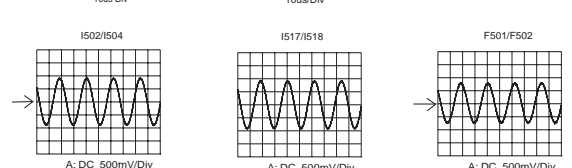
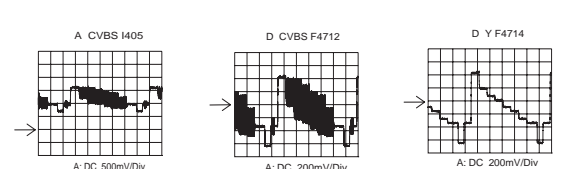
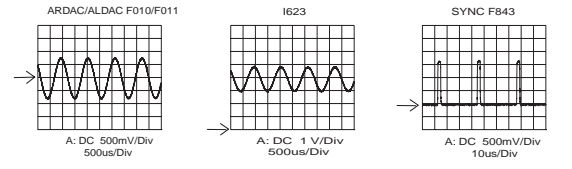
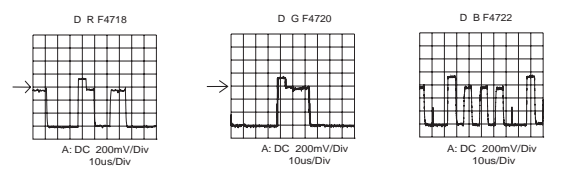


Waveforms Digital Board Chrysalis 2.1

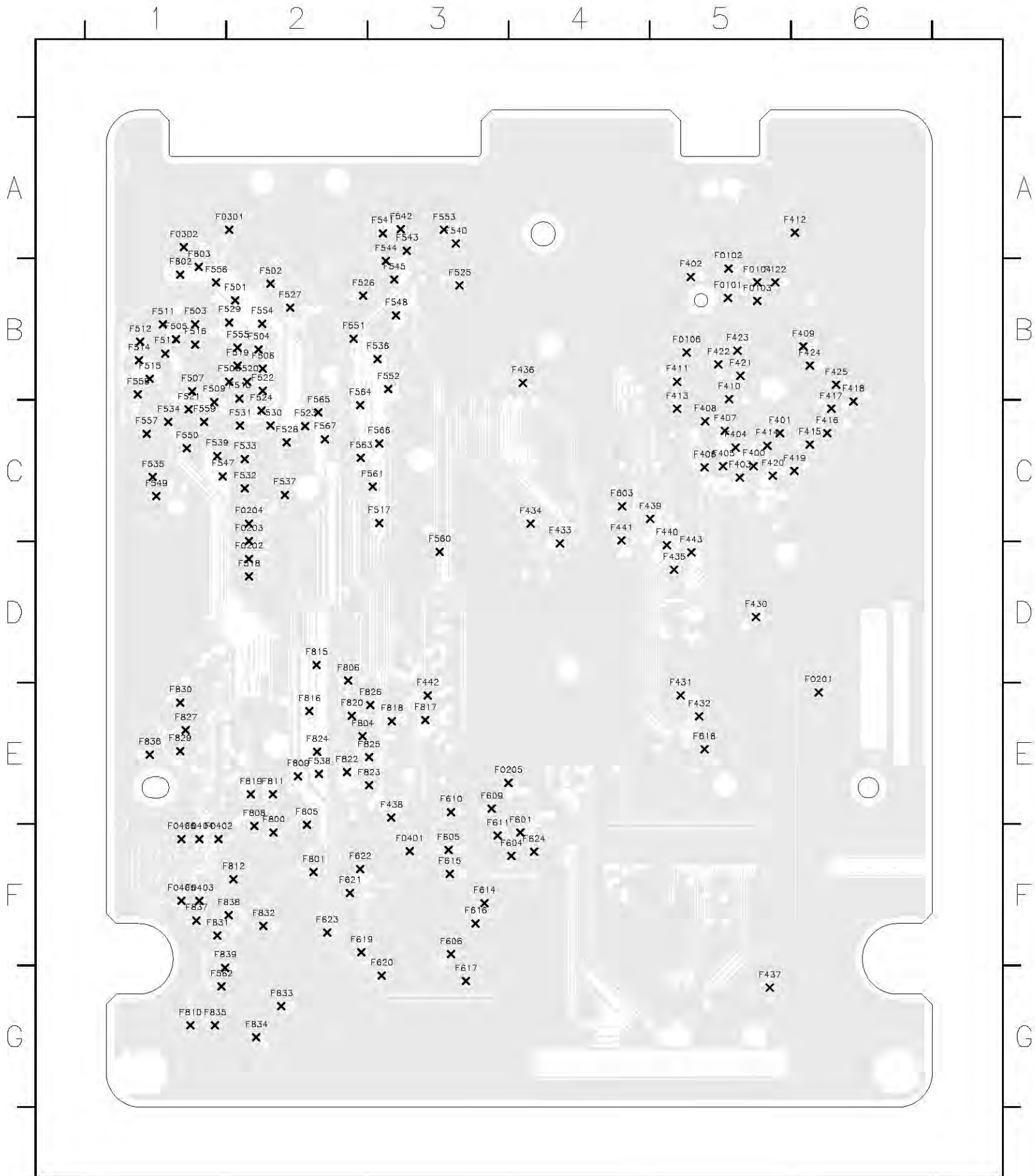


Test points overview Analog Board

F0001 A10	F301 A3	F321 C3	F343 A2	F363 A2	F4205 C6	F5102 A5	F5216 C8	I004 C10	I036 A9	I319 C3	I339 A2	I361 A2	I429 A9	I454 A9	I481 B6	I507 A9	I611 B7	I528 B7	I707 B4	I732 A3	I956 B9
F0002 C10	F302 A4	F322 C4	F344 C9	F364 A3	F4207 C6	F5103 A5	F5219 A4	I005 B10	I037 A1	I320 C3	I340 C1	I402 A6	I431 A7	I456 B6	I482 B6	I508 A7	I612 B7	I529 A8	I708 B4	I733 A3	I957 B9
F0003 C10	F304 B1	F323 B1	F346 A2	F366 B2	F4209 C6	F5106 A5	F5220 A4	I006 B9	I030 A3	I321 B1	I341 A5	I405 A10	I433 A7	I457 B5	I483 B5	I509 A8	I613 C7	I530 A8	I709 B4	I734 A3	I958 B9
F0005 C10	F305 B2	F324 B3	F347 C8	F367 B2	F4210 B5	F5108 A5	F5221 C6	I007 B10	I033 B2	I322 B1	I342 A2	I406 A4	I434 A7	I459 A5	I484 A5	I510 A8	I614 B7	I531 A8	I711 C4	I735 A3	I959 B9
F0007 C10	F306 A1	F325 A9	F348 C8	F368 B2	F4505 A9	F5110 A5	F6002 C10	I008 B9	I034 B3	I323 A3	I343 C1	I407 A4	I437 A6	I459 A5	I485 A7	I511 A8	I615 B7	I532 A7	I712 B4	I739 B4	I987 A10
F0009 C10	F307 B1	F326 B2	F349 C3	F369 B2	F4707 A6	F5113 A4	F6004 C6	I009 B9	I035 B3	I324 B1	I344 C2	I408 A4	I438 B6	I460 A5	I486 A6	I513 B7	I616 B7	I533 A8	I713 C4	I741 B3	I988 A10
F0010 C9	F308 A2	F328 B1	F350 C3	F371 A3	F4712 B6	F5116 A5	F701 A3	I013 B9	I036 A1	I325 B1	I345 A2	I409 A4	I439 A6	I461 A4	I487 A9	I514 C6	I617 B7	I534 A7	I715 A9	I742 B3	I989 A10
F0011 C10	F309 A2	F329 B1	F351 A3	F372 A3	F4714 B6	F5119 A4	F702 B4	I014 B10	I037 C1	I326 A2	I346 A3	I411 B6	I440 A6	I462 A4	I488 A9	I515 B7	I620 B6	I535 A7	I716 A10	I743 B4	I990 A10
F0012 C10	F310 A2	F331 A3	F352 C8	F373 B3	F4716 B6	F5120 A4	F703 A3	I015 B9	I038 B2	I327 B2	I347 B7	I412 B6	I441 A6	I463 A4	I489 A9	I516 B7	I621 B6	I539 A8	I717 B4	I744 B4	I991 A10
F0014 C10	F311 A2	F333 A3	F353 C8	F374 B3	F4718 B6	F5201 A5	F704 A3	I018 B10	I039 B3	I329 A2	I348 C1	I413 C5	I442 B7	I464 A4	I490 A10	I517 B8	I623 B6	I540 A8	I721 C4	I745 B4	I992 A10
F0016 C10	F312 B1	F334 A2	F354 A2	F381 C8	F4720 B6	F5202 A5	F707 A3	I019 B10	I040 B3	I330 C1	I349 B7	I414 A5	I443 A7	I465 A4	I491 A10	I518 B8	I624 B7	I601 B6	I723 C7	I746 B4	I993 A10
F0021 A10	F313 A1	F335 A2	F355 C3	F382 C9	F4721 A6	F5203 A5	F708 B5	I020 A9	I041 B9	I331 C1	I350 C2	I415 C8	I444 A6	I466 B5	I492 A9	I519 A8	I625 B7	I602 C8	I724 C5	I748 B4	I994 A10
F006 C9	F314 A1	F336 A2	F356 C3	F383 C8	F4722 B6	F5206 A5	F709 B4	I021 B9	I042 B9	I332 B2	I351 C2	I416 B5	I445 A6	I467 A6	I493 A9	I520 A8	I630 C6	I603 B6	I725 C5	I749 C4	I995 A10
F007 C8	F315 C1	F337 A2	F357 C3	F384 C8	F485 A6	F5207 A5	F710 B3	I022 C9	I043 B3	I333 A3	I352 B7	I417 B5	I446 B6	I468 B6	I494 A9	I521 A4	I631 C6	I604 B6	I726 B4	I751 C5	I996 A9
F008 C9	F316 C2	F338 B1	F358 C6	F401 A9	F499 A4	F5208 A5	F713 C7	I023 B10	I044 A1	I334 A2	I353 A3	I418 C4	I447 B6	I469 B5	I495 B8	I522 A7	I632 B7	I605 B7	I727 B4	I754 C4	I997 A10
F009 C9	F317 C4	F339 B1	F359 C8	F4102 A9	F501 A7	F5210 A5	F713 B5	I029 C10	I045 B3	I335 C1	I354 A3	I419 C9	I448 A7	I470 B5	I496 A8	I523 A7	I633 B6	I606 B7	I728 B4	I755 A4	I998 A10
F010 A10	F318 C2	F340 A2	F360 C3	F4103 A9	F502 A7	F5211 A5	F950 C9	I030 B9	I046 A1	I336 B2	I355 C2	I420 C9	I449 A6	I472 A5	I497 A8	I524 B9	I634 C6	I607 B4	I729 B4	I756 A4	I999 A10
F011 B10	F319 C2	F341 B3	F361 C2	F412 A8	F504 A3	F5213 A4	I001 C10	I031 B10	I047 A1	I337 A3	I356 A2	I424 A4	I451 A6	I478 B6	I505 C5	I526 B9	I635 B6	I608 C7	I730 B4	I757 A4	I999 A10
F300 A3	F320 C1	F342 C1	F362 A2	F4203 C5	F5101 A5	F5215 A5	I002 B10	I032 B10	I048 A7	I338 A3	I357 A2	I428 A7	I453 A9	I479 B5	I506 B5	I527 B6	I610 B7	I706 B3	I731 C4	I758 A4	I999 A10



Test points overview DIVIO Board



F0101	B5	F503	B1	F565	C2
F0102	B5	F504	B2	F566	C3
F0103	B5	F505	B1	F567	C2
F0104	B5	F506	B2	F601	F4
F0106	B5	F507	B1	F603	C4
F0201	E6	F508	B2	F604	F4
F0202	D2	F509	C1	F605	F3
F0203	C2	F510	B2	F606	F3
F0204	C2	F511	B1	F609	E3
F0205	E3	F512	B1	F610	E3
F0301	A2	F513	B1	F611	F3
F0302	A1	F514	B1	F614	F3
F0401	F3	F515	B1	F615	F3
F0402	F1	F516	B1	F616	F3
F0403	F1	F517	C3	F617	G3
F0404	F1	F518	D2	F618	E5
F0405	F1	F519	B2	F619	F2
F0406	F1	F520	B2	F620	G3
F122	B5	F521	C1	F621	F2
F400	C5	F522	B2	F622	F2
F401	C5	F523	C2	F623	F2
F402	B5	F524	C2	F624	F4
F403	C5	F525	B3	F800	F2
F404	C5	F526	B2	F801	F2
F405	C5	F527	B2	F802	B1
F406	C5	F528	C2	F803	B1
F407	C5	F529	B2	F804	E2
F408	C5	F530	C2	F805	F2
F409	B6	F531	C2	F806	D2
F410	B5	F532	C2	F808	F2
F411	B5	F533	C2	F809	E2
F412	A6	F534	C1	F810	G1
F413	C5	F535	C1	F811	E2
F414	C5	F536	B3	F812	F2
F415	C6	F537	C2	F815	D2
F416	C6	F538	E2	F816	E2
F417	C6	F539	C1	F817	E3
F418	C6	F540	A3	F818	E3
F419	C6	F541	A3	F819	E2
F420	C5	F542	A3	F820	E2
F421	B5	F543	A3	F822	E2
F422	B5	F544	B3	F823	E3
F423	B5	F545	B3	F824	E2
F424	B6	F547	C1	F825	E3
F425	B6	F548	B3	F826	E3
F430	D5	F549	C1	F827	E1
F431	E5	F550	C1	F829	E1
F432	E5	F551	B2	F830	E1
F433	D4	F552	B3	F831	F1
F434	C4	F553	A3	F832	F2
F435	D5	F554	B2	F833	G2
F436	B4	F555	B2	F834	G2
F437	G5	F556	B1	F835	G1
F438	E3	F557	C1	F836	E1
F439	C5	F558	B1	F837	F1
F440	D5	F559	C1	F838	F2
F441	C4	F560	D3	F839	G1
F442	E3	F561	C3		
F443	D5	F562	G1		
F501	B2	F563	C2		
F502	B2	F564	C2		

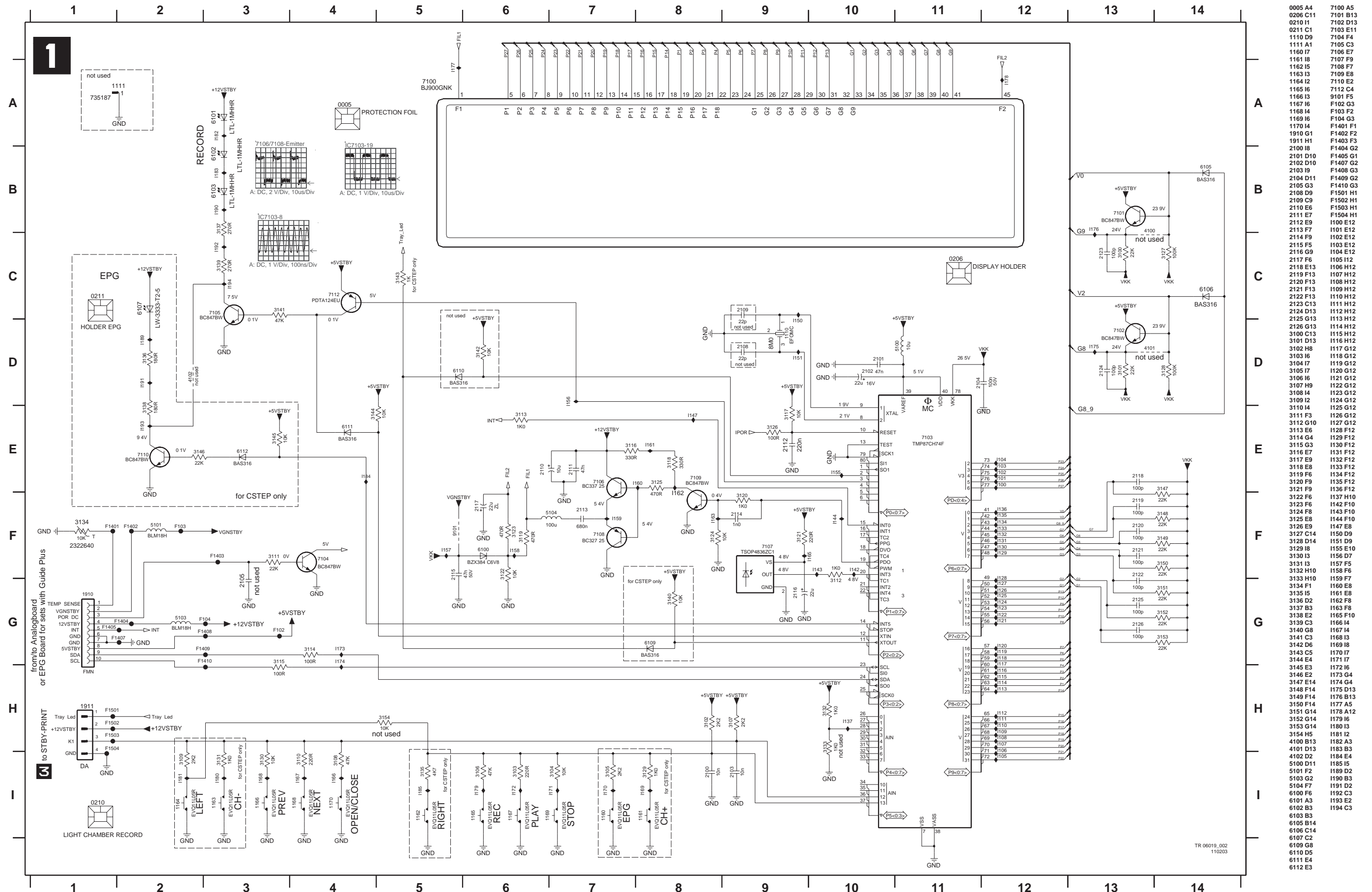
TR03021_001
090802

Layout Digital Board (Mapping Testlands)

F214	A3	I175	A3	I300	A2	I610	A5	I720	B3	I880	C3
F247	A2	I176	A3	I301	A2	I611	B5	I721	B2	I881	C3
F248	A2	I177	A3	I302	A2	I612	A5	I722	B3	I882	C3
F249	A2	I178	A3	I303	B2	I613	B5	I723	B2	I883	C2
F250	A2	I179	A3	I304	B3	I614	A5	I724	B2	I884	C2
F264	A2	I180	A3	I305	B3	I615	B5	I725	B3	I900	B4
F265	A3	I181	A3	I306	A3	I616	A5	I726	B2	I901	B4
F931	A4	I182	B3	I307	B3	I617	A5	I727	B2	I902	B4
F932	A4	I183	A2	I308	A3	I618	C4	I728	A1	I903	B4
F933	A5	I184	A3	I309	B3	I619	A5	I729	A1	I904	B2
F934	A4	I186	A3	I400	A4	I621	A1	I730	A1	I905	A4
F935	A4	I187	A3	I401	A4	I622	A1	I731	A1	I906	A4
I100	A4	I188	A3	I402	B4	I623	A1	I732	B2	I907	A4
I101	C5	I200	A2	I403	A4	I624	A1	I733	B2	I908	A5
I102	C5	I201	B3	I404	B4	I625	A1	I734	B1	I909	B4
I103	B4	I202	A5	I405	B4	I626	A1	I735	B1	I911	B3
I104	B4	I203	A3	I406	B4	I627	B4	I800	C4	I912	A3
I105	B3	I204	C3	I407	A4	I628	C4	I801	C3	I913	B3
I106	B3	I205	A2	I408	A5	I629	A5	I802	C3	I915	B3
I107	B3	I206	A4	I409	A4	I630	C4	I803	C3	I916	B3
I108	B3	I207	A2	I410	A4	I631	C4	I805	C3	I917	B3
I109	B4	I208	B3	I412	B4	I632	C4	I806	C3	I918	A5
I110	B3	I209	B4	I413	A4	I633	B4	I807	C3	I919	B3
I111	A2	I210	A2	I414	B4	I634	C4	I808	C2	I920	B3
I112	B5	I211	A2	I415	B4	I635	C5	I809	C2	I921	A5
I113	B5	I212	A2	I416	B4	I636	C4	I810	C3	I922	A5
I114	B5	I213	A2	I500	C5	I637	C5	I811	C3	I923	B3
I115	B5	I215	B5	I501	C5	I638	C5	I812	C2	I924	A4
I116	C3	I216	A1	I502	C5	I639	C5	I813	C2	I925	B3
I117	C3	I217	A2	I503	C5	I640	C5	I814	C1	I926	A5
I118	C4	I218	A2	I504	C5	I641	B5	I815	B2	I927	A5
I119	C4	I219	A1	I505	C5	I642	A5	I816	B2	I928	A5
I120	A4	I220	A1	I506	C5	I643	A5	I817	B2	I930	B3
I121	A3	I221	B2	I507	C5	I644	A5	I818	C2	I931	A5
I122	B3	I222	B2	I508	C5	I645	B5	I819	C3	I932	B2
I123	A2	I223	A2	I509	C5	I646	C4	I820	C3	I933	B3
I124	B4	I224	A1	I510	B5	I647	A5	I821	C3		
I125	A2	I225	A2	I511	C4	I649	C5	I822	C3		
I126	A3	I226	A2	I512	C5	I650	B4	I823	C3		
I127	A2	I227	A2	I513	B5	I651	B5	I824	B2		
I128	A4	I228	A2	I514	B4	I652	B5	I825	B2		
I129	A2	I229	B5	I515	C5	I653	B5	I826	C3		
I130	B3	I230	A2	I516	C5	I654	B4	I827	C3		
I131	A3	I231	A2	I517	C5	I655	B4	I828	C3		
I132	B1	I232	A2	I518	C4	I656	B5	I829	C3		
I133	A3	I233	A2	I519	C5	I657	C4	I830	C3		
I134	A3	I234	A4	I520	C4	I658	C4	I831	C3		
I136	A3	I235	A4	I521	C4	I659	C3	I832	C3		
I137	A2	I236	B4	I522	C4	I660	B5	I833	C3		
I138	A3	I237	A2	I523	C4	I661	B5	I834	B3		
I140	A3	I238	A2	I524	C4	I662	C5	I835	B3		
I141	A4	I239	B5	I525	C5	I663	B4	I836	B2		
I142	A3	I240	A4	I526	C5	I664	B5	I837	C3		
I143	B4	I241	B2	I527	C5	I665	C4	I838	C3		
I145	A3	I242	B1	I528	C4	I666	C5	I839	C3		
I147	B4	I243	B1	I529	C5	I667	B5	I840	C3		
I149	B3	I244	A2	I530	C5	I668	B4	I841	C3		
I152	B3	I245	A1	I531	C5	I669	B4	I842	C3		
I153	B5	I246	A2	I532	C5	I670	A5	I843	C2		
I154	B3	I251	A1	I533	C4	I671	B5	I844	C2		
I155	B3	I252	A2	I535	C5	I700	B2	I845	C2		
I156	A3	I253	A2	I536	C4	I701	B1	I846	B3		
I157	A3	I254	A1	I537	C5	I702	B1	I847	B2		
I158	B4	I255	A1	I538	C4	I703	C2	I848	B2		
I159	A5	I256	A2	I540	C5	I704	C2	I849	B2		
I160	B3	I257	C5	I543	C5	I705	C2	I850	B2		
I161	B3	I258	A2	I551	C5	I706	C2	I851	B1		
I162	C4	I259	A2	I552	C4	I707	C2	I852	B1		
I163	A3	I260	A1	I553	C4	I708	C2	I858	C2		
I164	B4	I261	A1	I555	C4	I709	C1	I869	C2		
I165	A3	I262	A1	I600	A5	I710	B3	I870	B2		
I166	B4	I263	A1	I601	A5	I711	C2	I871	C3		
I167	A3	I264	A2	I602	A5	I712	C2	I872	C3		
I168	C5	I265	B5	I603	C5	I713	A1	I873	B2		
I169	A3	I266	A2	I604	A5	I714	C2	I874	C2		
I170	A3	I267	A2	I605	A5	I715	C2	I875	C2		
I171	A3	I268	B2	I606	A5	I716	B3	I876	C3		
I172	A3	I269	B2	I607	A5	I717	B3	I877	C2		
I173	A3	I270	A2	I608	A5	I718	B3	I878	C3		
I174	A3	I271	B1	I609	B5	I719	B3	I879	C3		

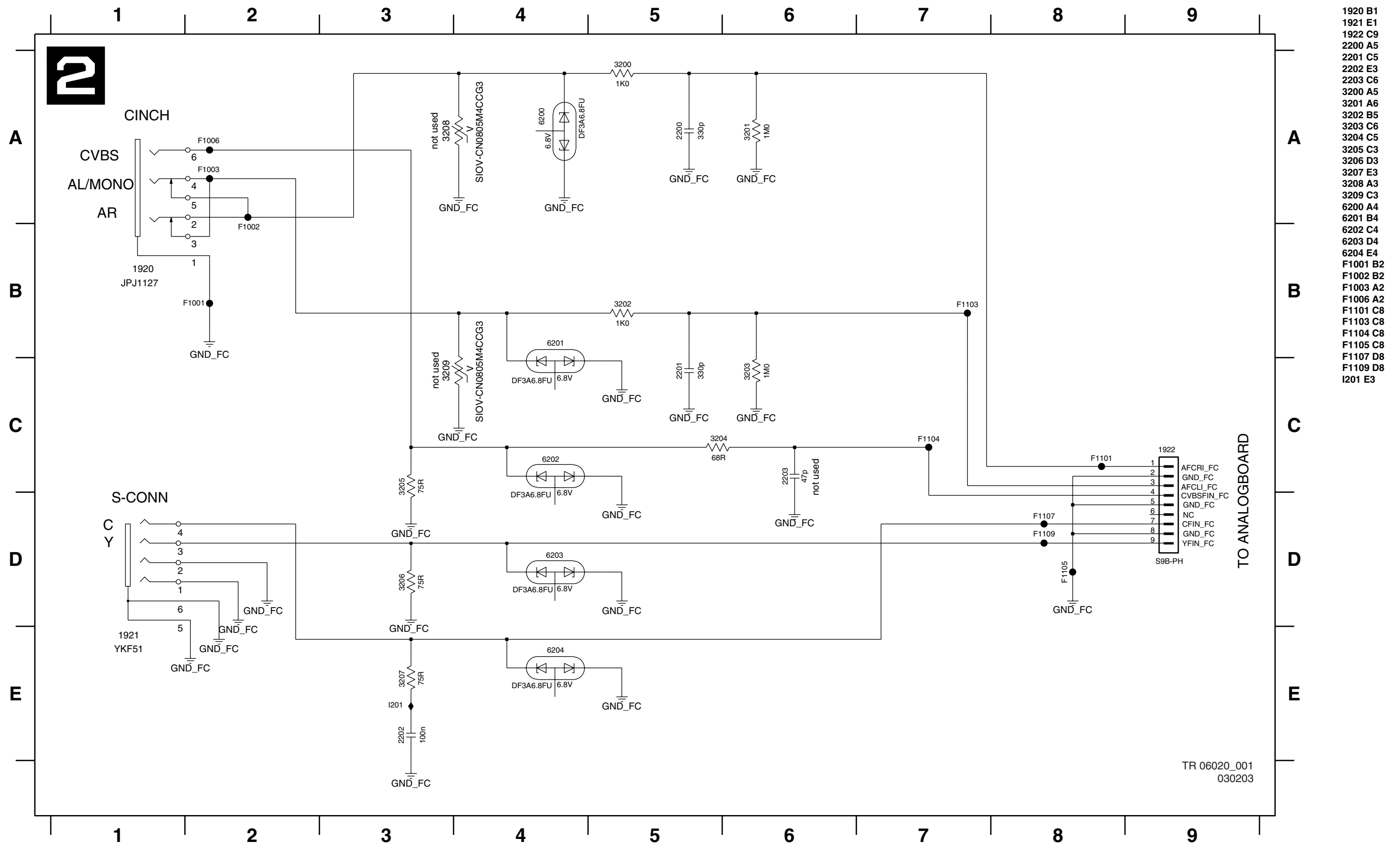
7. Circuit Diagrams and PWB Layouts

Display Panel

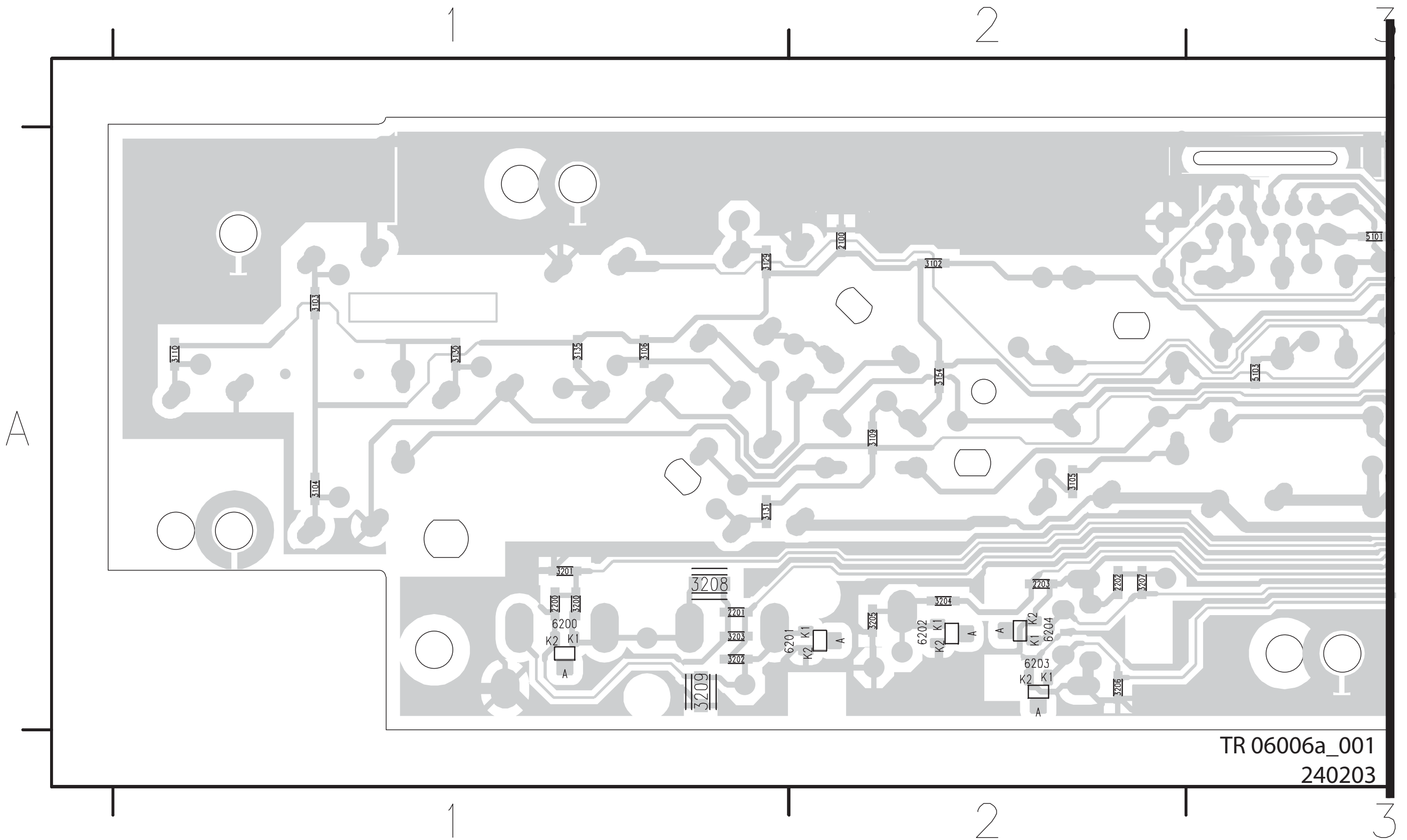


0005 A4	7100 A5
0206 C11	7101 B13
0210 I1	7102 D13
0211 C1	7103 E11
1110 D9	7104 F4
1111 A1	7105 C3
1160 I7	7106 E7
1161 B8	7107 F9
1162 I5	7108 F7
1163 I3	7109 E8
1164 I2	7110 E2
1165 I6	7112 C4
1166 I3	9101 F5
1167 I6	F102 G3
1168 I4	F103 F2
1169 I6	F104 G3
1170 I4	F1401 F1
1910 G1	F1402 F2
1911 H1	F1403 F3
2100 I8	F1404 G2
2101 D10	F1405 G1
2102 D10	F1407 G2
2103 I9	F1408 G3
2104 D11	F1409 G2
2105 G3	F1410 G3
2108 D9	F1501 H1
2109 C9	F1502 H1
2110 E6	F1503 H1
2111 E7	F1504 H1
2112 E9	I100 E12
2113 F7	I101 E12
2114 F9	I102 E12
2115 F5	I103 E12
2116 G9	I104 E12
2117 F6	I105 I12
2118 E13	I106 H12
2119 F13	I107 H12
2120 F13	I108 H12
2121 F13	I109 H12
2122 F13	I110 H12
2123 C13	I111 H12
2124 D13	I112 H12
2125 G13	I113 H12
2126 G13	I114 H12
3100 C13	I115 H12
3101 D13	I116 H12
3102 H8	I117 G12
3103 I6	I118 G12
3104 I7	I119 G12
3105 I7	I120 G12
3106 I6	I121 G12
3107 H9	I122 G12
3108 I4	I123 G12
3109 I2	I124 G12
3110 I4	I125 G12
3111 F3	I126 G12
3112 G10	I127 G12
3113 E6	I128 F12
3114 G4	I129 F12
3115 G3	I130 F12
3116 E7	I131 F12
3117 E9	I132 F12
3118 E8	I133 F12
3119 F6	I134 F12
3120 F9	I135 F12
3121 F9	I136 F12
3122 F6	I137 H10
3123 F6	I142 F10
3124 F8	I143 F10
3125 E8	I144 F10
3126 E9	I147 E9
3127 C14	I150 D9
3128 D14	I151 D9
3129 I8	I155 E10
3130 I3	I156 D7
3131 I3	I157 F5
3132 H10	I158 F6
3133 H10	I159 F7
3134 F1	I160 E8
3135 I5	I161 E8
3136 D2	I162 F8
3137 B3	I163 F8
3138 E2	I165 F10
3139 C3	I166 I4
3140 G8	I167 I4
3141 C3	I168 I3
3142 D6	I169 I8
3143 C5	I170 I7
3144 E4	I171 I7
3145 E3	I172 I6
3146 E2	I173 G4
3147 E14	I174 G4
3148 F14	I175 D13
3149 F14	I176 B13
3150 F14	I177 A5
3151 G14	I178 A12
3152 G14	I179 I6
3153 G14	I180 I3
3154 H5	I181 I2
4100 B13	I182 A3
4101 D13	I183 B3
4102 D2	I184 E4
5100 D11	I185 I5
5101 F2	I189 D2
5103 G2	I190 B3
5104 F7	I191 D2
6100 F6	I192 C3
6101 A3	I193 E2
6102 B3	I194 C3
6103 B3	
6105 B14	
6106 C14	
6107 C2	
6109 G8	
6110 D5	
6111 E4	
6112 E3	

Front Connector (FC)

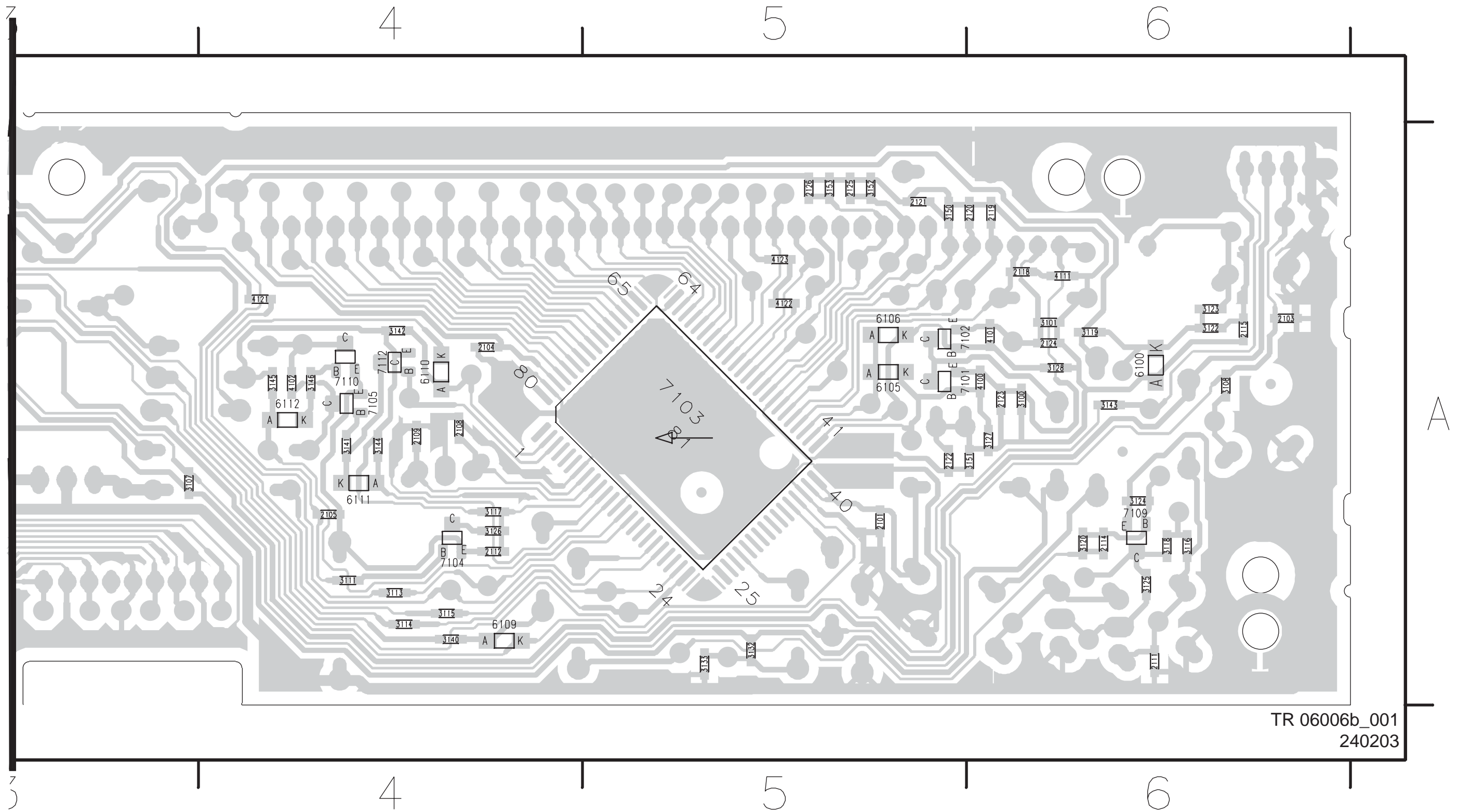


Layout Display Panel (Part 1 Bottom View)



TR 06006a_001
240203

Layout Display Panel (Part 2 Bottom View)

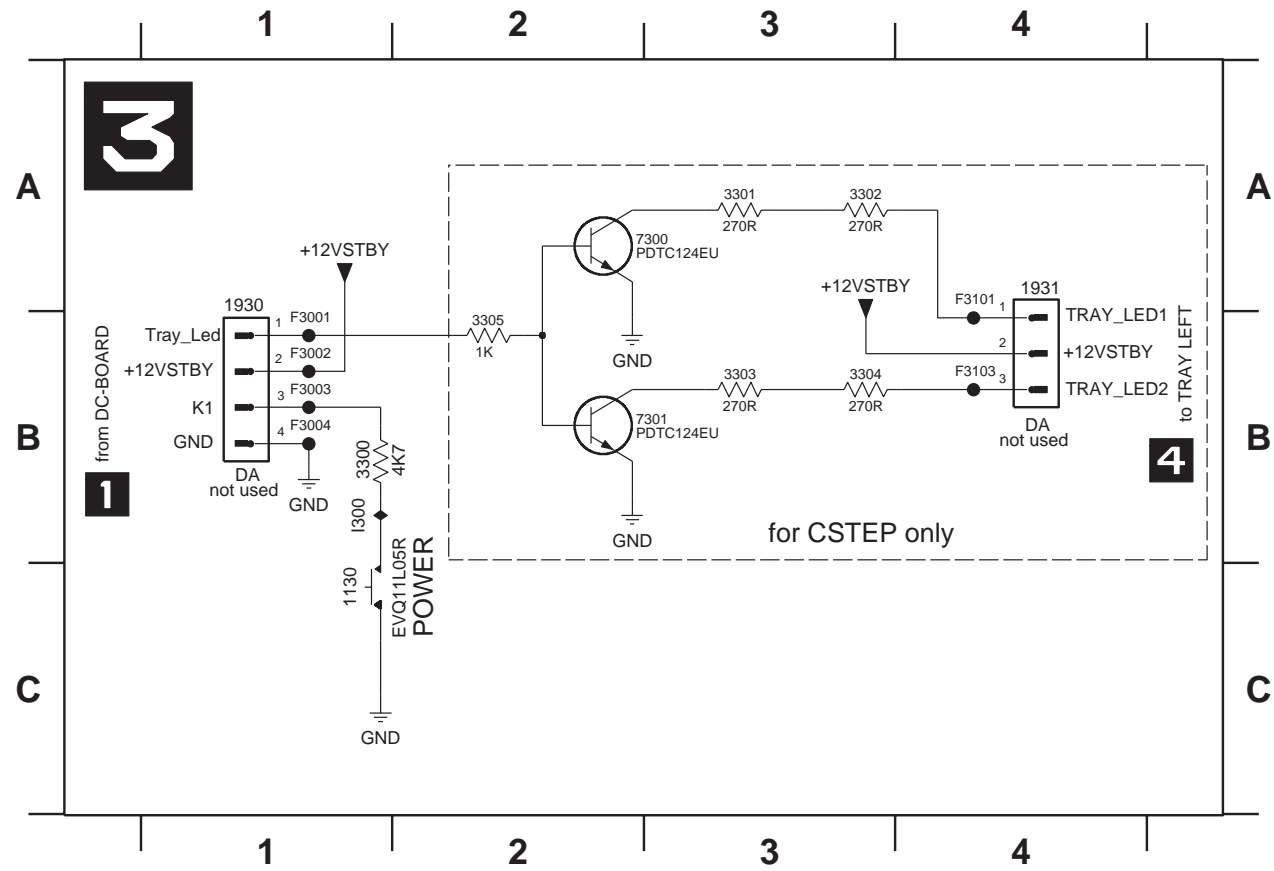


TR 06006b_001
240203

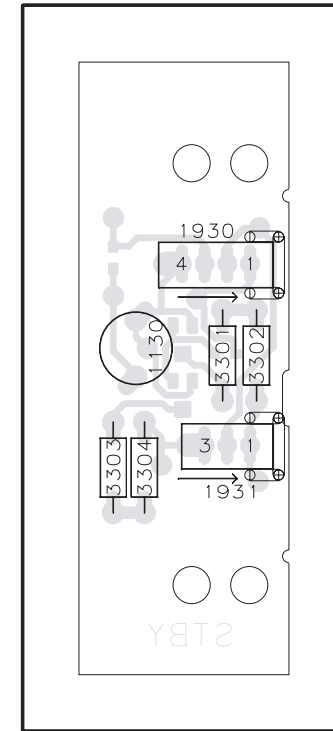
Standby Panel (STBY)

Layout Standby Panel

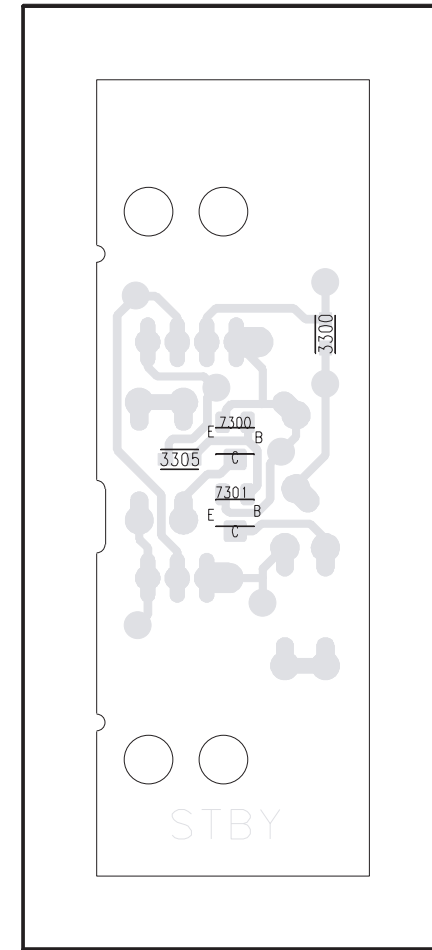
1130 C1	1931 A4	3301 A3	3303 B3	3305 B2	7301 B2	F3002 B1	F3004 B1	F3103 B4
1930 A1	3300 B1	3302 A3	3304 B3	7300 A2	F3001 B1	F3003 B1	F3101 A4	I300 B1



TR 07003_001
110303



1130	--
1930	--
1931	--
3300	--
3301	--
3302	--
3303	--
3304	--

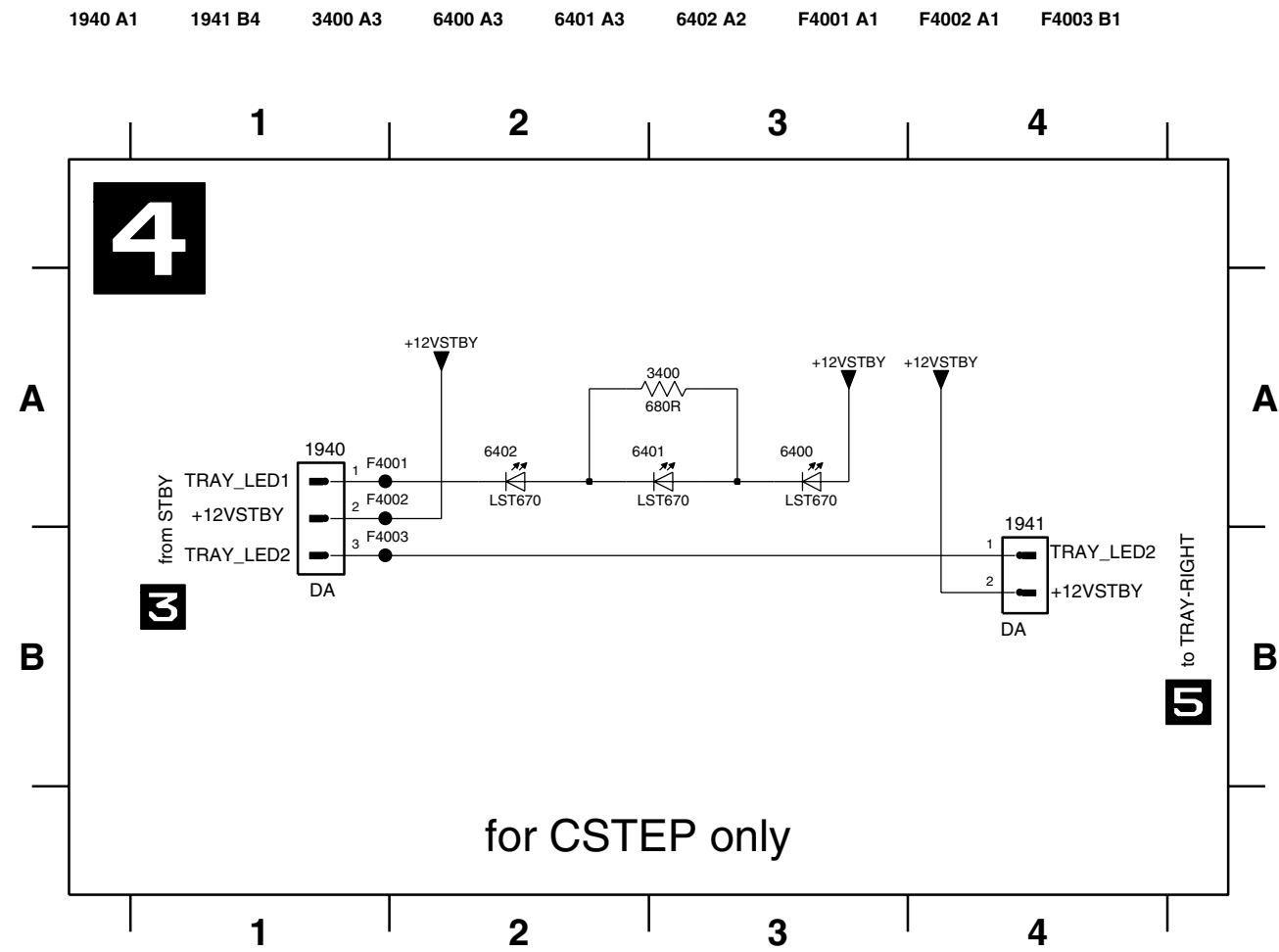


3300	--
3305	--
7300	--
7301	--

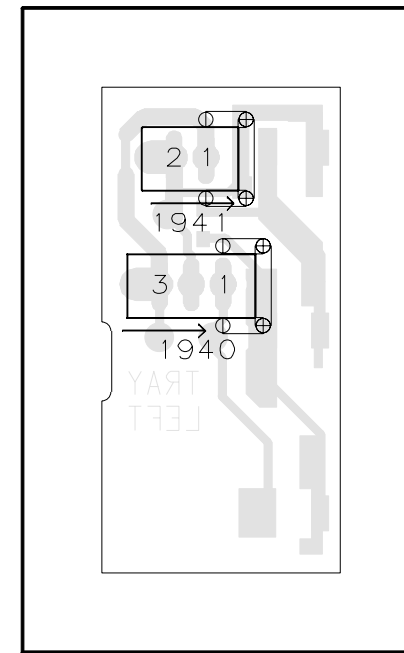
TR 06007_001
030203

Tray Left Panel (TRL)

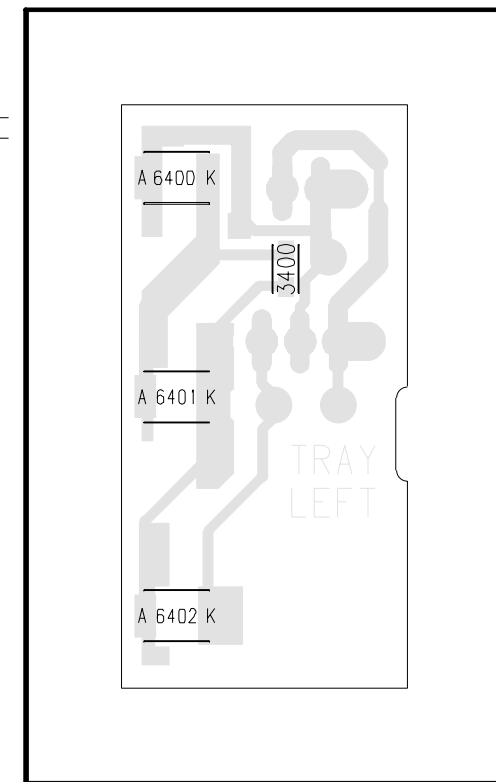
Layout Tray Left Panel



TR 06021_001
030203



1940 --
1941 --

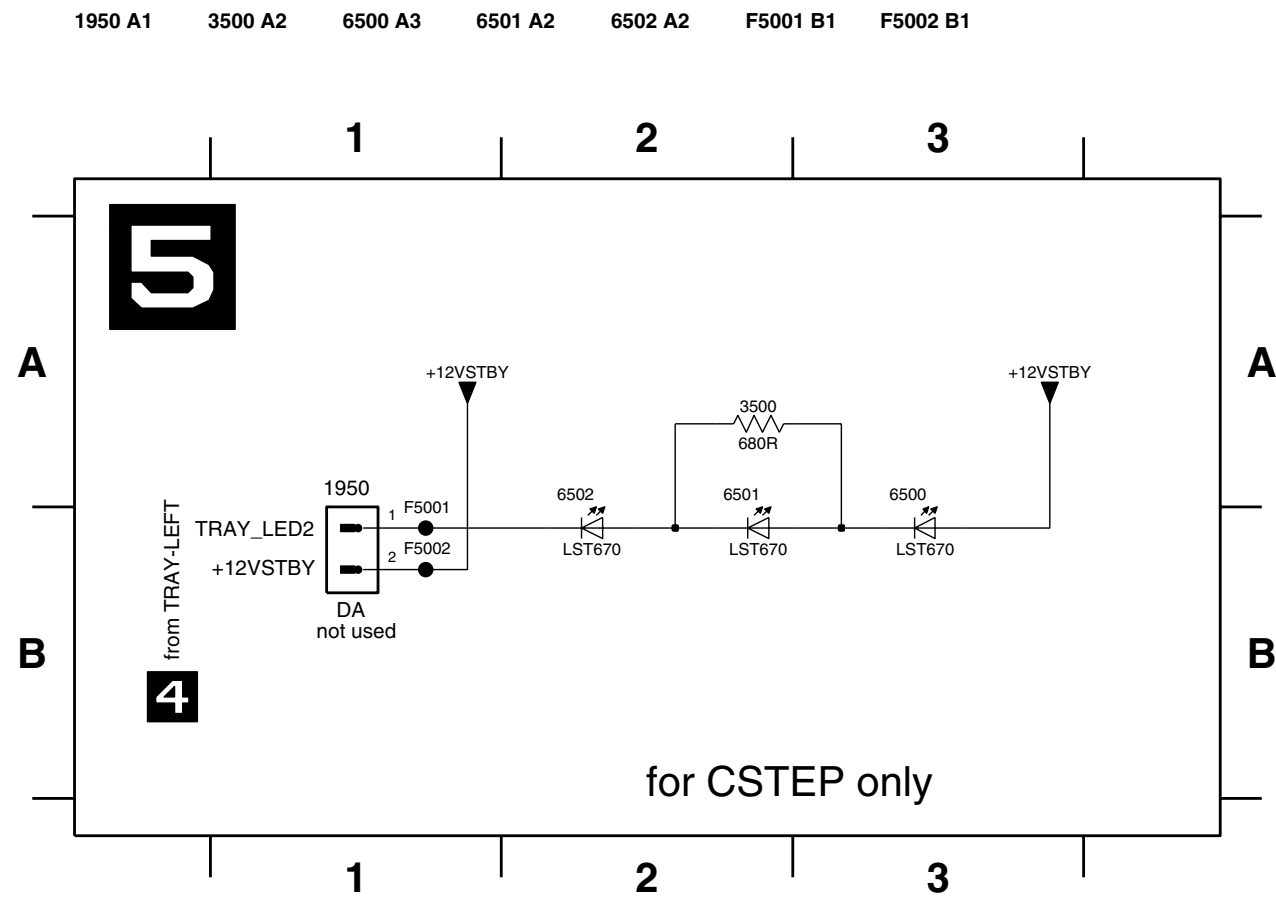


3400 --
6400 --
6401 --
6402 --

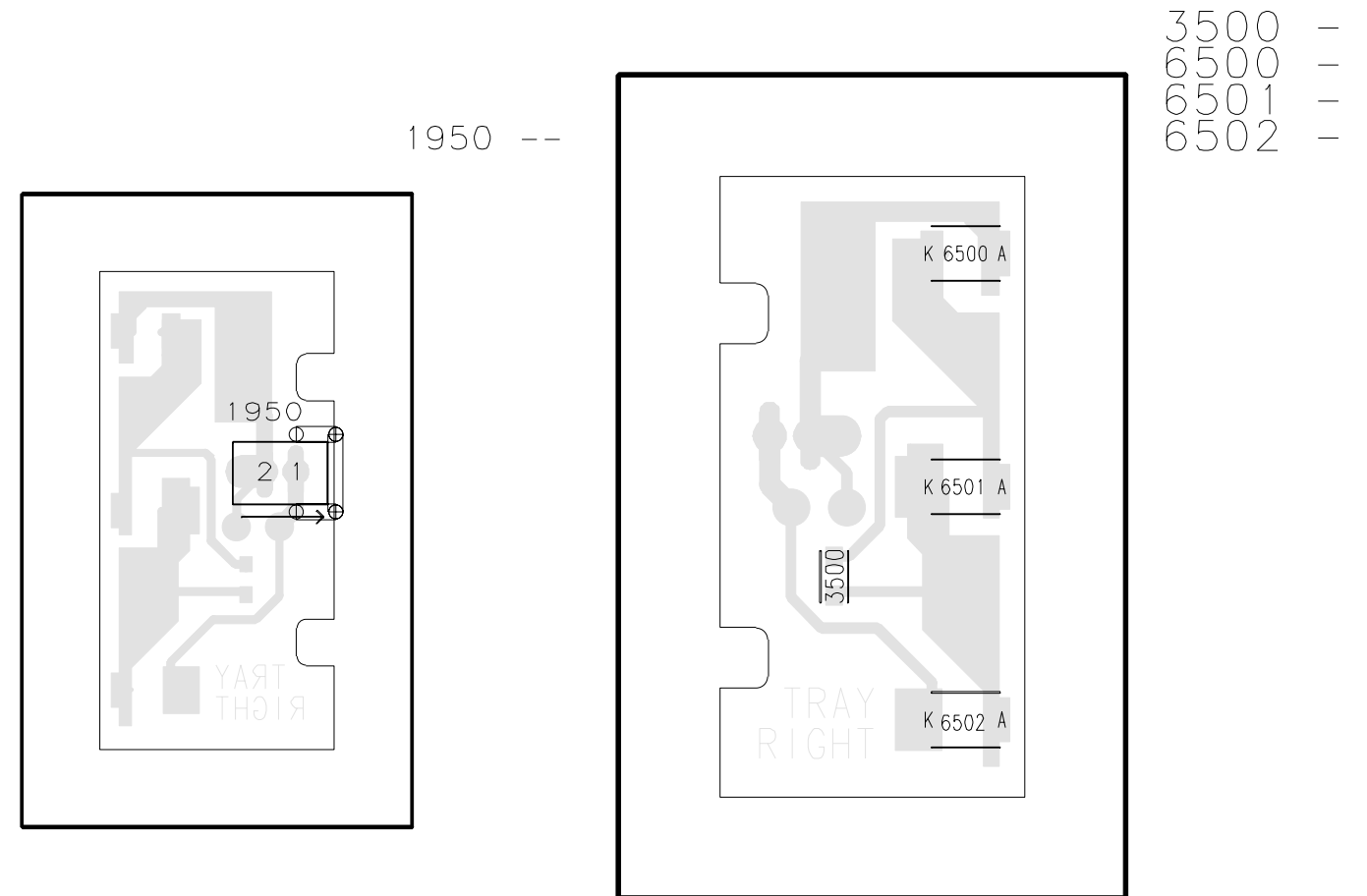
TR06008_001
030203

Tray Right Panel (TRR)

Layout Tray Right Panel

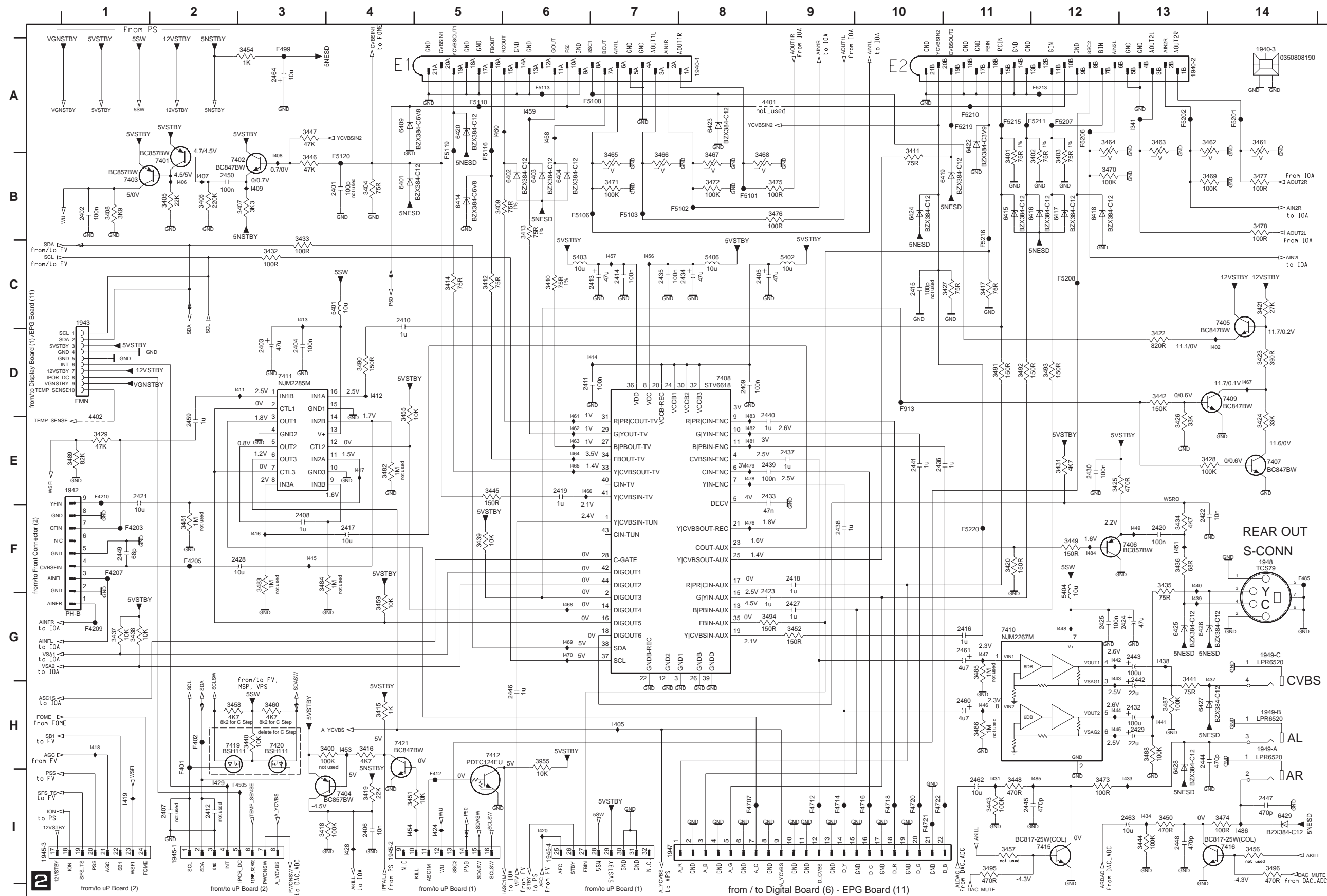


TR 06022_001
030203

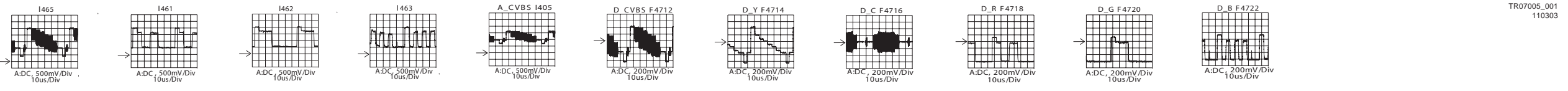


TR06009_001
030203

Analog Board: In/Out Video (IOV)

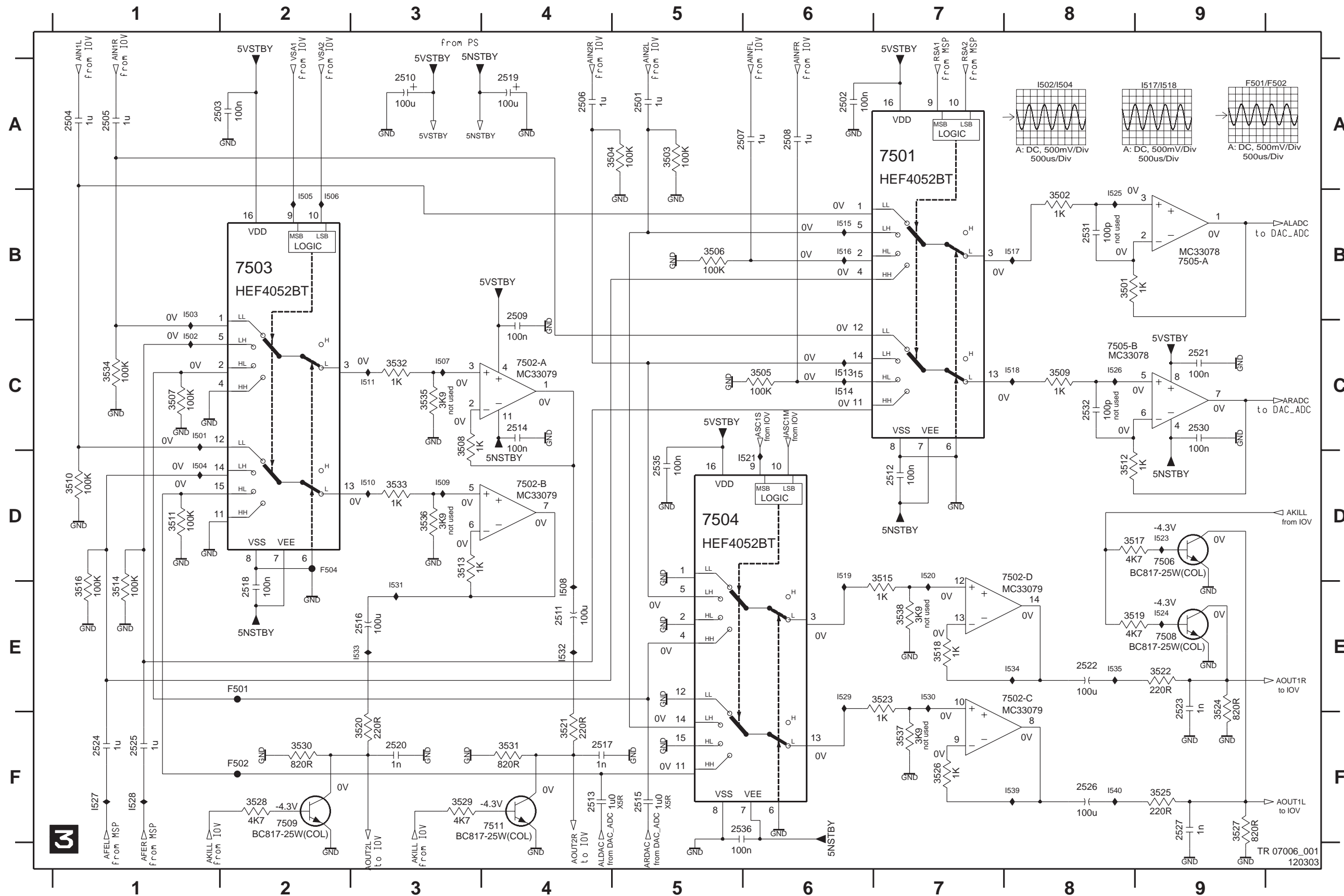


- 1940 1 A8
- 1940 2 A13
- 1940 3 A14
- 1942 E1
- 1943 C1
- 1945 I 12
- 1947 I7
- 1948 F14
- 1949 A H14
- 1949 B H14
- 1949 C G14
- 2002 B1
- 2002 B2
- 2003 G1
- 2004 D3
- 2005 C8
- 2006 I4
- 2007 I2
- 2008 F3
- 2009 D8
- 2010 D4
- 2011 D6
- 2012 I2
- 2013 C7
- 2014 C7
- 2015 C10
- 2016 G11
- 2017 F4
- 2018 F9
- 2019 E6
- 2020 F13
- 2021 E1
- 2022 F13
- 2023 F2
- 2024 G13
- 2025 F2
- 2027 G9
- 2028 F1
- 2029 H13
- 2030 E12
- 2031 H4
- 2033 E9
- 2034 H10
- 2037 E9
- 2038 F9
- 2039 E9
- 2040 E9
- 2041 D1
- 2042 H13
- 2043 G11
- 2044 H13
- 2045 H11
- 2046 H6
- 2047 H4
- 2048 H3
- 2049 F1
- 2050 B2
- 2051 A14
- 2052 E2
- 2060 H11
- 2061 G11
- 2062 H11
- 2063 I13
- 2064 A3
- 2065 H4
- 2066 B11
- 2067 B11
>
- 2068 B12
- 2069 F11
- 2070 D10
- 2071 A13
- 2072 D14
- 2073 B3
- 2074 B3
- 2075 B2
- 2076 B2
- 2077 B2
- 2078 B3
- 2079 B3
- 2080 B3
- 2081 B3
- 2082 B3
- 2083 B3
- 2084 B3
- 2085 B3
- 2086 B3
- 2087 B3
- 2088 B3
- 2089 B3
- 2090 B3
- 2091 B3
- 2092 B3
- 2093 B3
- 2094 B3
- 2095 B3
- 2096 B3
- 2097 B3
- 2098 B3
- 2099 B3
- 2100 B3
- 2101 B3
- 2102 B3
- 2103 B3
- 2104 B3
- 2105 B3
- 2106 B3
- 2107 B3
- 2108 B3
- 2109 B3
- 2110 B3
- 2111 B3
- 2112 B3
- 2113 B3
- 2114 B3
- 2115 B3
- 2116 B3
- 2117 B3
- 2118 B3
- 2119 B3
- 2120 B3
- 2121 B3
- 2122 B3
- 2123 B3
- 2124 B3
- 2125 B3
- 2126 B3
- 2127 B3
- 2128 B3
- 2129 B3
- 2130 B3
- 2131 B3
- 2132 B3
- 2133 B3
- 2134 B3
- 2135 B3
- 2136 B3
- 2137 B3
- 2138 B3
- 2139 B3
- 2140 B3
- 2141 B3
- 2142 B3
- 2143 B3
- 2144 B3
- 2145 B3
- 2146 B3
- 2147 B3
- 2148 B3
- 2149 B3
- 2150 B3
- 2151 B3
- 2152 B3
- 2153 B3
- 2154 B3
- 2155 B3
- 2156 B3
- 2157 B3
- 2158 B3
- 2159 B3
- 2160 B3
- 2161 B3
- 2162 B3
- 2163 B3
- 2164 B3
- 2165 B3
- 2166 B3
- 2167 B3
- 2168 B3
- 2169 B3
- 2170 B3
- 2171 B3
- 2172 B3
- 2173 B3
- 2174 B3
- 2175 B3
- 2176 B3
- 2177 B3
- 2178 B3
- 2179 B3
- 2180 B3
- 2181 B3
- 2182 B3
- 2183 B3
- 2184 B3
- 2185 B3
- 2186 B3
- 2187 B3
- 2188 B3
- 2189 B3
- 2190 B3
- 2191 B3
- 2192 B3
- 2193 B3
- 2194 B3
- 2195 B3
- 2196 B3
- 2197 B3
- 2198 B3
- 2199 B3
- 2200 B3
- 2201 B3
- 2202 B3
- 2203 B3
- 2204 B3
- 2205 B3
- 2206 B3
- 2207 B3
- 2208 B3
- 2209 B3
- 2210 B3
- 2211 B3
- 2212 B3
- 2213 B3
- 2214 B3
- 2215 B3
- 2216 B3
- 2217 B3
- 2218 B3
- 2219 B3
- 2220 B3
- 2221 B3
- 2222 B3
- 2223 B3
- 2224 B3
- 2225 B3
- 2226 B3
- 2227 B3
- 2228 B3
- 2229 B3
- 2230 B3
- 2231 B3
- 2232 B3
- 2233 B3
- 2234 B3
- 2235 B3
- 2236 B3
- 2237 B3
- 2238 B3
- 2239 B3
- 2240 B3
- 2241 B3
- 2242 B3
- 2243 B3
- 2244 B3
- 2245 B3
- 2246 B3
- 2247 B3
- 2248 B3
- 2249 B3
- 2250 B3
- 2251 B3
- 2252 B3
- 2253 B3
- 2254 B3
- 2255 B3
- 2256 B3
- 2257 B3
- 2258 B3
- 2259 B3
- 2260 B3
- 2261 B3
- 2262 B3
- 2263 B3
- 2264 B3
- 2265 B3
- 2266 B3
- 2267 B3
- 2268 B3
- 2269 B3
- 2270 B3
- 2271 B3
- 2272 B3
- 2273 B3
- 2274 B3
- 2275 B3
- 2276 B3
- 2277 B3
- 2278 B3
- 2279 B3
- 2280 B3
- 2281 B3
- 2282 B3
- 2283 B3
- 2284 B3
- 2285 B3
- 2286 B3
- 2287 B3
- 2288 B3
- 2289 B3
- 2290 B3
- 2291 B3
- 2292 B3
- 2293 B3
- 2294 B3
- 2295 B3
- 2296 B3
- 2297 B3
- 2298 B3
- 2299 B3
- 2300 B3



TR07005_001
110303

Analog Board: IN/Out Audio (IOA)

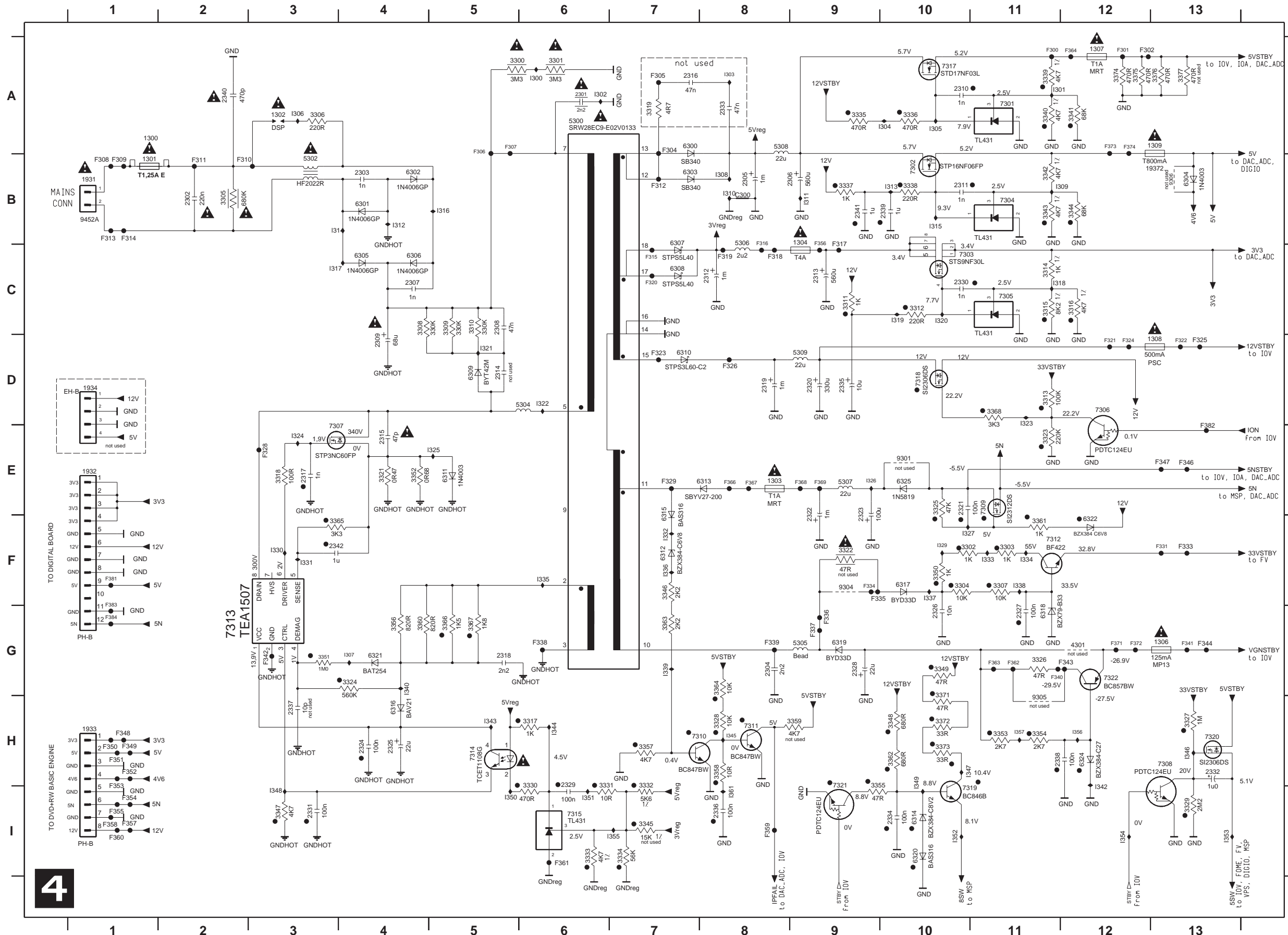


- 2501 A5
- 2502 A6
- 2503 A2
- 2504 A1
- 2505 A1
- 2506 A4
- 2507 A6
- 2508 A6
- 2509 B4
- 2510 A3
- 2511 E4
- 2512 D7
- 2513 F4
- 2514 C4
- 2515 F5
- 2516 E3
- 2517 F4
- 2518 E2
- 2519 A4
- 2520 F3
- 2521 C9
- 2522 E8
- 2523 E9
- 2524 F1
- 2525 F1
- 2526 F8
- 2527 F9
- 2530 C9
- 2531 B8
- 2532 C8
- 2533 D5
- 2536 F5
- 3501 B8
- 3502 B8
- 3503 A5
- 3504 A5
- 3505 C6
- 3506 B5
- 3507 C1
- 3508 C3
- 3509 C8
- 3510 D1
- 3511 D1
- 3512 D8
- 3513 D3
- 3514 E1
- 3515 D7
- 3516 E1
- 3517 D8
- 3518 E7
- 3519 E8
- 3520 F3
- 3521 F4
- 3522 E9
- 3523 E7
- 3524 E9
- 3525 F9
- 3526 F7
- 3527 F9
- 3528 F2
- 3529 F3
- 3530 F2
- 3531 F4
- 3532 C3
- 3533 D3
- 3534 C1
- 3535 C3
- 3536 D3
- 3537 F7
- 3538 E7
- 7501 A7
- 7502-A C4
- 7502-B D4
- 7502-C E7
- 7502-D D7
- 7503 B2
- 7504 D5
- 7505-A B9
- 7505-B C8
- 7506 D9
- 7508 E9
- 7509 F2
- 7511 F4
- F501 E2
- F502 F2
- I501 C1
- I502 C1
- I503 B1
- I504 D1
- I505 B2
- I506 B2
- I507 C3
- I508 E4
- I509 D3
- I510 D3
- I511 C3
- I512 C6
- I513 C6
- I514 C6
- I515 B6
- I516 B6
- I517 B8
- I518 C8
- I519 D6
- I520 D7
- I521 D6
- I523 D9
- I524 E9
- I525 B8
- I526 C8
- I527 F1
- I528 F1
- I529 E6
- I530 E7
- I531 E3
- I532 E4
- I533 E3
- I534 E8
- I535 E8
- I539 F8
- I540 F8

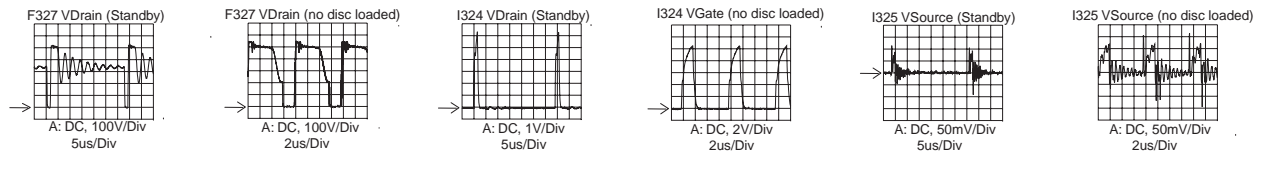


TR 07006_001
120303

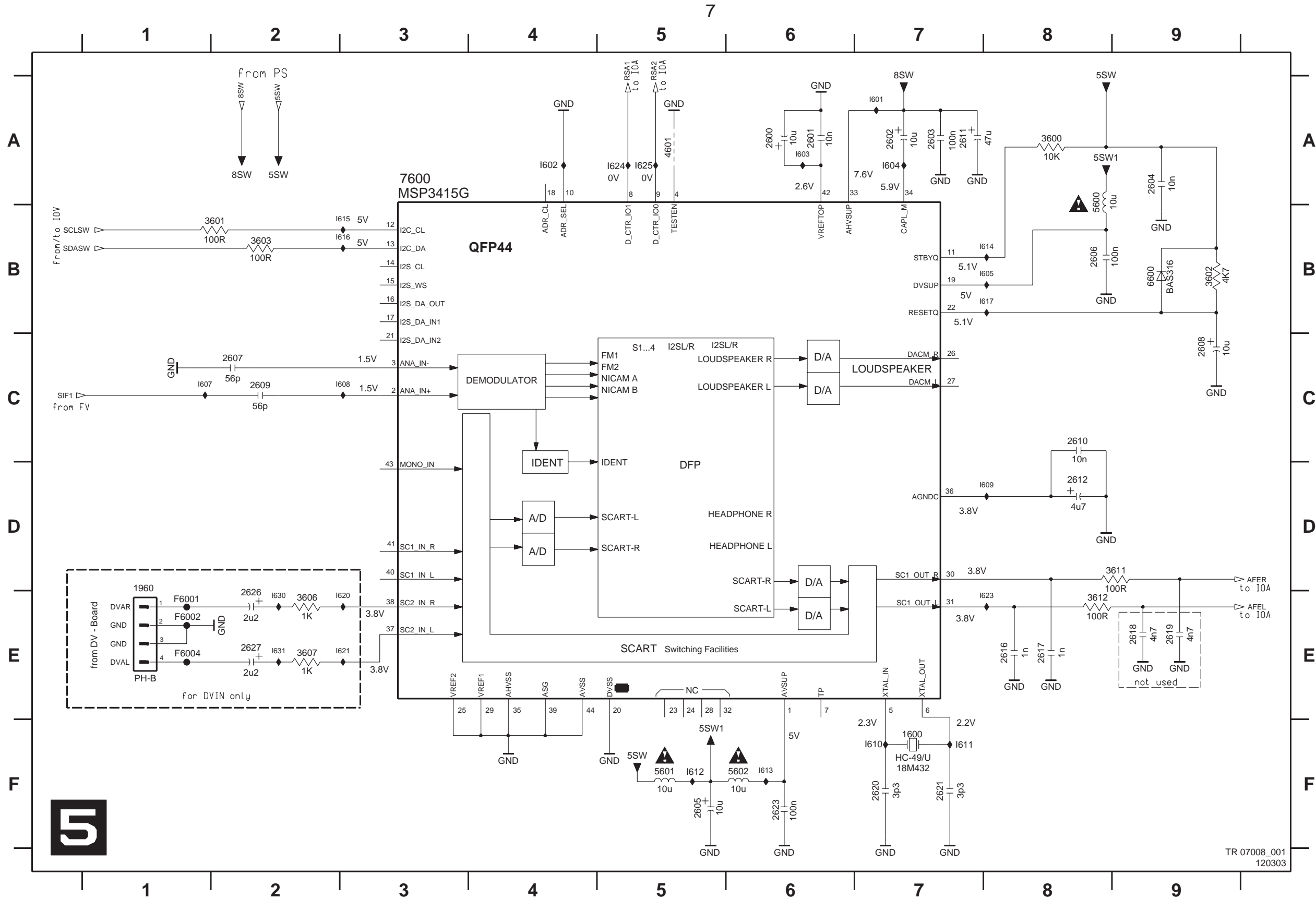
Analog Board for VAE8020: Power Supply (PS)



1300 A1	3364 G8	F351 H1
1301 B1	3365 F3	F352 H1
1302 A3	3366 G5	F353 H1
1303 E8	3367 G5	F354 H1
1304 C9	3368 D11	F355 H1
1306 G13	3371 H10	F356 C9
1307 A12	3372 H10	F357 H1
1308 D13	3373 H10	F358 H1
1309 A13	3374 A12	F359 I8
1931 B1	3375 A12	F360 H1
1932 E1	3376 A13	F361 I6
1933 H1	3377 A12	F362 G11
1934 D1	4301 G12	F363 G11
2301 A6	5300 A6	F364 A12
2302 B2	5302 B3	F366 E8
2303 B4	5304 D6	F367 E8
2304 G8	5305 G9	F368 E8
2305 B8	5306 C8	F369 E9
2306 B9	5307 E9	F371 G12
2307 C4	5308 A8	F372 G12
2308 C5	5309 D9	F373 A12
2309 D4	6300 A7	F374 A12
2310 A10	6301 B4	F381 F1
2311 B10	6302 B4	F382 E13
2312 C8	6303 B7	F383 G1
2313 C9	6304 B13	F384 G1
2314 D5	6305 C4	I300 A6
2315 E4	6306 C4	I301 A11
2316 A7	6307 C7	I302 A6
2317 E3	6308 C7	I303 A8
2318 G5	6309 D5	I304 A10
2319 D8	6310 D7	I305 A10
2320 D9	6311 E5	I306 A3
2321 E10	6312 F7	I307 G4
2322 E9	6313 E8	I308 B8
2323 E9	6314 H10	I309 B12
2324 H4	6315 E7	I310 B8
2325 H4	6316 H4	I311 B9
2326 G10	6317 F10	I312 B4
2327 G11	6318 G11	I313 B10
2328 G9	6319 G9	I314 B3
2329 I6	6320 I10	I315 B10
2330 C10	6321 G4	I316 B5
2331 I3	6322 F12	I317 C3
2332 H13	6324 H12	I318 C11
2333 A8	6325 E10	I319 C10
2334 I10	7301 A11	I320 C10
2335 D9	7302 B10	I321 D5
2336 I8	7303 C10	I322 D6
2337 H3	7304 B11	I323 D11
2338 H11	7305 C11	I324 E5
2339 E10	7306 D12	I325 E5
2340 A2	7307 E3	I326 E9
2341 B9	7308 H13	I327 F10
2342 F3	7309 E11	I329 F10
3300 A5	7310 H7	I330 F3
3301 A6	7311 H8	I331 F3
3302 F10	7312 F11	I332 F11
3303 F11	7313 G12	I333 F11
3304 F10	7314 H5	I334 F11
3305 B2	7315 I6	I335 F6
3306 A3	7317 A10	I336 F7
3307 F11	7318 D10	I337 F10
3308 C4	7319 I10	I338 F11
3309 C5	7320 H13	I339 G7
3310 C5	7321 I9	I340 G4
3311 C9	7322 G12	I342 I12
3312 C10	9301 E10	I343 H5
3313 D11	9304 F9	I344 H6
3314 C11	9305 H11	I345 H8
3315 C11	9306 B13	I346 H13
3316 C12	C300 B8	I347 H10
3317 H6	F300 A11	I348 I3
3318 E3	F301 A12	I349 H10
3319 A7	F302 A12	I350 I5
3321 E4	F304 A7	I351 I6
3322 F9	F305 A7	I352 I10
3323 E11	F306 A5	I353 I13
3324 G4	F307 A5	I354 I12
3325 E10	F308 B1	I355 I7
3326 G11	F309 B1	I356 H12
3327 H13	F310 B2	I357 H11
3328 H8	F311 B2	I361 I8
3329 I13	F312 B7	
3330 I6	F313 B1	
3331 I6	F314 B1	
3332 I7	F315 C7	
3333 I6	F316 C8	
3334 I7	F317 C9	
3335 A9	F318 C8	
3336 A10	F319 C8	
3337 B9	F320 C7	
3338 B10	F321 D12	
3339 A11	F322 D13	
3340 A11	F323 D7	
3341 A12	F324 D12	
3342 B11	F325 D13	
3343 B11	F326 D8	
3344 B12	F328 E3	
3345 I7	F329 E7	
3346 F7	F331 F13	
3347 I3	F333 F13	
3348 H10	F334 F9	
3349 G10	F335 F9	
3350 F10	F336 G9	
3351 G3	F337 G9	
3352 E4	F338 G6	
3353 H11	F339 G8	
3354 H11	F340 G11	
3355 I9	F341 G13	
3356 G4	F342 G3	
3357 H7	F343 G12	
3358 H8	F344 G13	
3359 H9	F346 E13	
3360 G4	F347 E13	
3361 F11	F348 H1	
3362 H10	F349 H1	
3363 G7	F350 H1	



Analog Board: Multi Sound Processing (MSP)

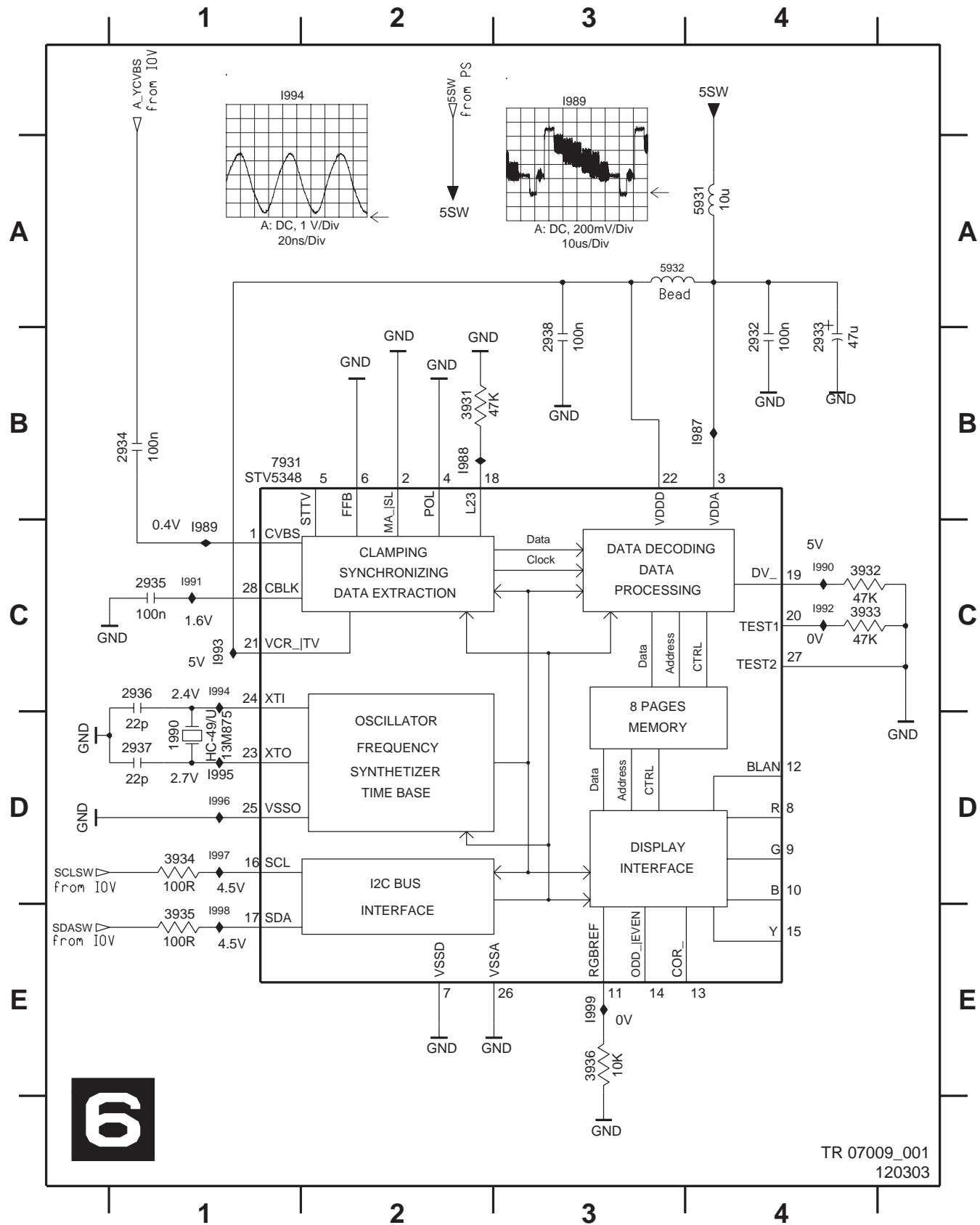


- 1600 F7
- 1960 E1
- 2600 A6
- 2601 A6
- 2602 A7
- 2603 A7
- 2604 A9
- 2605 F5
- 2606 B8
- 2607 C2
- 2608 C9
- 2609 C2
- 2610 C8
- 2611 A7
- 2612 D8
- 2616 E8
- 2617 E8
- 2618 E9
- 2619 E9
- 2620 F7
- 2621 F7
- 2623 F6
- 2626 E2
- 2627 E2
- 3600 A8
- 3601 B2
- 3602 B9
- 3603 B2
- 3606 E2
- 3607 E2
- 3611 D9
- 3612 E8
- 4601 A5
- 5600 A8
- 5601 F5
- 5602 F6
- 6600 B9
- 7600 A3
- F6001 E1
- F6002 E1
- F6004 E1
- I601 A7
- I602 A4
- I603 A6
- I604 A7
- I605 B8
- I607 C1
- I608 C3
- I609 D8
- I610 F7
- I611 F7
- I612 F5
- I613 F6
- I614 B8
- I615 B3
- I616 B3
- I617 B8
- I620 E3
- I621 E3
- I623 E8
- I624 A5
- I625 A5
- I630 E2
- I631 E2



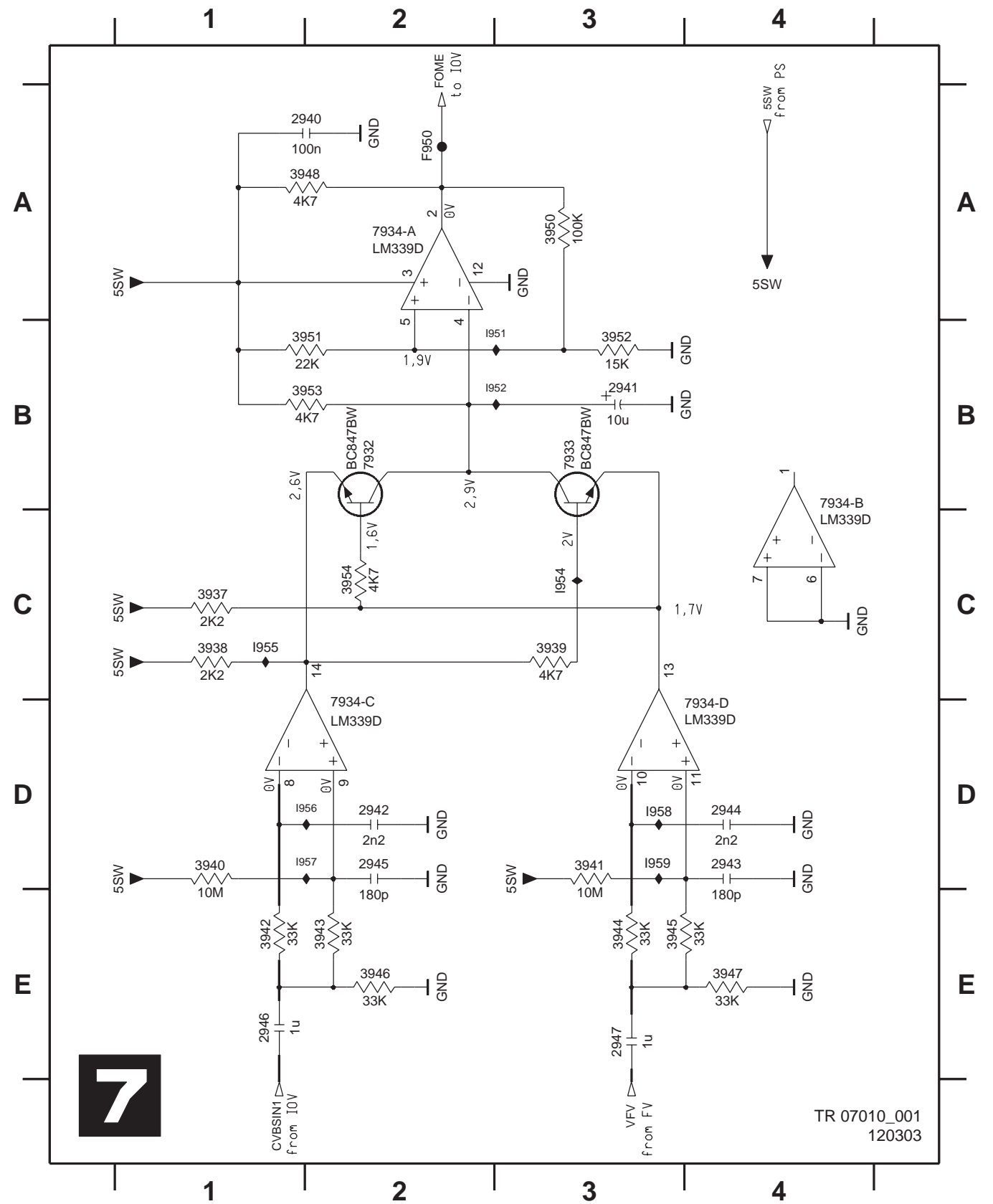
Analog Board: VPS

1990 D1	2934 B1	2937 D1	3932 C4	3935 E1	5932 A3	1988 B2	1991 C1	1994 C1	1997 D1
2932 B4	2935 C1	2938 B3	3933 C4	3936 E3	7931 B2	1989 C1	1992 C4	1995 D1	1998 E1
2933 B4	2936 C1	3931 B2	3934 D1	5931 A4	1987 B4	1990 C4	1993 C1	1996 D1	1999 E3



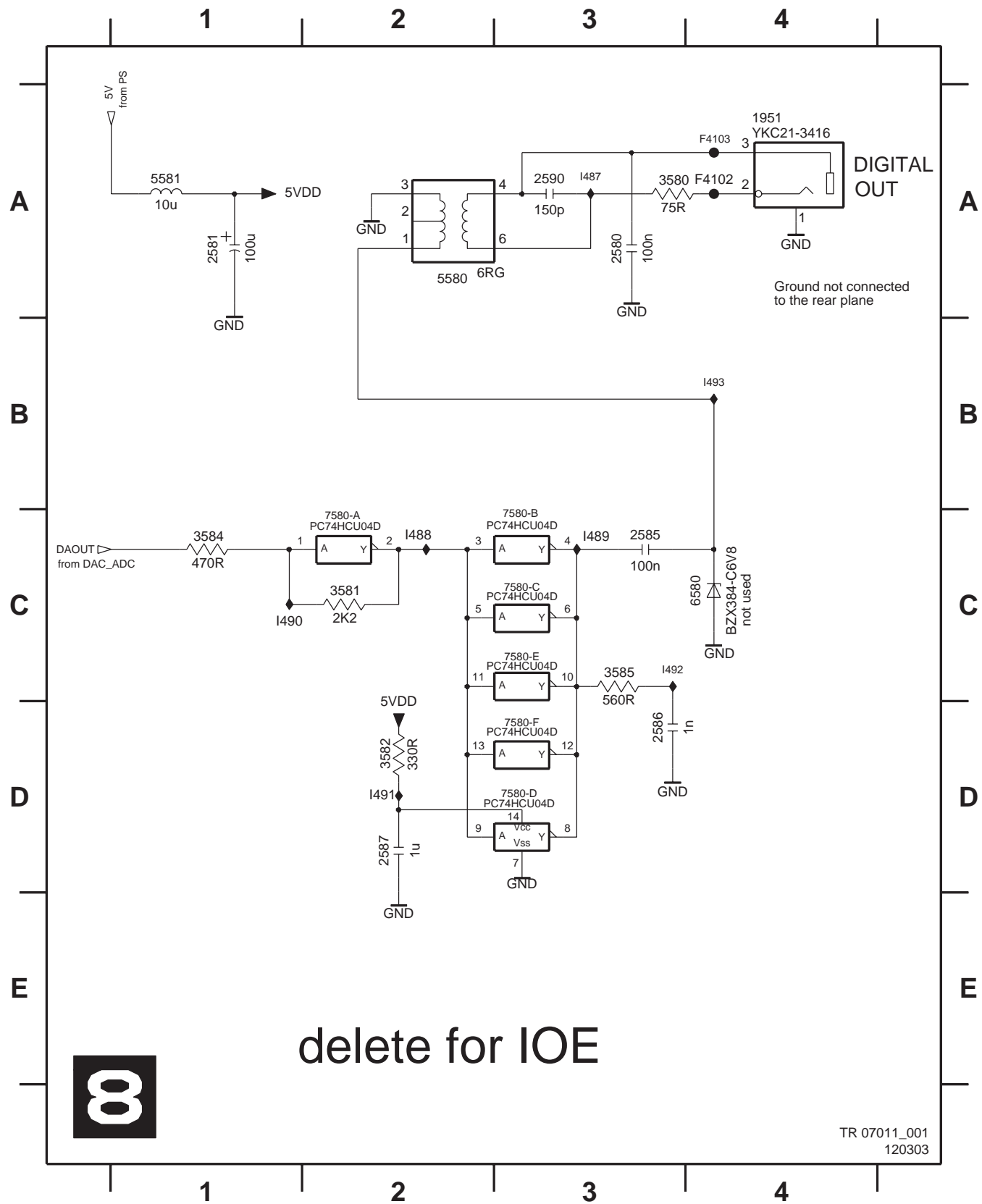
Analog Board: Follow Me (FOME)

2940 A2	2944 D4	3937 C1	3941 D3	3945 E3	3950 A3	3954 C2	7934-B B4	1951 B3	1956 D2
2941 B3	2945 D2	3938 C1	3942 E1	3946 E2	3951 B2	7932 B2	7934-C C2	1952 B3	1957 D2
2942 D2	2946 E1	3939 C3	3943 E2	3947 E4	3952 B3	7933 B3	7934-D C3	1954 C3	1958 D3
2943 D4	2947 E3	3940 D1	3944 E3	3948 A2	3953 B2	7934-A A2	F950 A2	1955 C1	1959 D3

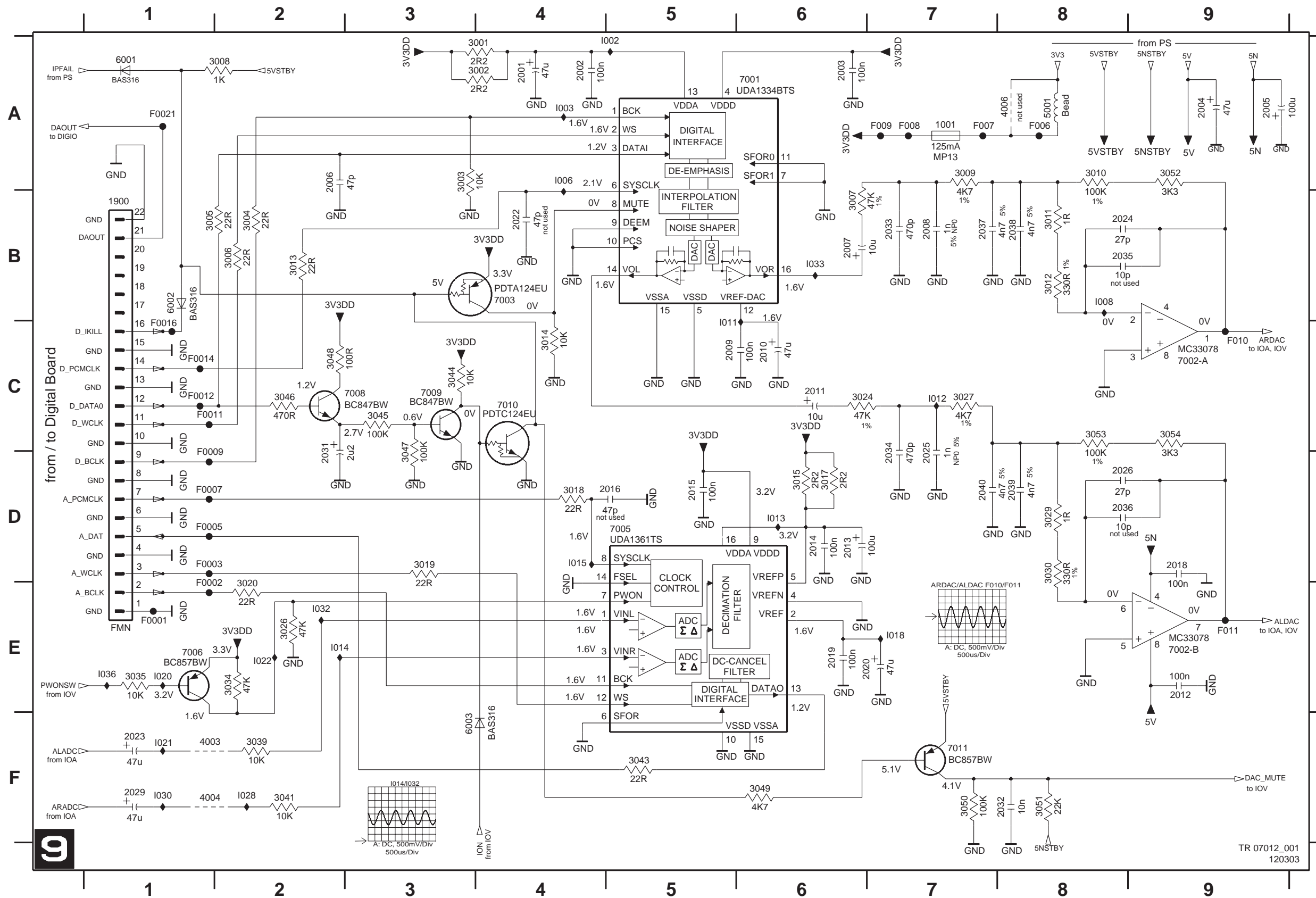


Analog Board: Digital In / Out (DIGIO)

1951 A4	2585 C3	2590 A3	3582 D2	5580 A2	7580-A C2	7580-D D3	F4102 A4	I488 C2	I491 D2
2580 A3	2586 D3	3580 A3	3584 C1	5581 A1	7580-B C3	7580-E C3	F4103 A4	I489 C3	I492 C3
2581 A1	2587 D2	3581 C2	3585 C3	6580 C4	7580-C C3	7580-F D3	I487 A3	I490 C1	I493 B4

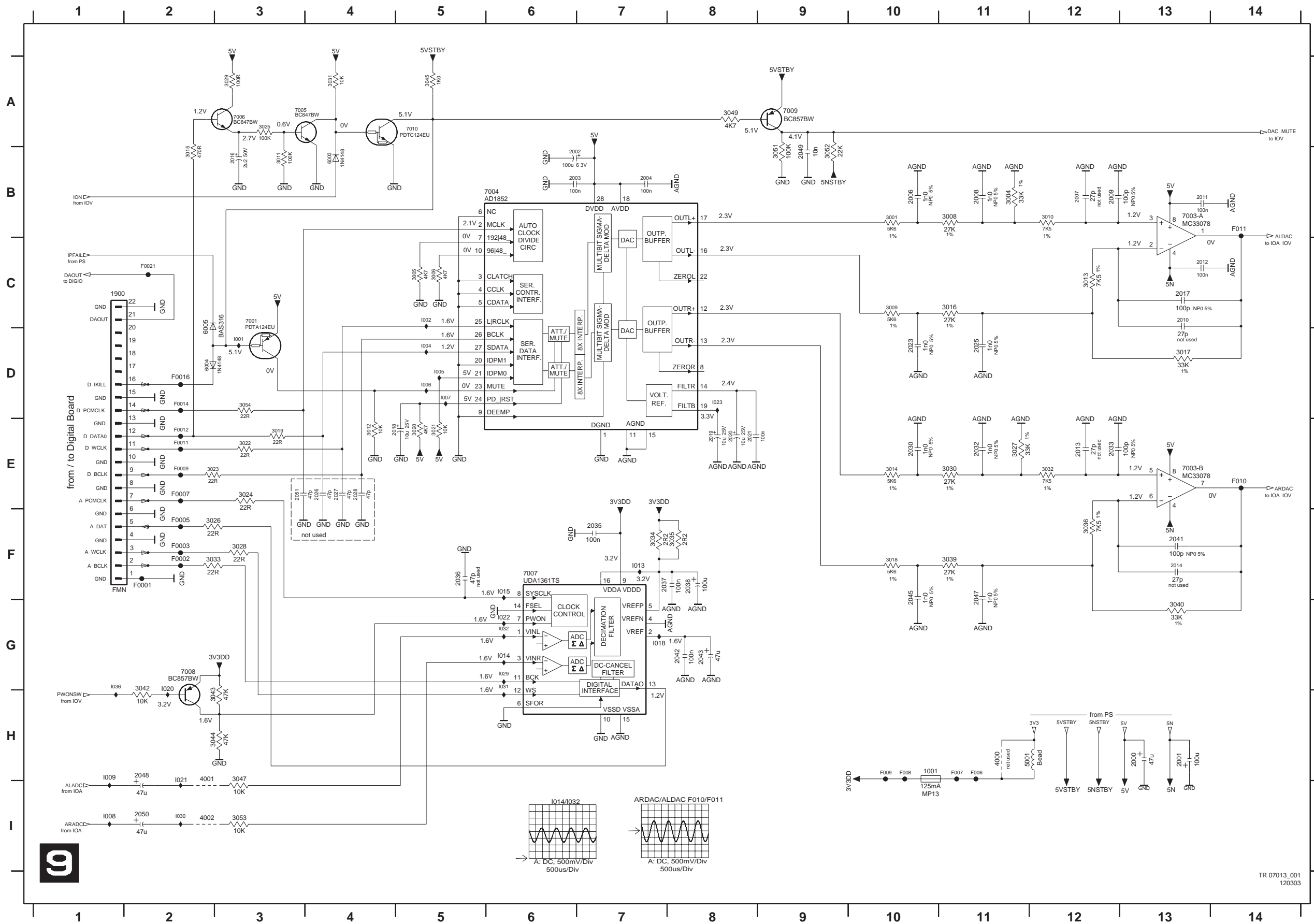


Analog Board 603 3033: Audio Converter (DAC_ADC)



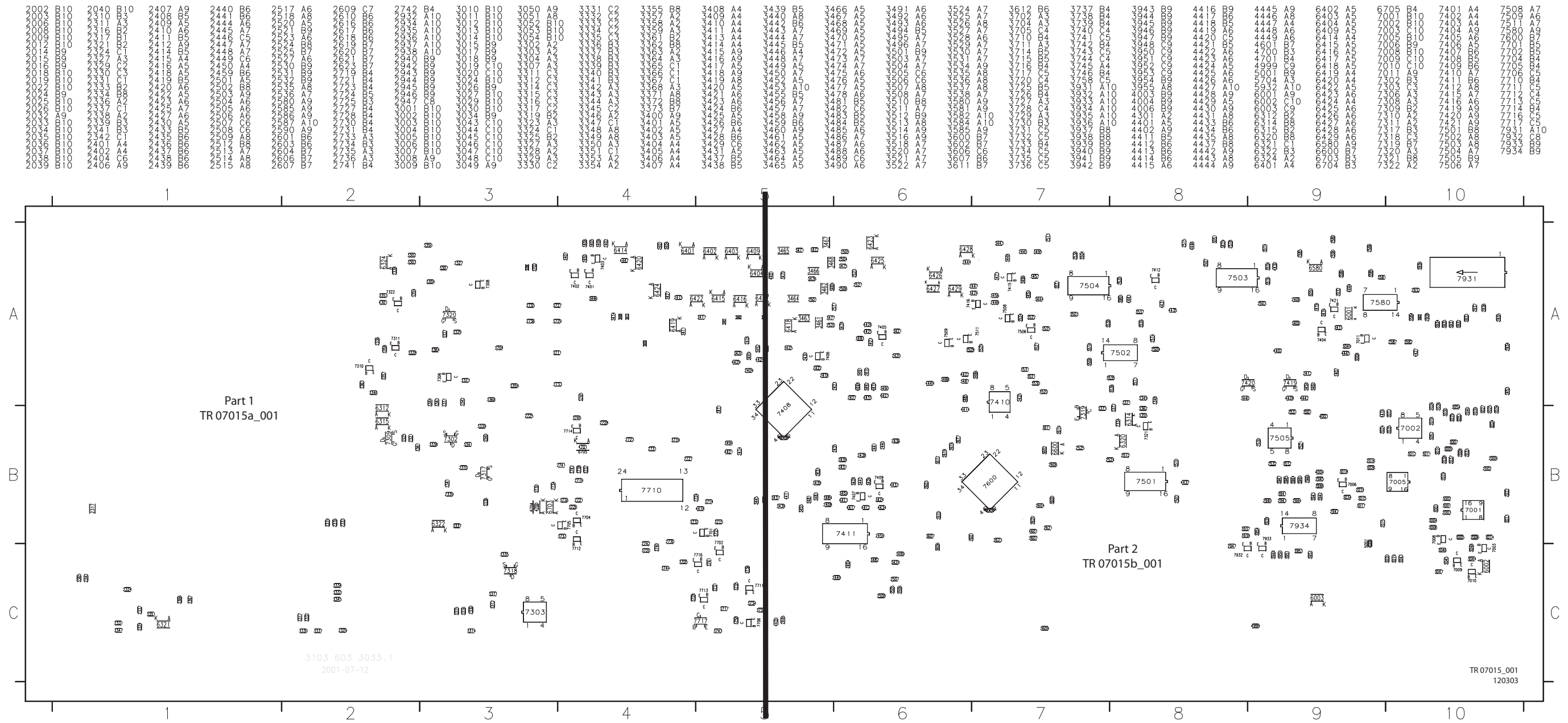
- 1001 A7
- 1900 B1
- 2001 A4
- 2002 A4
- 2003 A6
- 2004 A9
- 2005 A9
- 2006 A2
- 2007 B6
- 2008 B7
- 2009 C5
- 2010 C6
- 2011 C6
- 2012 E9
- 2013 D6
- 2014 D6
- 2015 D5
- 2016 D5
- 2018 D9
- 2019 E6
- 2020 E7
- 2022 B4
- 2023 F1
- 2024 B8
- 2025 D7
- 2026 D8
- 2029 F1
- 2031 D2
- 2032 F8
- 2033 B7
- 2034 D7
- 2035 B8
- 2036 D8
- 2037 B7
- 2038 B8
- 2039 D8
- 2040 D7
- 3001 A4
- 3002 A4
- 3003 A3
- 3004 B2
- 3005 B1
- 3006 B2
- 3007 B6
- 3008 A2
- 3009 A7
- 3010 A8
- 3011 B8
- 3012 B8
- 3013 B2
- 3014 C4
- 3015 D6
- 3017 D6
- 3018 D4
- 3019 D3
- 3020 E2
- 3024 C6
- 3026 E2
- 3027 C7
- 3029 D8
- 3030 D8
- 3034 E2
- 3035 E1
- 3039 F2
- 3041 F2
- 3043 F5
- 3044 C3
- 3045 C3
- 3046 C2
- 3047 D3
- 3048 C2
- 3049 F6
- 3050 F7
- 3051 F8
- 3052 A9
- 3053 C8
- 3054 C9
- 4003 F1
- 4004 F1
- 4006 A8
- 5001 A8
- 6001 A1
- 6002 B1
- 6003 F3
- 7001 A6
- 7002-A C9
- 7002-B E9
- 7003 B4
- 7005 D5
- 7006 E1
- 7008 C2
- 7009 C3
- 7010 C4
- 7011 F7
- F0001 E1
- F0002 E1
- F0003 D1
- F0005 D1
- F0007 D1
- F0009 D1
- F0011 C1
- F0012 C1
- F0014 C1
- F0016 C1
- F0021 A1
- F006 A8
- F007 A7
- F008 A7
- F009 A7
- F010 C9
- F011 E9
- I002 A5
- I003 A4
- I006 A4
- I008 B8
- I010 B5
- I012 C7
- I013 D6
- I014 E2
- I015 D4
- I018 E7
- I020 E1
- I021 F1
- I022 E2
- I028 F2
- I030 F1
- I032 E2
- I033 B6
- I036 E1
- I040 E1

Analog Board 603 3028: Audio Converter (DAC_ADC)

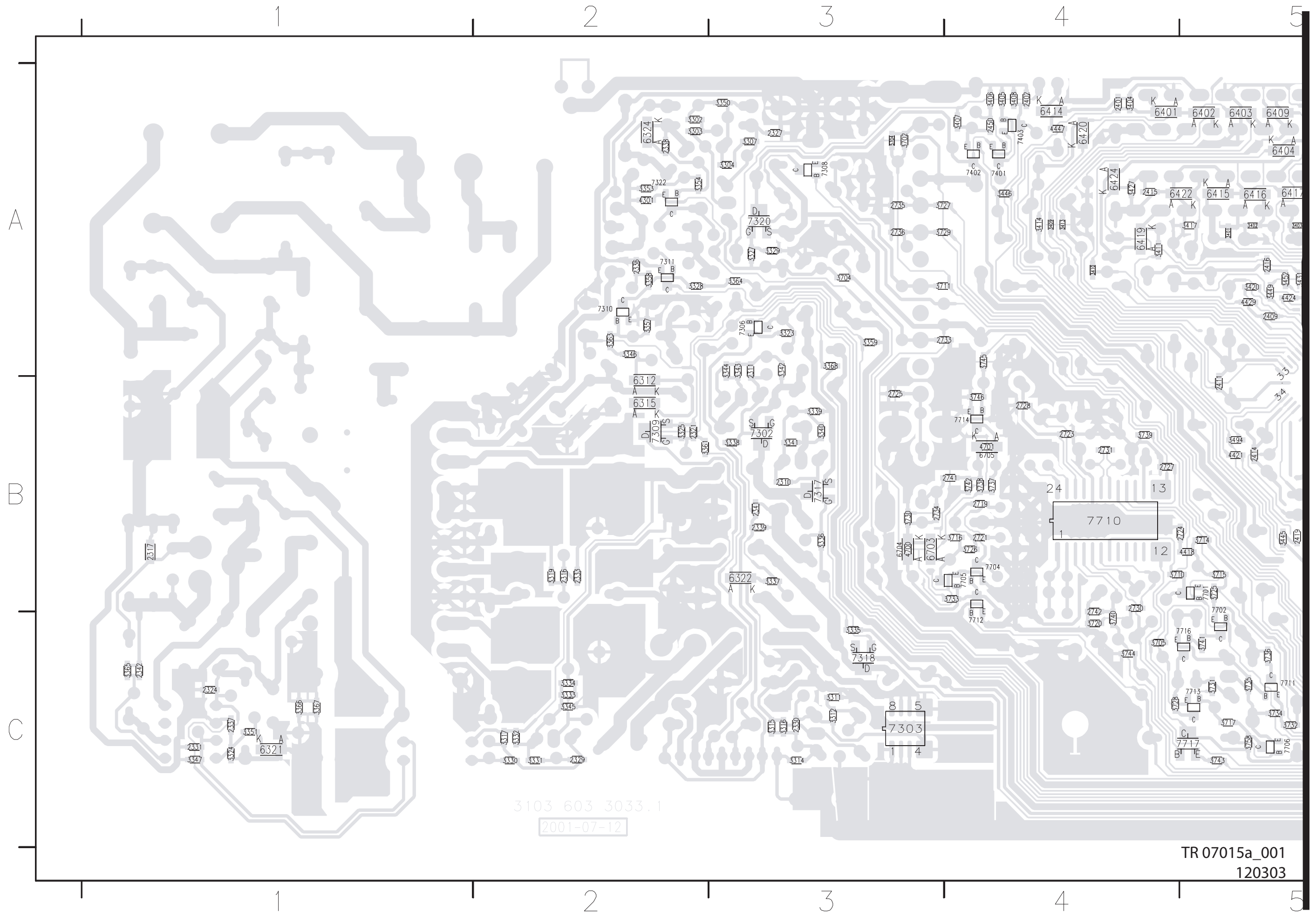


- 1001 H10
- 1900 C2
- 2000 H13
- 2001 H13
- 2002 B6
- 2003 B6
- 2004 B7
- 2006 B10
- 2007 B12
- 2008 B11
- 2009 B12
- 2010 C13
- 2011 B13
- 2012 C13
- 2013 E12
- 2014 F13
- 2016 B3
- 2017 C13
- 2018 E5
- 2019 E8
- 2020 E8
- 2021 E8
- 2023 D10
- 2025 D11
- 2026 E4
- 2027 E4
- 2028 E4
- 2030 E10
- 2032 E11
- 2033 E12
- 2035 F7
- 2036 F5
- 2037 F7
- 2038 F8
- 2041 F13
- 2042 G8
- 2043 G8
- 2045 F10
- 2047 F11
- 2048 H2
- 2049 B9
- 2050 I2
- 2051 E3
- 3001 B10
- 3004 B11
- 3005 C5
- 3006 C5
- 3008 B11
- 3009 C10
- 3010 B12
- 3011 B3
- 3012 E4
- 3013 C12
- 3014 E10
- 3015 B2
- 3016 C11
- 3017 D13
- 3018 F10
- 3019 E3
- 3020 E3
- 3021 E5
- 3022 E3
- 3023 E2
- 3024 E3
- 3025 A3
- 3026 F2
- 3027 E11
- 3028 F3
- 3029 A3
- 3030 E11
- 3031 A4
- 3032 E12
- 3033 F2
- 3034 F7
- 3035 F8
- 3036 F12
- 3039 F11
- 3040 G13
- 3042 H2
- 3043 H3
- 3044 H3
- 3045 A5
- 3047 I3
- 3049 A8
- 3051 B9
- 3052 B9
- 3053 I3
- 3054 D3
- 4000 H11
- 4001 I2
- 4002 I2
- 5001 H11
- 6003 B4
- 6004 D2
- 6005 C2
- 7001 C3
- 7003-A B13
- 7003-B E13
- 7004 B5
- 7005 A3
- 7006 A3
- 7007 F6
- 7008 G2
- 7009 A9
- 7010 A5
- F0001 F2
- F0002 F2
- F0003 F2
- F0005 F2
- F0007 E2
- F0009 E2
- F0011 E2
- F0012 E2
- F0014 D2
- F0016 D2
- F0021 C2
- F006 H11
- F007 H11
- F008 H10
- F009 H10
- F010 E14
- F011 B14
- I001 D3
- I002 C5
- I004 D5
- I005 D5
- I006 D5
- I007 D5
- I008 I1
- I009 H1
- I013 F7
- I014 G6
- I015 F6
- I018 G7
- I020 G2
- I021 H2
- I022 H2
- I023 D8
- I029 G6
- I030 I2
- I031 G6
- I032 G6
- I036 G1

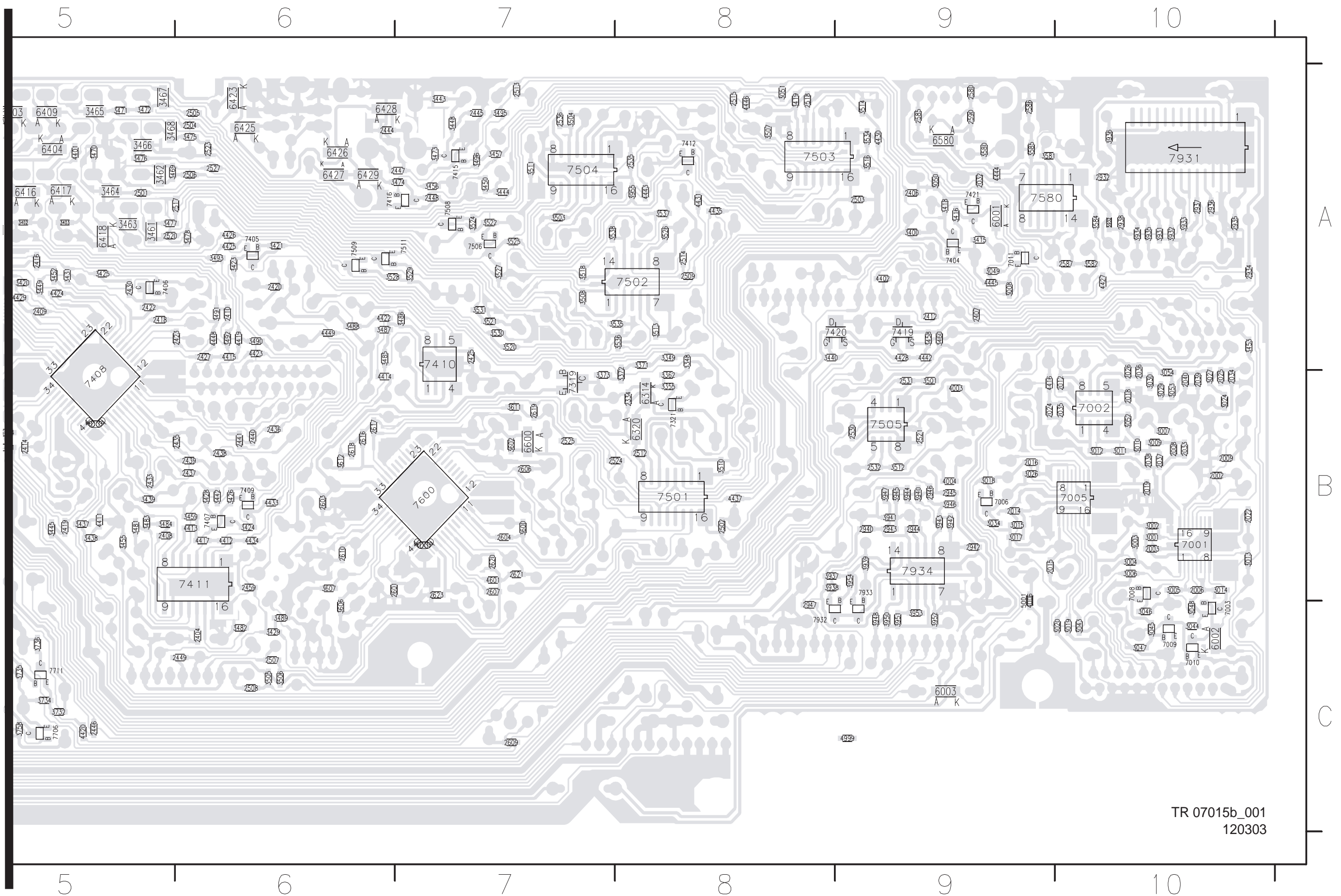
Layout Analog Board 603 3033 (Overview Bottom View)



Layout Analog Board 603 3033 (Part 1 Bottom View)

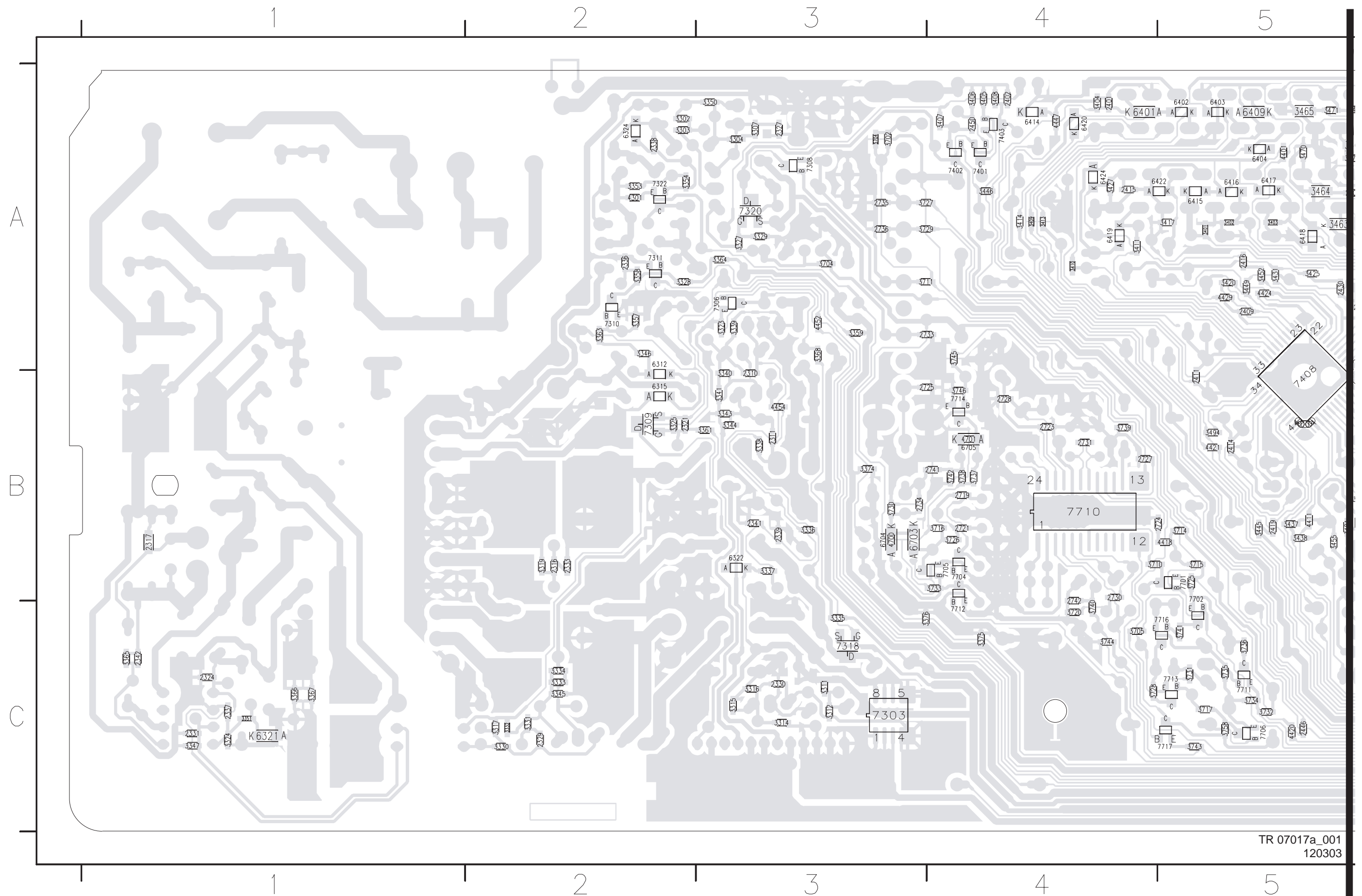


Layout Analog Board 603 3033 (Part 2 Bottom View)

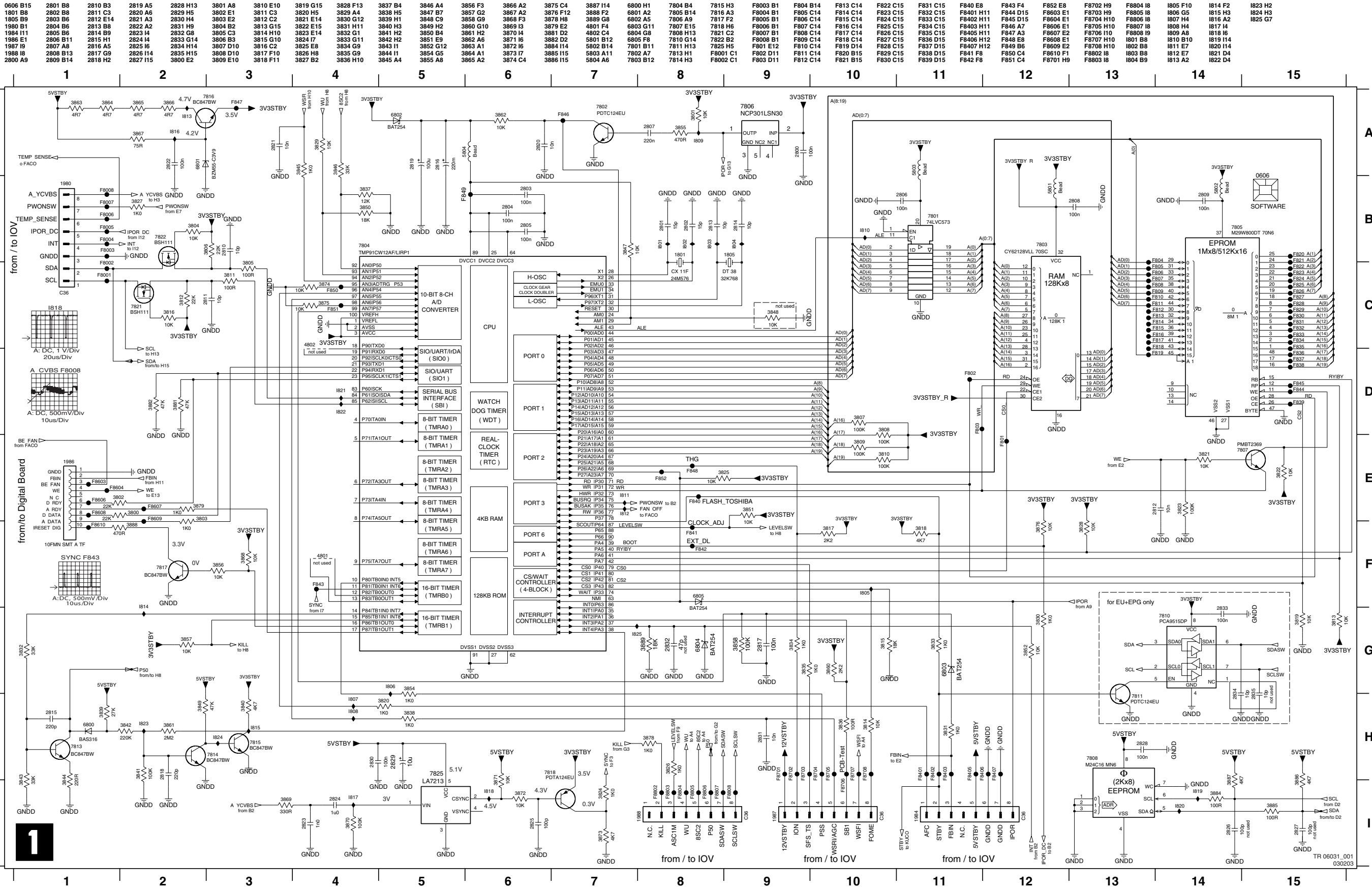


TR 07015b_001
120303

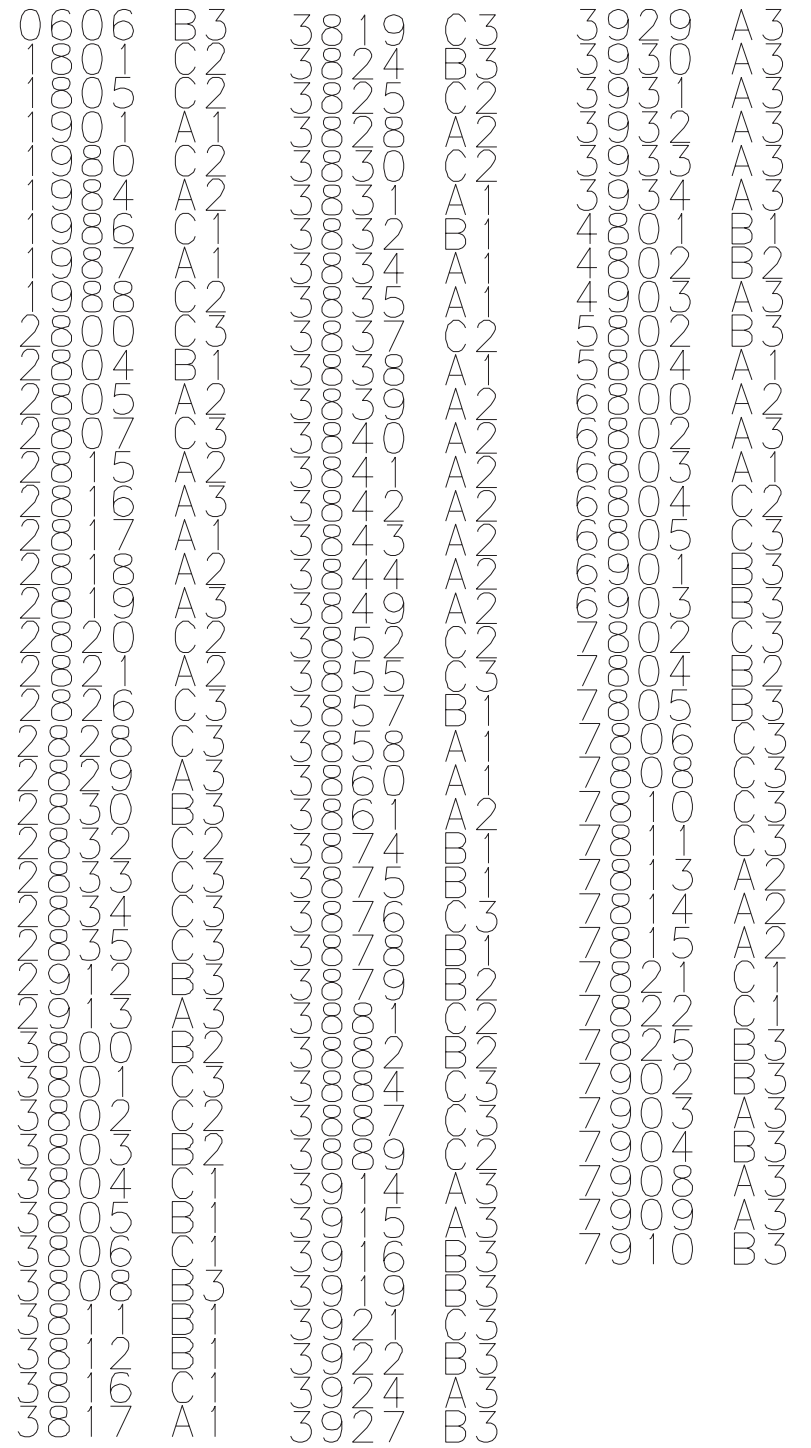
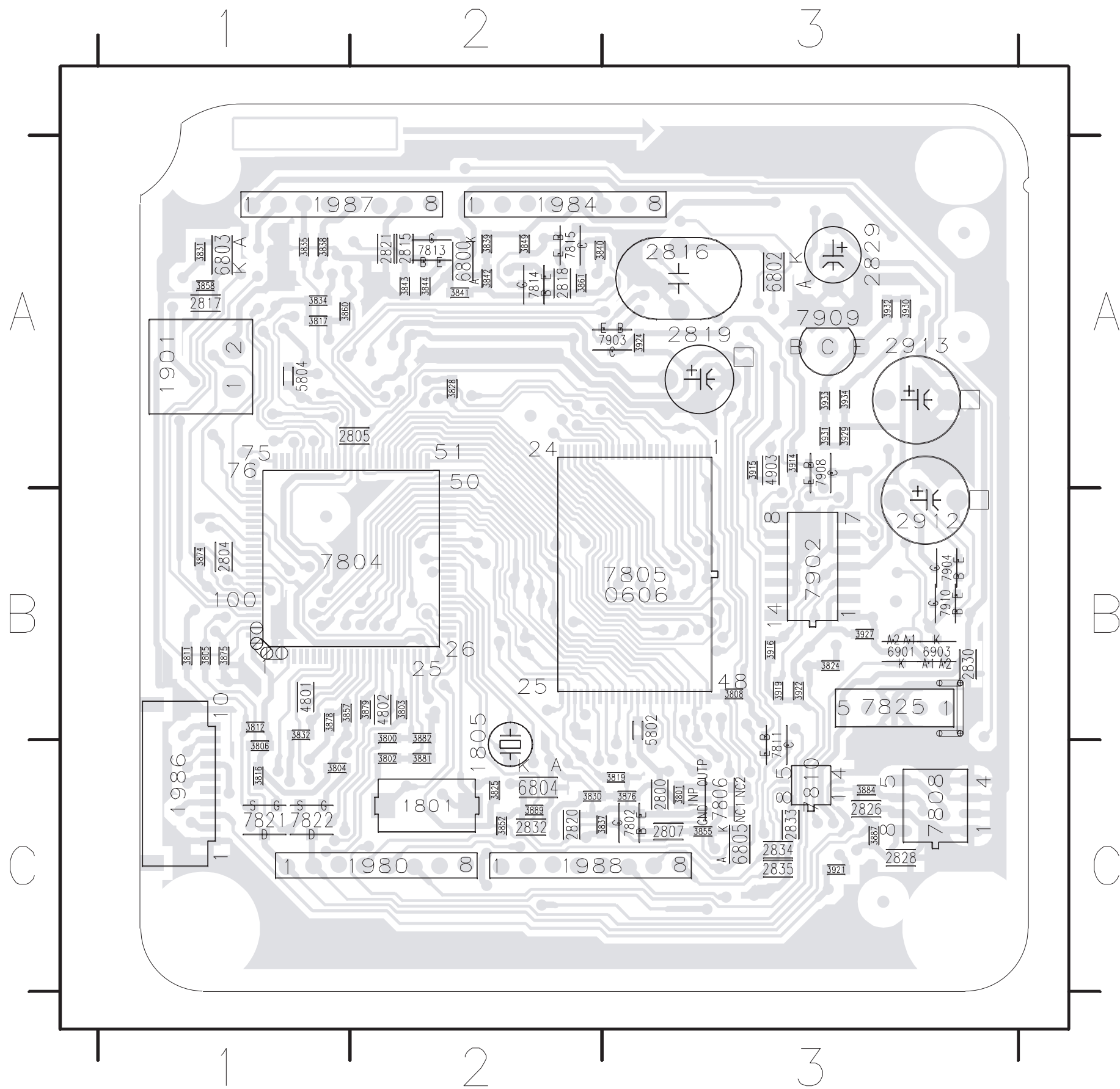
Layout Analog Board 603 3028 (Part 1 Bottom View)



UP Sub Board: Central Controller (CECO)

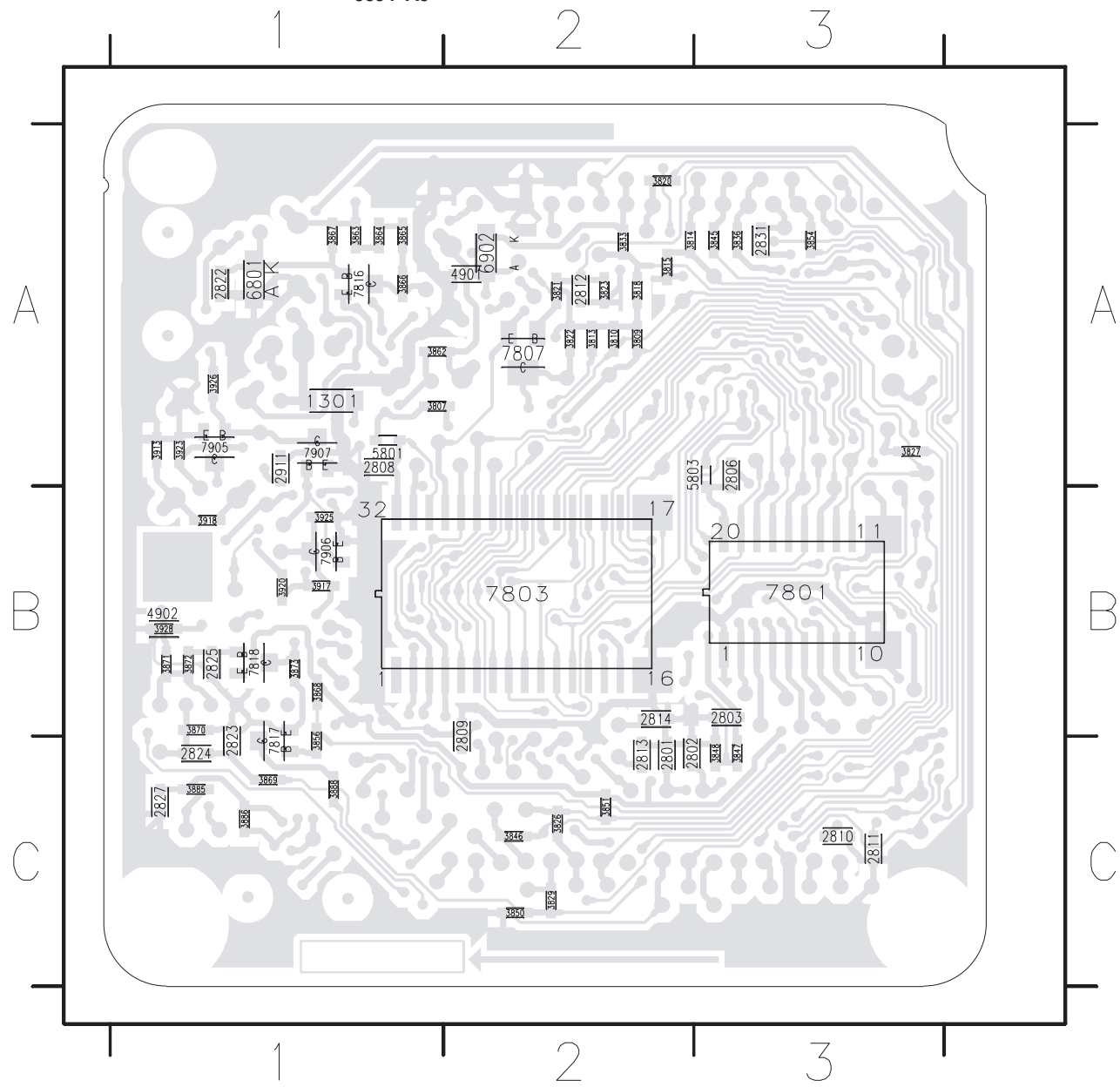


Layout UP Sub Board (Top View)

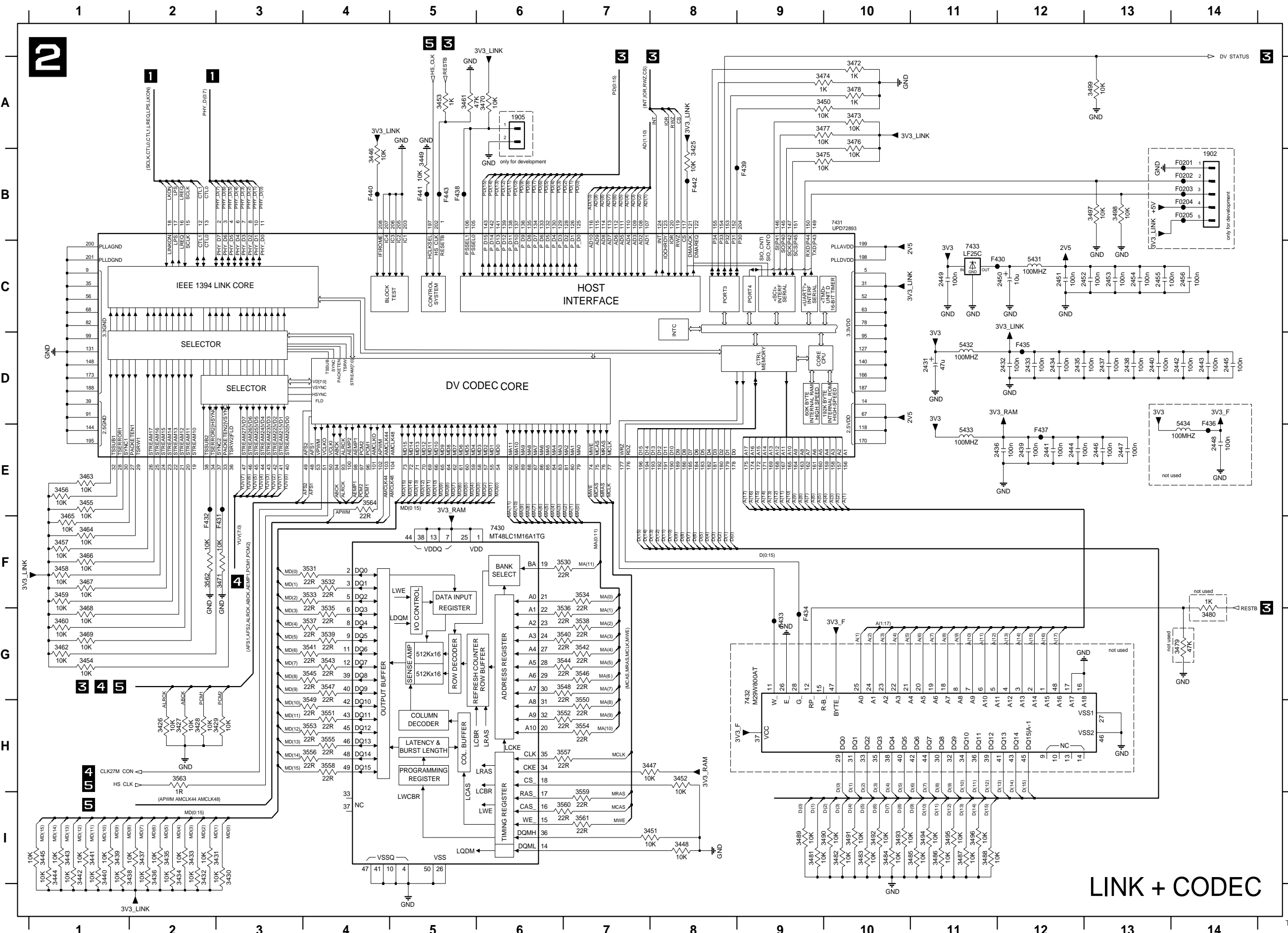


Layout UP Sub Board (Bottom View)

1301 A1	2824 C1	3822 A2	3856 C1	3886 C1	6801 A1
2801 C2	2825 B1	3823 A2	3862 A1	3888 C1	6902 A2
2802 C2	2827 C1	3826 C2	3863 A1	3913 A1	7801 B3
2803 B3	2831 A3	3827 A3	3864 A1	3917 B1	7803 B2
2806 A3	2911 A1	3829 C2	3865 A1	3918 B1	7807 A2
2808 A1	3807 A1	3833 A2	3866 A1	3920 B1	7816 A1
2809 B2	3809 A2	3836 A3	3867 A1	3923 A1	7817 C1
2810 C3	3810 A2	3845 A3	3868 B1	3925 B1	7818 B1
2811 C3	3813 A2	3846 C2	3869 C1	3926 A1	7905 A1
2812 A2	3814 A2	3847 C3	3870 B1	3928 B1	7906 B1
2813 C2	3815 A2	3848 C3	3871 B1	4901 A2	7907 A1
2814 B2	3818 A2	3850 C2	3872 B1	4902 B1	
2822 A1	3820 A2	3851 C2	3873 B1	5801 A1	
2823 C1	3821 A2	3854 A3	3885 C1	5803 A2	

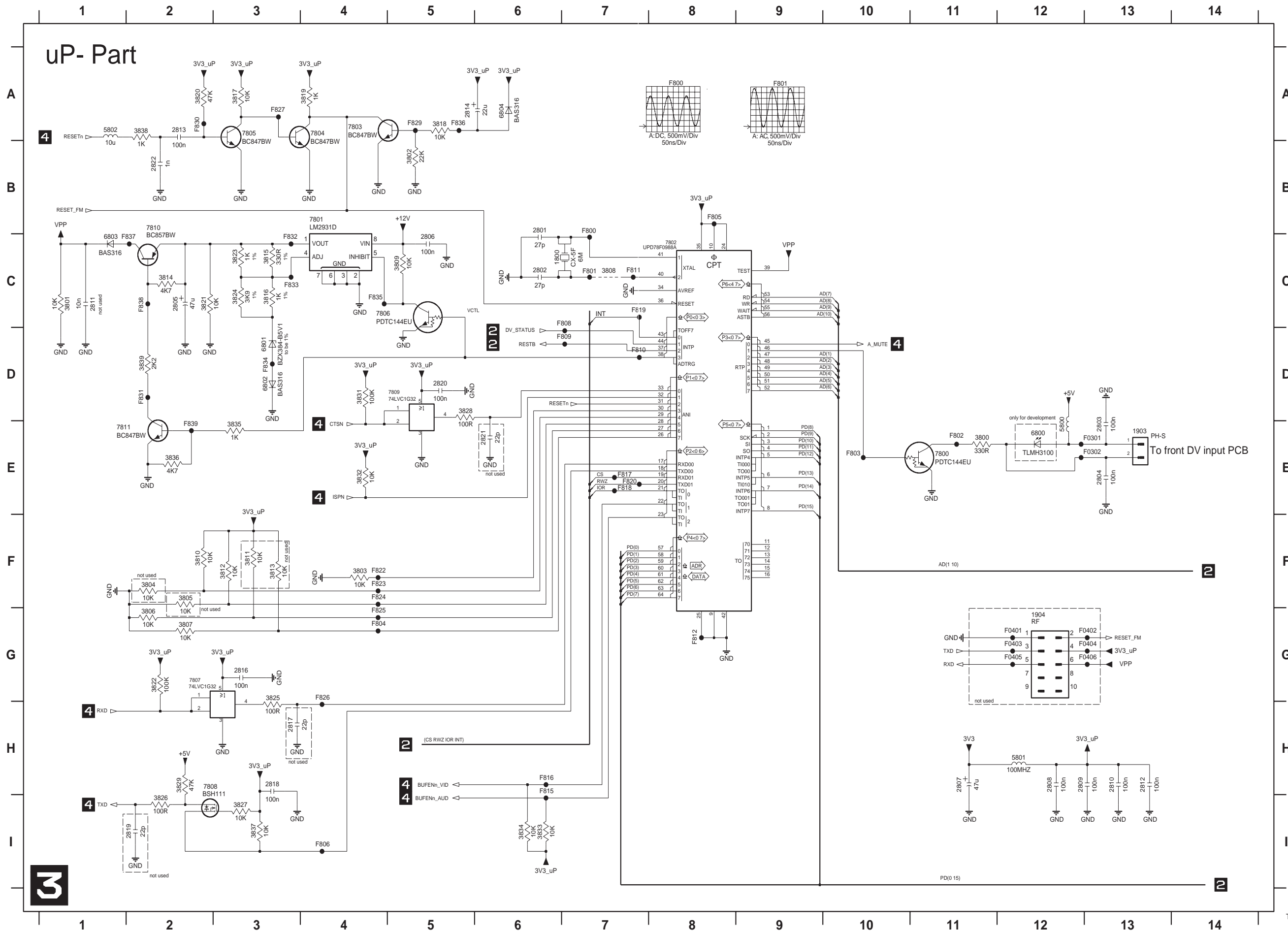


DVIO Board: Link+Codec



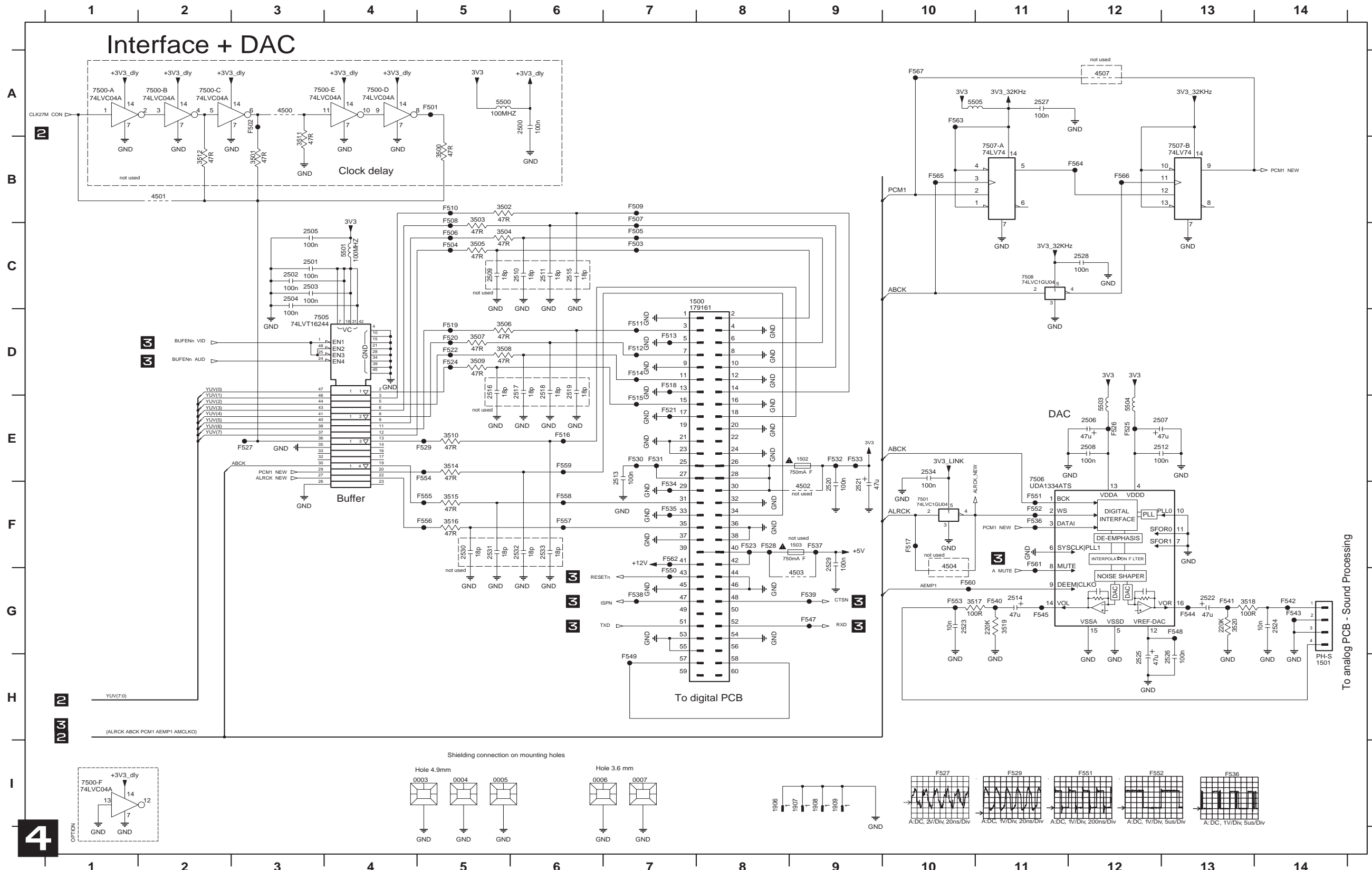
- 1902 B14
- 1905 A6
- 2431 D11
- 2432 D12
- 2433 D12
- 2434 D12
- 2435 D12
- 2436 E12
- 2437 D13
- 2438 D13
- 2439 E12
- 2440 D13
- 2441 E12
- 2442 D14
- 2443 D14
- 2444 E12
- 2445 D14
- 2446 E13
- 2447 E13
- 2448 E14
- 2449 C11
- 2450 C12
- 2451 C12
- 2452 C13
- 2453 C13
- 2454 C13
- 2455 C13
- 2456 C14
- 3425 A8
- 3426 H2
- 3427 H2
- 3428 H2
- 3429 H3
- 3430 I3
- 3431 I2
- 3432 I2
- 3433 I2
- 3434 I2
- 3435 I2
- 3436 I2
- 3437 I1
- 3438 I1
- 3439 I1
- 3440 I1
- 3441 I1
- 3442 I1
- 3443 I1
- 3444 I1
- 3445 I1
- 3446 B4
- 3447 H7
- 3448 B5
- 3449 B5
- 3450 A9
- 3451 B8
- 3452 H8
- 3453 A5
- 3454 G1
- 3455 E1
- 3456 E1
- 3457 G1
- 3458 F1
- 3459 F1
- 3460 G1
- 3461 A5
- 3462 G1
- 3463 G1
- 3470 A6
- 3471 F3
- 3472 A10
- 3473 A9
- 3474 A10
- 3475 G14
- 3476 A10
- 3477 A9
- 3478 A10
- 3479 G14
- 3480 G14
- 3481 I9
- 3482 I10
- 3483 I10
- 3484 I10
- 3485 I11
- 3486 I11
- 3487 I11
- 3488 I11
- 3489 I9
- 3490 I10
- 3491 I10
- 3492 I10
- 3493 I10
- 3494 I11
- 3495 I11
- 3496 I11
- 3497 B13
- 3498 B13
- 3499 A13
- 3530 F7
- 3531 F4
- 3532 F4
- 3533 F4
- 3534 F4
- 3535 G4
- 3536 G7
- 3537 G4
- 3538 G7
- 3539 G4
- 3540 G7
- 3541 G4
- 3542 G7
- 3543 G4
- 3544 G7
- 3545 G4
- 3546 G7
- 3547 G4
- 3548 G7
- 3549 H4
- 3550 H7
- 3551 H4
- 3552 H7
- 3553 H4
- 3554 H7
- 3555 H4
- 3556 H4
- 3557 H7
- 3558 H4
- 3559 I7
- 3560 I7
- 3561 I7
- 3562 F2
- 3563 H2
- 3564 E4
- 5431 C12
- 5432 D13
- 5433 E11
- 5434 E14
- 7430 F6
- 7431 B10
- 7432 H9
- 7433 C11
- F0201 B14
- F0202 B14
- F0203 B14
- F0204 B14
- F0205 B14
- F430 C12
- F431 F3
- F432 F2
- F433 G9
- F434 G9
- F435 D12
- F436 E12
- F437 E12
- F438 B5
- F439 B9
- F440 B4
- F441 B5
- F442 B8
- F443 B5

DVIO Board: uP-Part



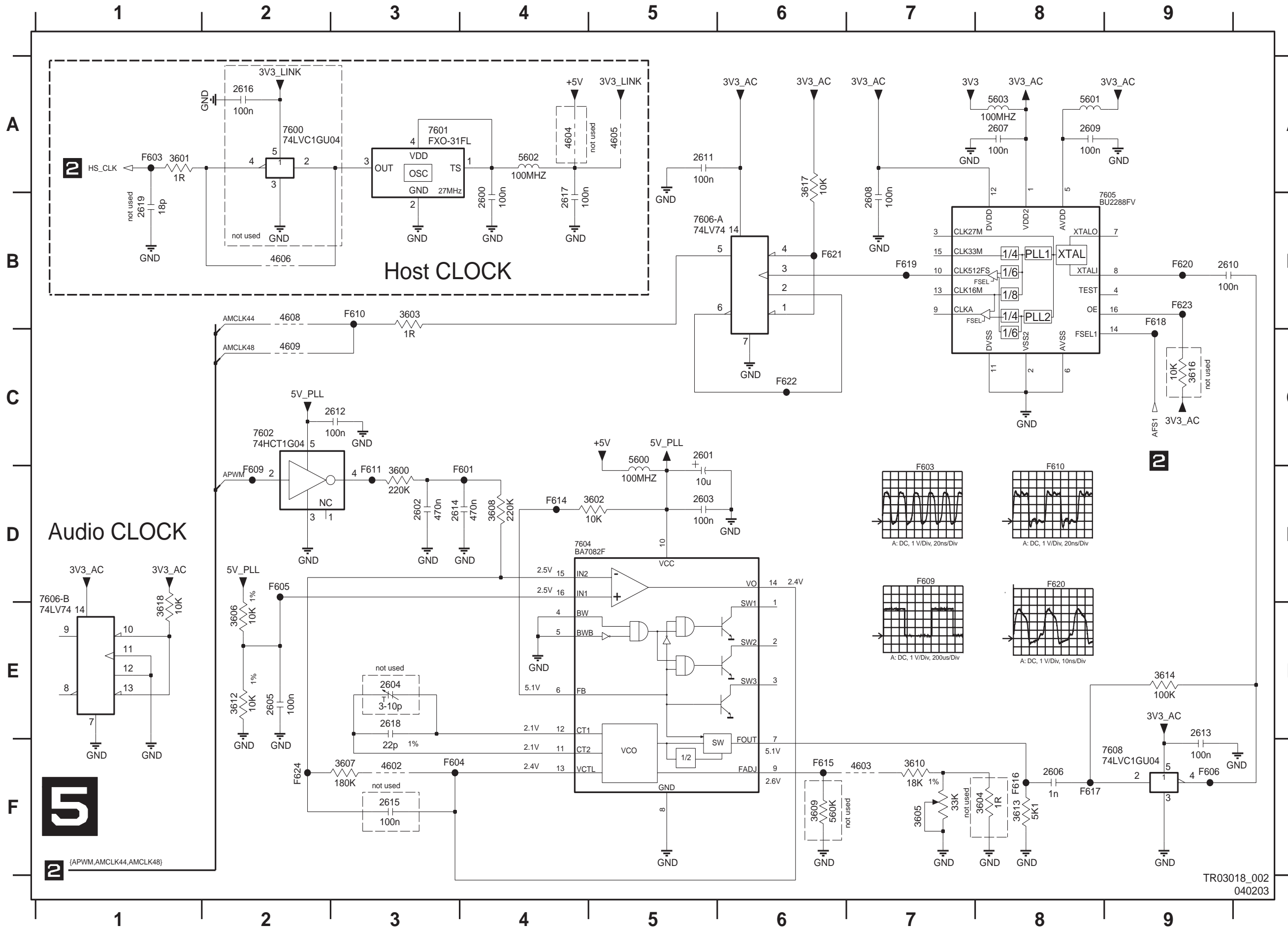
- 1800 C6
- 1903 E13
- 2801 G12
- 2801 B6
- 2802 C6
- 2803 E13
- 2804 E13
- 2805 C2
- 2806 C5
- 2807 H11
- 2808 H12
- 2809 H12
- 2810 H13
- 2811 C1
- 2812 H13
- 2813 A2
- 2814 A5
- 2816 G3
- 2817 H3
- 2818 H3
- 2819 I2
- 2820 D5
- 2821 E6
- 2822 B2
- 3800 E11
- 3801 C1
- 3802 B5
- 3803 F4
- 3804 F2
- 3805 F2
- 3806 G2
- 3807 G2
- 3808 C7
- 3809 C5
- 3810 F2
- 3811 F3
- 3812 F3
- 3813 F3
- 3814 C2
- 3815 C3
- 3816 C3
- 3817 A3
- 3818 A5
- 3819 A4
- 3820 A2
- 3821 C2
- 3822 G2
- 3823 C3
- 3824 C3
- 3825 G3
- 3826 I2
- 3827 I3
- 3828 D5
- 3829 H2
- 3831 D4
- 3832 E4
- 3833 I6
- 3834 I6
- 3835 E3
- 3836 E2
- 3837 I3
- 3838 A2
- 3839 D2
- 5800 E12
- 5801 H12
- 5802 A1
- 6800 E12
- 6801 D3
- 6802 D3
- 6803 C1
- 6804 A6
- 7800 E11
- 7801 B4
- 7802 C8
- 7803 A4
- 7804 A4
- 7805 A3
- 7806 C4
- 7807 G2
- 7808 H2
- 7809 D5
- 7810 B2
- 7811 E1
- F0301 E13
- F0302 E13
- F0401 G12
- F0402 G13
- F0403 G12
- F0404 G13
- F0405 G12
- F0406 G13
- F800 B7
- F801 C7
- F802 E11
- F803 E10
- F804 G4
- F805 B8
- F806 I4
- F808 C7
- F809 D7
- F810 D7
- F811 C7
- F812 G8
- F815 H6
- F816 H6
- F817 E7
- F818 E7
- F819 C7
- F820 E7
- F822 F4
- F823 F4
- F824 F4
- F825 G4
- F826 G4
- F827 A3
- F829 A5
- F830 A2
- F831 D2
- F832 C3
- F833 C3
- F834 D3
- F835 C4
- F836 A5
- F837 C2
- F838 C2
- F839 E2

DVIO Board: Interface+DAC



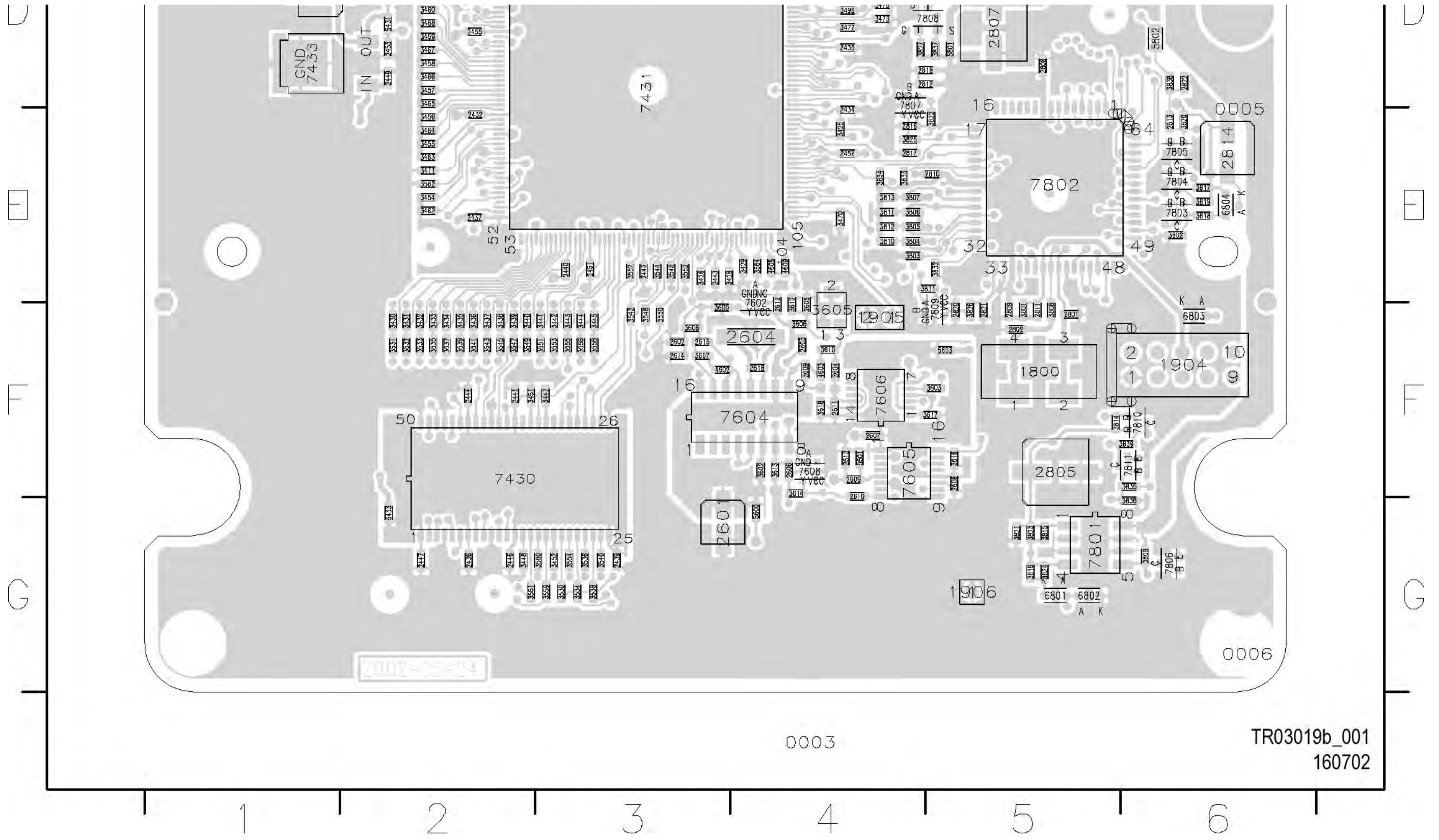
- 0003 I4
- 0004 I5
- 0005 I6
- 0006 I6
- 0007 I7
- 1500 C7
- 1501 H14
- 1502 E9
- 1503 F9
- 1906 I8
- 1907 I9
- 1908 I9
- 1909 I9
- 2500 A6
- 2501 C3
- 2502 C3
- 2503 C3
- 2504 C3
- 2505 C3
- 2506 E12
- 2507 E12
- 2508 E12
- 2509 C5
- 2510 C6
- 2511 C6
- 2512 E12
- 2513 E7
- 2514 G11
- 2515 C6
- 2516 D5
- 2517 D6
- 2518 D6
- 2519 D6
- 2520 F9
- 2521 F9
- 2522 G13
- 2523 G10
- 2524 G14
- 2525 H12
- 2526 H13
- 2527 A11
- 2528 C12
- 2529 F9
- 2530 F5
- 2531 F5
- 2532 F6
- 2533 F6
- 2534 E10
- 3500 B5
- 3501 B3
- 3502 B5
- 3503 B5
- 3504 C5
- 3505 C5
- 3506 D5
- 3507 D5
- 3508 D5
- 3509 D5
- 3510 E3
- 3511 B3
- 3512 B2
- 3514 E5
- 3515 F5
- 3516 F5
- 3517 G10
- 3518 G13
- 3519 G11
- 3520 G13
- 4500 A3
- 4501 B2
- 4502 F9
- 4503 G9
- 4504 G10
- 4507 A12
- 5500 A5
- 5501 C4
- 5503 E12
- 5504 E12
- 5505 A10
- 7500-A A1
- 7500-B A2
- 7500-C A2
- 7500-D A4
- 7500-E A3
- 7500-F I1
- 7501 F10
- 7505 D4
- 7506 E11
- 7507-A B11
- 7507-B B13
- 7508 C11
- F501 A5
- F502 A3
- F503 C7
- F504 C5
- F505 C7
- F506 C5
- F507 B7
- F508 B5
- F509 B7
- F510 B5
- F511 D7
- F512 D7
- F513 D7
- F514 D7
- F515 E7
- F516 E6
- F517 F10
- F518 D7
- F519 D5
- F520 D5
- F521 E7
- F522 D5
- F523 F8
- F524 D5
- F525 E12
- F526 E12
- F527 E3
- F528 F8
- F529 E5
- F530 E7
- F531 E7
- F532 E9
- F533 E9
- F534 F7
- F535 F7
- F536 F11
- F537 F9
- F538 G7
- F539 G9
- F540 G11
- F541 G13
- F542 G14
- F543 G13
- F544 G13
- F545 H7
- F546 H7
- F547 G9
- F548 G9
- F549 H7
- F550 G7
- F551 F11
- F552 F11
- F553 G10
- F554 E5
- F555 F5
- F556 F5
- F557 F6
- F558 F6
- F559 E6
- F560 G10
- F561 F11
- F562 F7
- F563 A10
- F564 B12
- F565 B10
- F566 B12
- F567 A10

DVIO Board: Clock

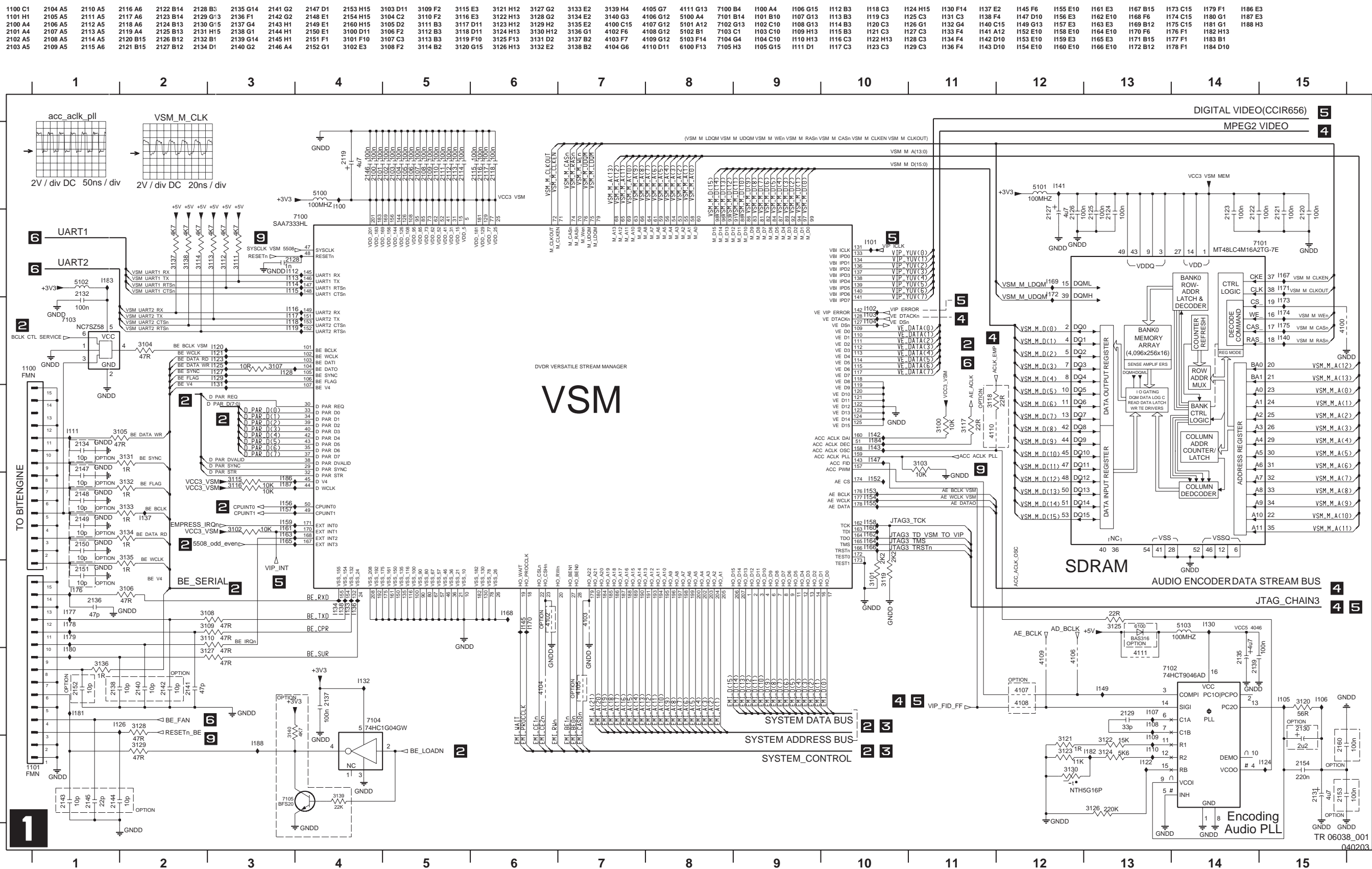


- 2600 B4
- 2601 C5
- 2602 D3
- 2603 D5
- 2604 E3
- 2605 E2
- 2606 F8
- 2607 A8
- 2608 B7
- 2609 A8
- 2610 B9
- 2611 A5
- 2612 C3
- 2613 E9
- 2614 D3
- 2615 F3
- 2616 A2
- 2617 B4
- 2618 E3
- 2619 B1
- 3600 D3
- 3601 A1
- 3602 D5
- 3603 B3
- 3604 F8
- 3605 F7
- 3606 E2
- 3607 F3
- 3608 D4
- 3609 F6
- 3610 F7
- 3612 E2
- 3613 F8
- 3614 E9
- 3616 C9
- 3617 A6
- 3618 E1
- 4602 F3
- 4603 F7
- 4604 A4
- 4605 A5
- 4606 B2
- 4608 B2
- 4609 C2
- 4600 C5
- 5601 A8
- 5602 A4
- 5603 A8
- 7600 A2
- 7601 A3
- 7602 C2
- 7604 D4
- 7605 B8
- 7606-A B5
- 7606-B D1
- 7608 F8
- F601 D4
- F603 A1
- F604 F3
- F605 D2
- F606 F9
- F609 D2
- F610 B3
- F611 D3
- F614 D4
- F615 F6
- F616 F8
- F617 F8
- F618 B9
- F619 B7
- F620 B9
- F621 B6
- F622 C6
- F623 B9
- F624 F2

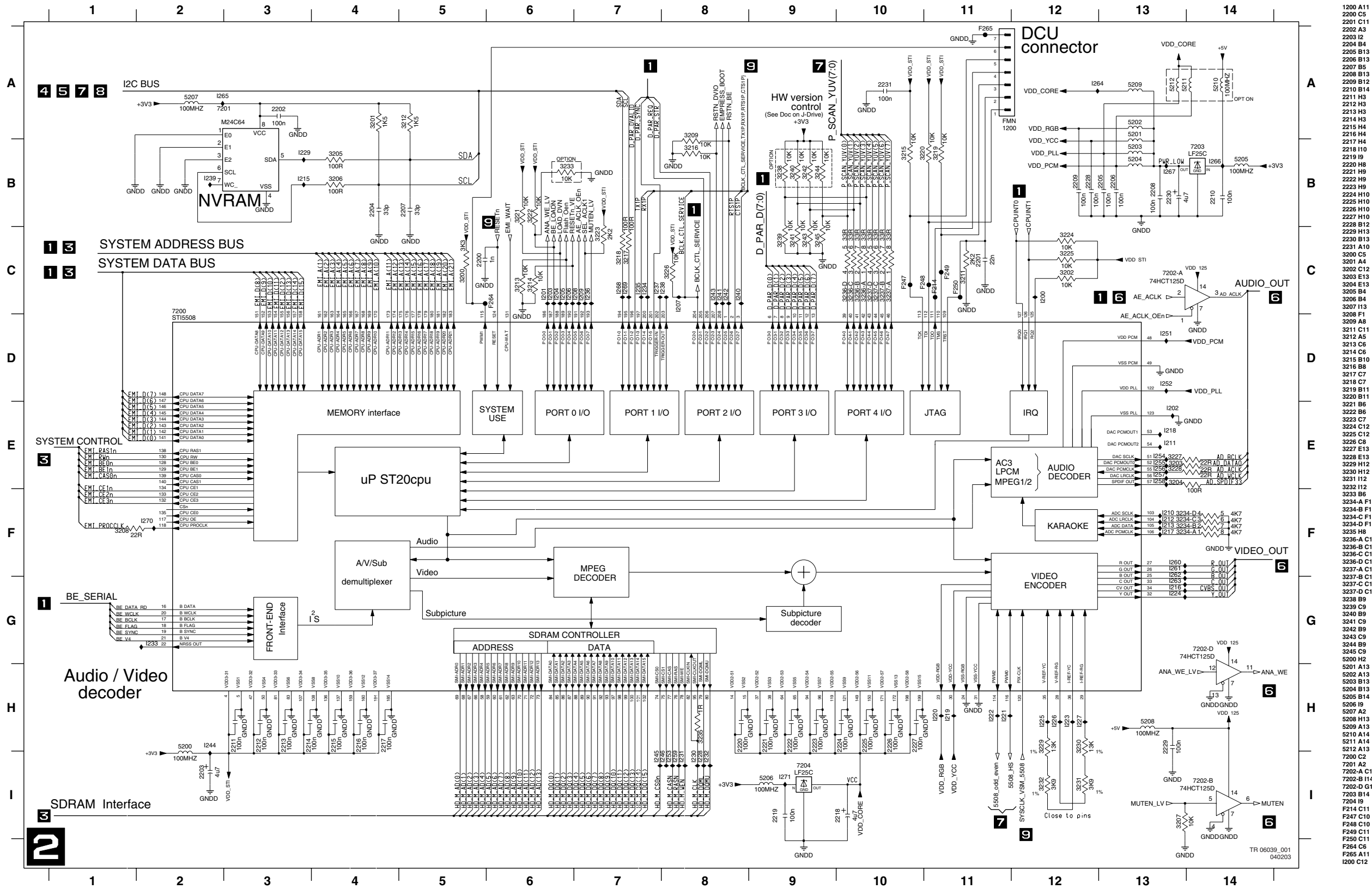
Layout DVIO Board (Part 2 Top View)



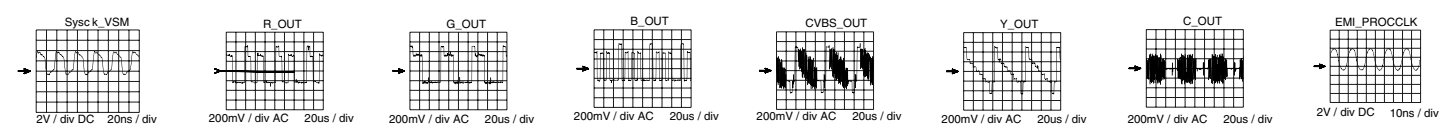
Digital Board 1.5: VSM, Buffer Memory and Bit Engine Interface



Digital Board 1.5: AV Decoder STI5519

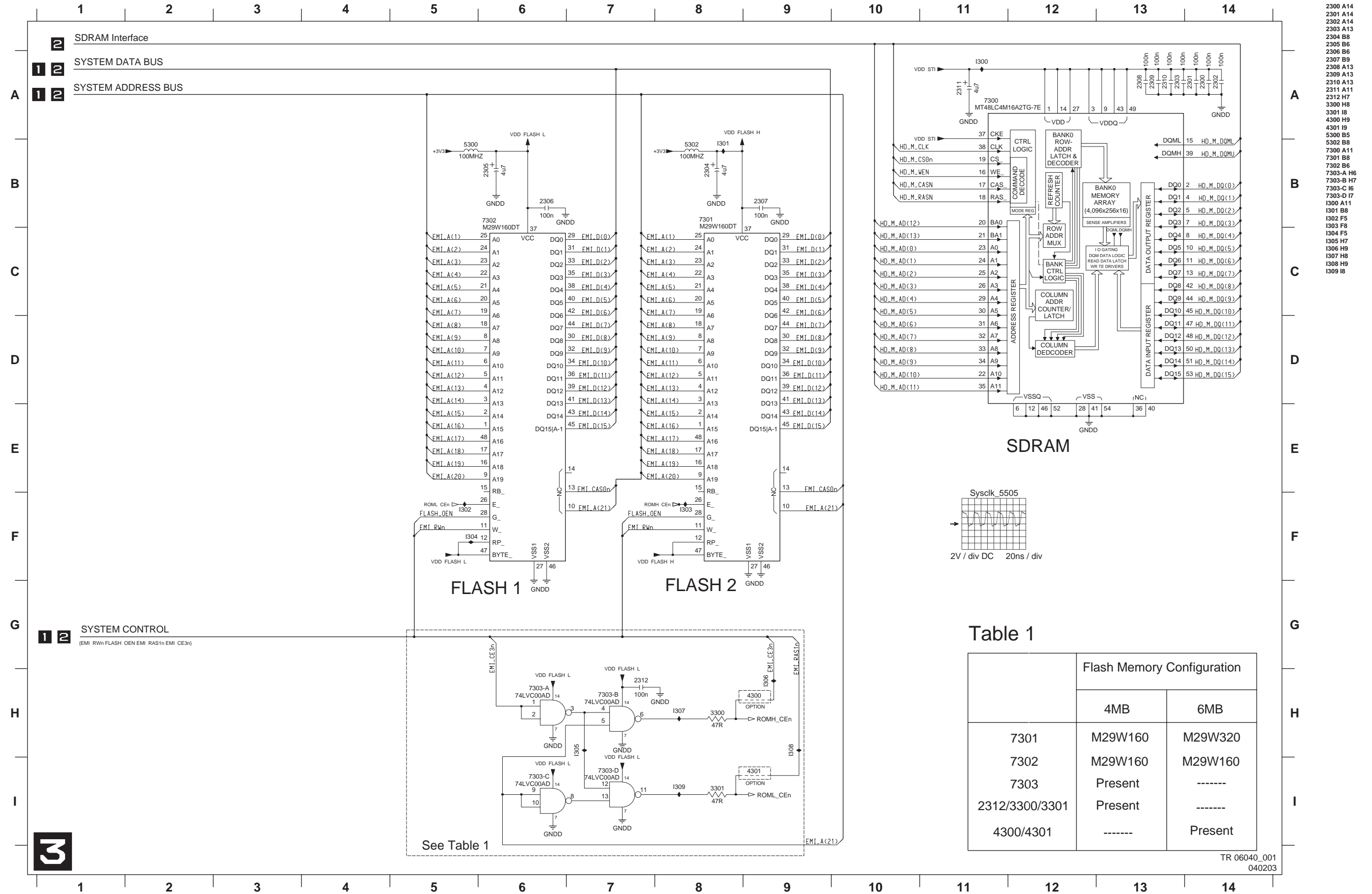


- 1200 A11
- 2200 C5
- 2301 C11
- 2202 A3
- 2203 I2
- 2204 B4
- 2205 B13
- 2206 B13
- 2207 B5
- 2208 B13
- 2209 B12
- 2210 B14
- 2211 H3
- 2212 H3
- 2213 H3
- 2214 H3
- 2215 H4
- 2217 H4
- 2218 I10
- 2219 I9
- 2220 H8
- 2221 H9
- 2222 H8
- 2223 H8
- 2224 H10
- 2225 H10
- 2226 H10
- 2227 H10
- 2228 B12
- 2229 H13
- 2230 B13
- 2231 A10
- 3200 C5
- 3201 A4
- 3202 C12
- 3203 I3
- 3204 E13
- 3205 B4
- 3206 B4
- 3207 I13
- 3208 F1
- 3209 A8
- 3211 C11
- 3212 A5
- 3213 C6
- 3214 C6
- 3215 B10
- 3216 B8
- 3217 C7
- 3218 C7
- 3219 B11
- 3220 B11
- 3221 B6
- 3222 B6
- 3223 C7
- 3224 C12
- 3225 C12
- 3226 C8
- 3227 E13
- 3228 E13
- 3229 H12
- 3230 H12
- 3231 I12
- 3232 H2
- 3233 B5
- 3234-A F13
- 3234-B F13
- 3234-C F13
- 3234-D F13
- 3235 H8
- 3236-A C10
- 3236-B C10
- 3236-C C10
- 3236-D C10
- 3237-A C10
- 3237-B C10
- 3237-C C10
- 3237-D C10
- 3238 B9
- 3239 C9
- 3240 B9
- 3241 C9
- 3242 B9
- 3243 C9
- 3244 B9
- 3245 C9
- 5200 H2
- 5201 A13
- 5202 A13
- 5203 B13
- 5204 B13
- 5205 B14
- 5206 I9
- 5207 A2
- 5208 H13
- 5209 A13
- 5210 A14
- 5211 A14
- 5212 A13
- 7200 C2
- 7201 A2
- 7202-A C13
- 7202-B H14
- 7202-D G14
- 7203 B14
- 7204 I9
- F14 C11
- F247 C10
- F248 C10
- F249 C11
- F250 C11
- F264 C6
- F265 A11
- I200 C12
- I201 C6
- I202 E13
- I203 C6
- I204 C6
- I205 C6
- I206 C6
- I207 C8
- I208 C7
- I209 C7
- I210 F13
- I211 E13
- I212 F13
- I213 F13
- I214 H3
- I215 B3
- I216 G13
- I217 F13
- I218 E13
- I219 H11
- I220 H11
- I221 H11
- I222 H12
- I223 H12
- I224 G13
- I225 H12
- I226 H12
- I227 H12
- I228 I8
- I229 B3
- I230 I8
- I231 I8
- I232 I8
- I233 G2
- I234 C7
- I235 C7
- I236 C7
- I237 C7
- I238 C8
- I239 B2
- I240 C8
- I241 C8
- I242 C8
- I243 C8
- I244 H2
- I245 I7
- I246 I8
- I251 D13
- I252 D13
- I253 I8
- I254 E13
- I255 E13
- I256 E13
- I257 E13
- I258 E13
- I259 I8
- I260 F13
- I261 F13
- I262 F13
- I263 G13
- I264 A2
- I265 A2
- I266 B14
- I267 B13
- I268 C7
- I269 C7
- I270 F2
- I271 I9



TR 06039_001
040203

Digital Board 1.5: AV Decoder Memory



- 2300 A14
- 2301 A14
- 2302 A14
- 2303 A13
- 2304 B8
- 2305 B6
- 2306 B6
- 2307 B9
- 2308 A13
- 2309 A13
- 2310 A13
- 2311 A11
- 2312 H7
- 3300 H8
- 3301 I8
- 4300 H9
- 4301 I9
- 5300 B5
- 5302 B8
- 7300 A11
- 7301 B8
- 7302 B6
- 7303-A H6
- 7303-B H7
- 7303-C I6
- 7303-D I7
- I300 A11
- I301 B8
- I302 F5
- I303 F8
- I304 F5
- I305 H7
- I306 H9
- I307 H8
- I308 H9
- I309 I8

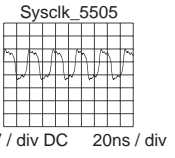
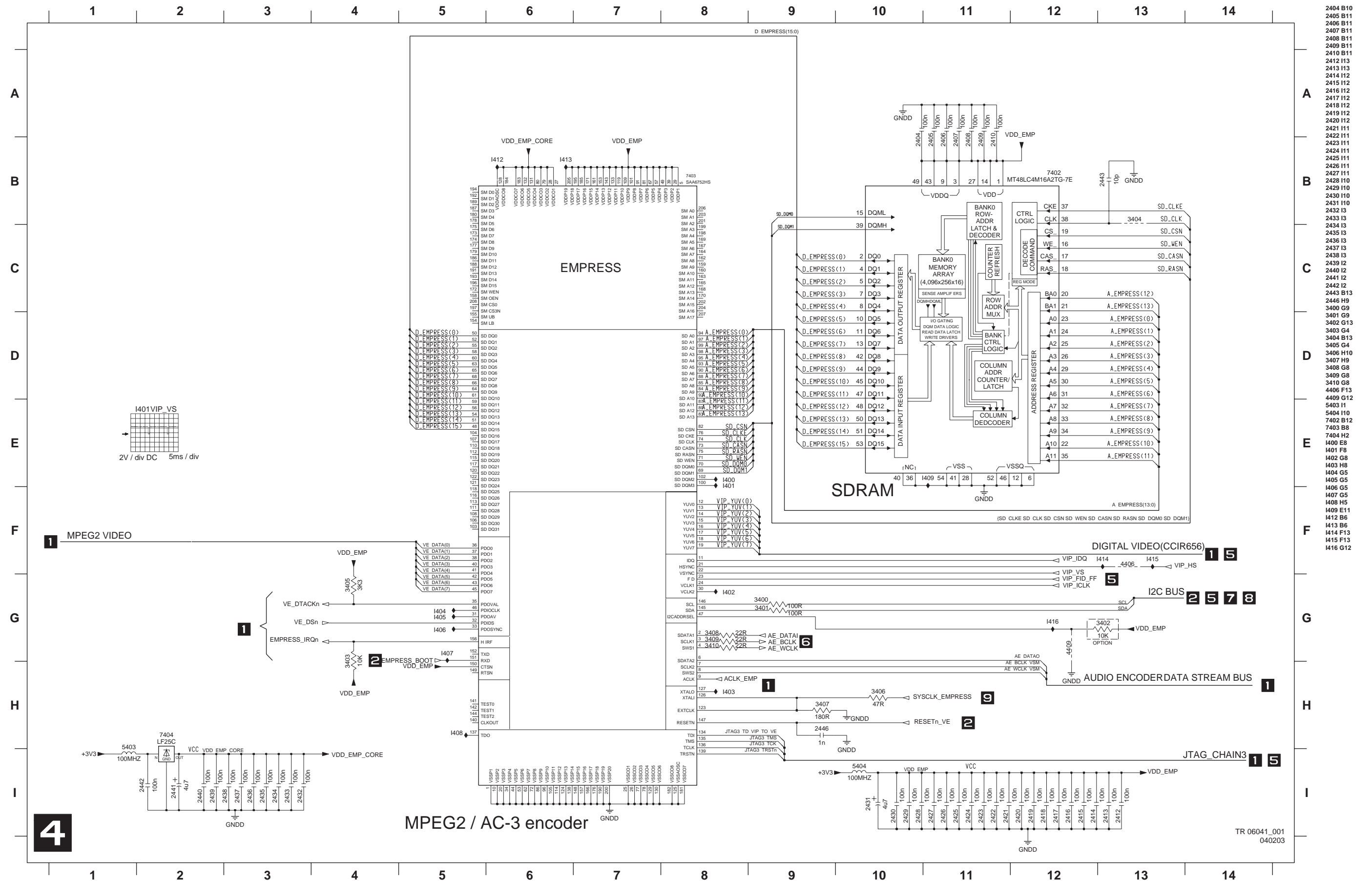


Table 1

	Flash Memory Configuration	
	4MB	6MB
7301	M29W160	M29W320
7302	M29W160	M29W160
7303	Present	-----
2312/3300/3301	Present	-----
4300/4301	-----	Present

Digital Board 1.5: Video Encoder, Empress

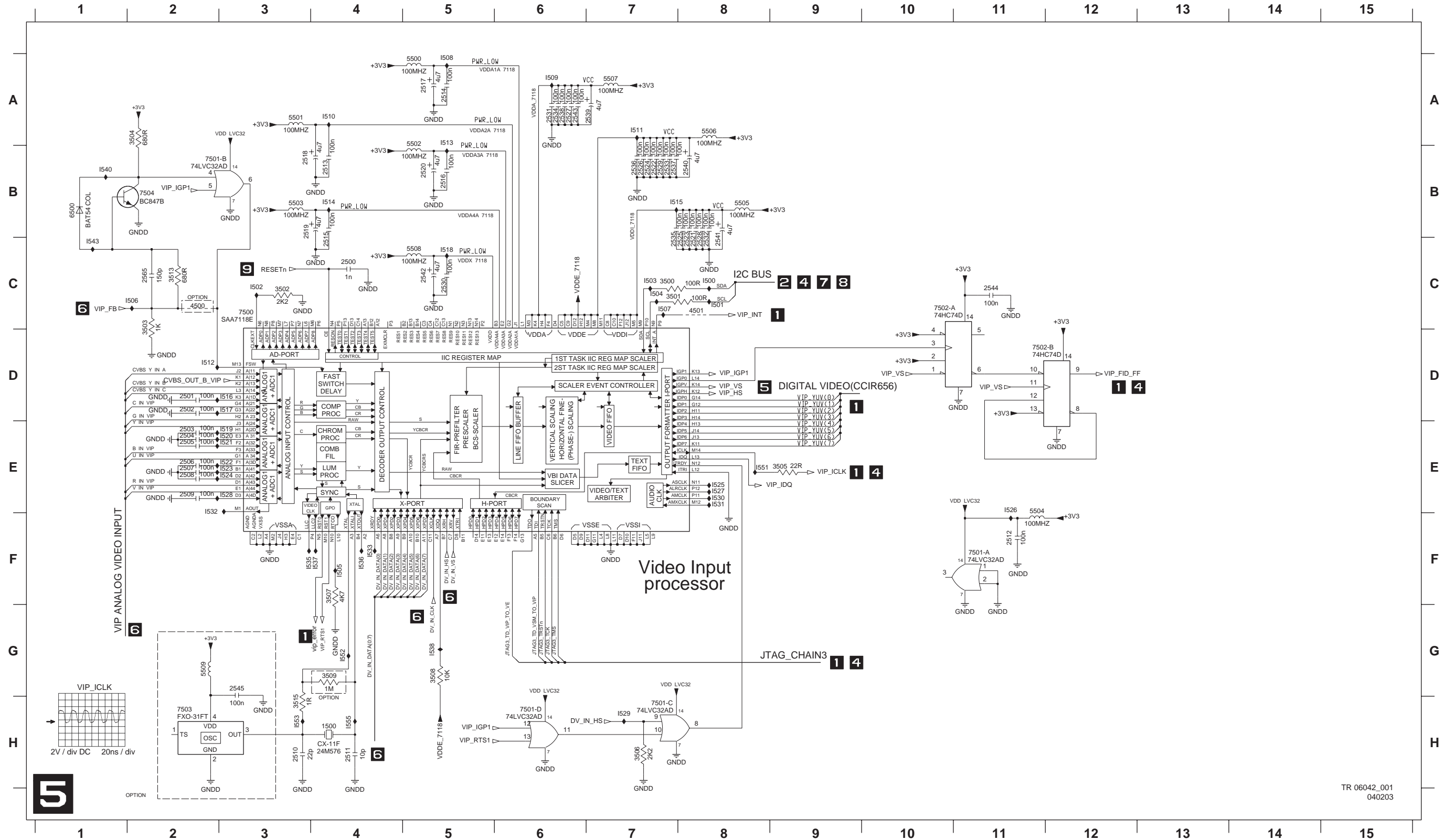


4

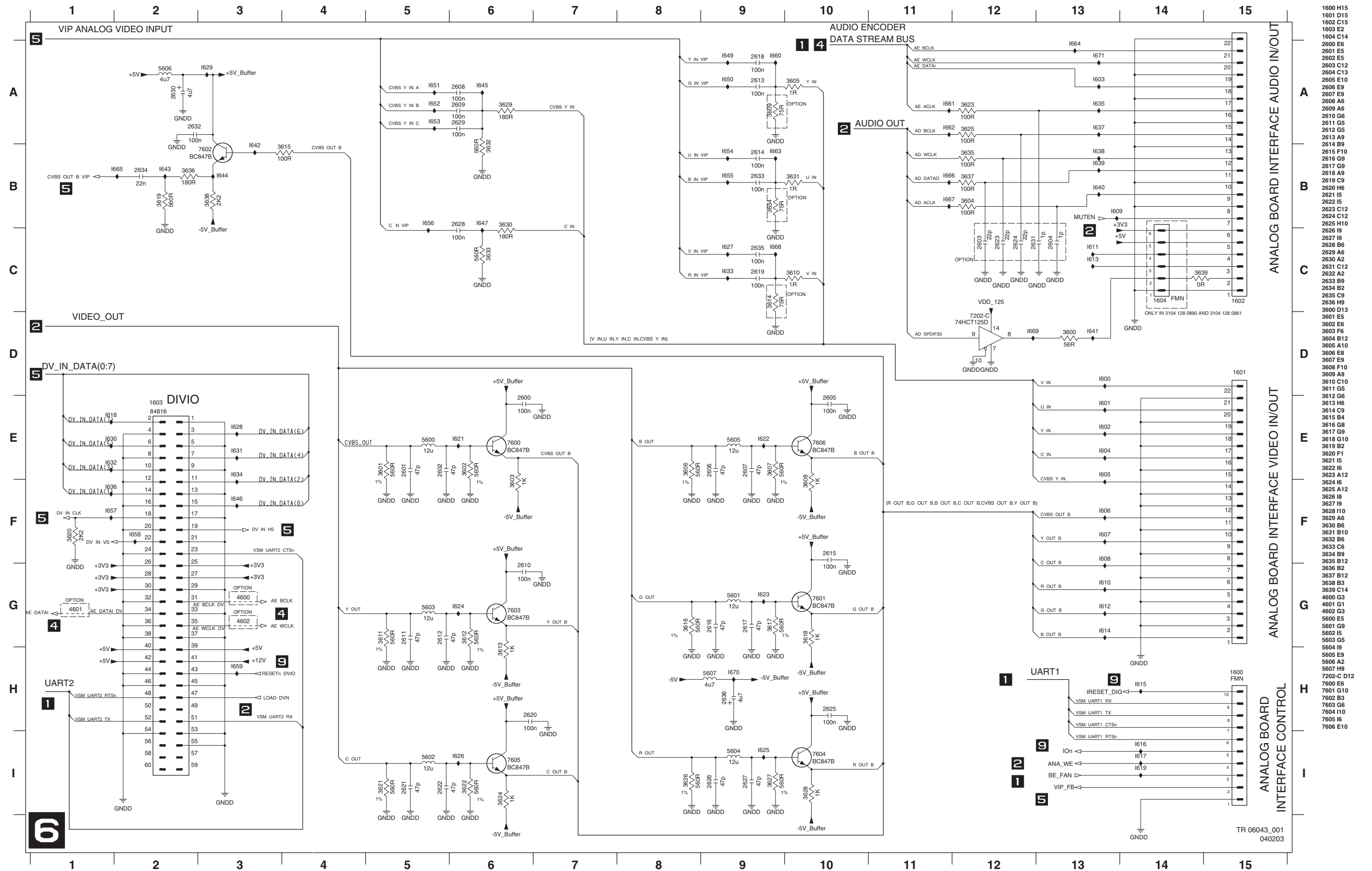
TR 06041_001
040203

Digital Board 1.5: VIP CVBS Y/C Video Input

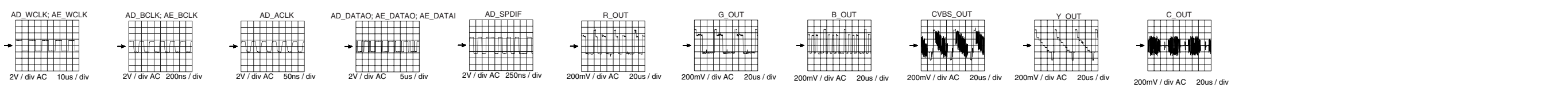
1500 H4	2504 E2	2509 E2	2514 A5	2519 B3	2524 B7	2529 B7	2534 A6	2539 A7	2544 C11	3502 C3	3507 F4	4500 C2	5503 B3	5508 C5	7501-B B2	7503 H2	I503 C7	I508 A5	I513 A5	I518 C5	I523 E3	I528 E3	I533 F4	I540 B1	I555 H4
2500 C4	2505 E2	2510 H3	2515 C4	2520 B5	2525 C8	2530 C5	2535 C7	2540 B8	2545 G3	3503 C2	3508 G5	4501 C8	5504 F11	5509 G2	7501-C H7	7504 B2	I504 C7	I509 A6	I514 B4	I519 E3	I524 E3	I529 H7	I535 F4	I543 C1	
2501 D2	2506 E2	2511 H4	2516 B5	2521 C8	2526 B7	2531 A6	2536 B7	2541 C8	2546 C2	3504 A2	3509 G4	4500 A5	5505 B8	5500 B1	7501-D H6	7504 C8	I505 F4	I510 A4	I515 B7	I520 E3	I525 E8	I530 E8	I536 F4	I543 C1	
2502 D2	2507 E2	2512 F11	2517 A5	2522 B7	2527 A6	2532 C8	2537 B7	2542 C5	3500 C7	3505 E9	3513 C2	4501 A3	5506 A8	7500 C3	7502-A C10	I501 C8	I506 C2	I511 A7	I516 D3	I521 E3	I526 E11	I531 E8	I537 F4	I545 G4	
2503 E2	2508 E2	2513 B4	2518 B3	2523 C8	2528 C8	2533 B7	2538 A6	2543 A6	3501 C7	3506 H7	3515 H3	4502 B5	5507 A7	7501-A F11	7502-B D11	I502 C3	I507 C7	I512 D2	I517 D3	I522 E3	I527 E8	I532 F2	I538 G5	I545 H3	



Digital Board 1.5: Analog Board Cons. Video In / Output

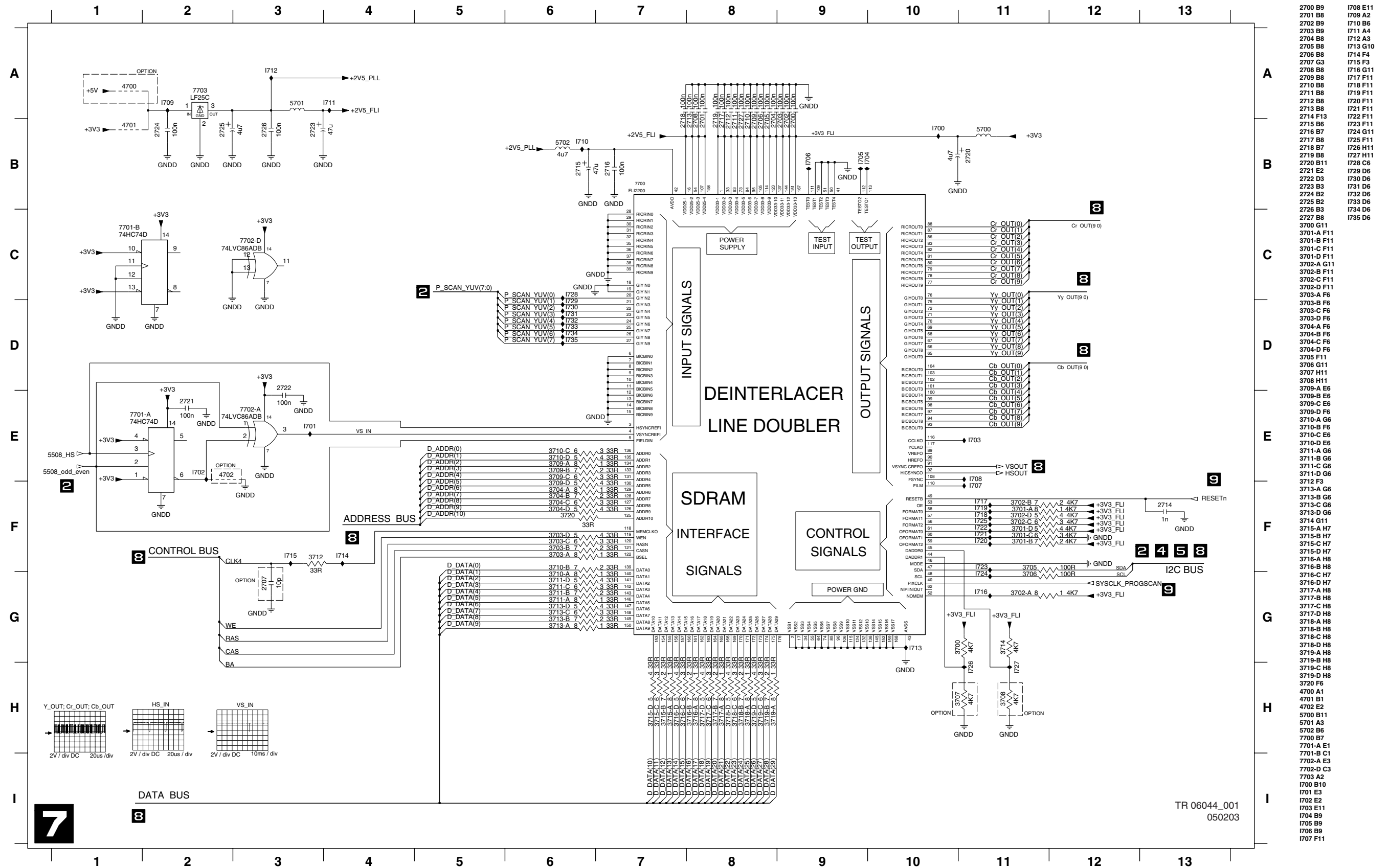


- 1600 H15
- 1601 D15
- 1602 C15
- 1603 E2
- 1604 C14
- 2600 E6
- 2601 E5
- 2602 E5
- 2603 C12
- 2604 C13
- 2605 E10
- 2606 E9
- 2607 E9
- 2608 A6
- 2609 A5
- 2610 G6
- 2611 G5
- 2612 G5
- 2613 A9
- 2614 B9
- 2615 F10
- 2616 G9
- 2617 G9
- 2618 A9
- 2619 C9
- 2620 H6
- 2621 I5
- 2622 I5
- 2623 C12
- 2624 C12
- 2625 H10
- 2626 I9
- 2627 I9
- 2628 B6
- 2629 A5
- 2630 A2
- 2631 C12
- 2632 A2
- 2633 B9
- 2634 B2
- 2635 C9
- 2636 H9
- 2637 D13
- 3601 E5
- 3602 E6
- 3603 F6
- 3604 B12
- 3605 A10
- 3606 E9
- 3607 E9
- 3608 F10
- 3609 A9
- 3610 C10
- 3611 G5
- 3612 G6
- 3613 H6
- 3614 C9
- 3615 B4
- 3616 G8
- 3617 G9
- 3618 G10
- 3619 B2
- 3620 F1
- 3621 I5
- 3622 I6
- 3623 A12
- 3624 I6
- 3625 A12
- 3626 I8
- 3627 I9
- 3628 I10
- 3629 A6
- 3630 B6
- 3631 B10
- 3632 B6
- 3633 C5
- 3634 B9
- 3635 B12
- 3636 B2
- 3637 B12
- 3638 B3
- 3639 C14
- 4600 G3
- 4601 G1
- 4602 G3
- 5600 E5
- 5601 G9
- 5602 I5
- 5603 G5
- 5604 I9
- 5605 E9
- 5606 A2
- 5607 H9
- 7202-C D12
- 7600 E6
- 7601 G10
- 7602 B3
- 7603 G6
- 7604 I10
- 7605 I6
- 7606 E10



TR 06043_001
040203

Digital Board 1.5: Progressive Scan

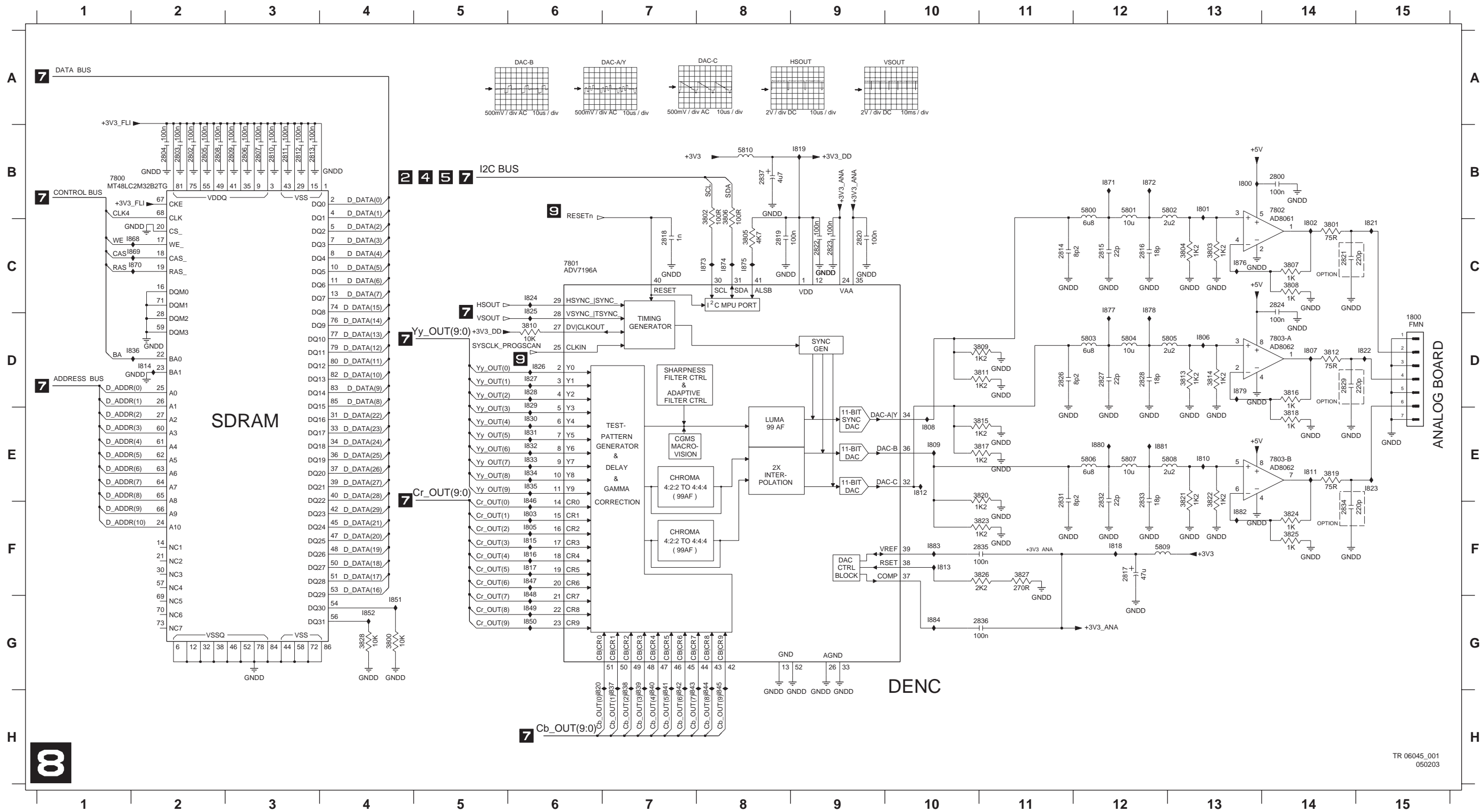


- 2700 B9
- 2701 B8
- 2702 B9
- 2703 B9
- 2704 B8
- 2705 B8
- 2706 B8
- 2707 G3
- 2708 B8
- 2709 B8
- 2710 B8
- 2711 B8
- 2712 B8
- 2713 B8
- 2714 F13
- 2715 B6
- 2716 B7
- 2717 B8
- 2718 B7
- 2719 B8
- 2720 B11
- 2721 E2
- 2722 D3
- 2723 B3
- 2724 B2
- 2725 B2
- 2726 B3
- 2727 B8
- 3700 G11
- 3701-A F11
- 3701-B F11
- 3701-C F11
- 3701-D F11
- 3702-A G11
- 3702-B F11
- 3702-C F11
- 3702-D F11
- 3703-A F6
- 3703-B F6
- 3703-C F6
- 3703-D F6
- 3704-A F6
- 3704-B F6
- 3704-C F6
- 3704-D F6
- 3705 F11
- 3706 G11
- 3707 H11
- 3708 H11
- 3709-A E6
- 3709-B E6
- 3709-C E6
- 3709-D E6
- 3710-A G6
- 3710-B F6
- 3710-C E6
- 3710-D E6
- 3711-A G6
- 3711-B G6
- 3711-C G6
- 3711-D G6
- 3712 F3
- 3713-A G6
- 3713-B G6
- 3713-C G6
- 3713-D G6
- 3714 G11
- 3715-A H7
- 3715-B H7
- 3715-C H7
- 3715-D H7
- 3716-A H8
- 3716-B H8
- 3716-C H7
- 3716-D H7
- 3717-A H8
- 3717-B H8
- 3717-C H8
- 3717-D H8
- 3718-A H8
- 3718-B H8
- 3718-C H8
- 3718-D H8
- 3719-A H8
- 3719-B H8
- 3719-C H8
- 3719-D H8
- 3720 F6
- 4700 A1
- 4701 B1
- 4702 E2
- 5700 B11
- 5701 A3
- 5702 B6
- 7700 B7
- 7701-A E1
- 7701-B C1
- 7702-A E3
- 7702-D C3
- 7703 A2
- 7700 B10
- 7701 E3
- 7702 E2
- 7703 E11
- 7704 B9
- 7705 B9
- 7706 B9
- 7707 F11
- 7708 E11
- 7709 A2
- 7710 B6
- 7711 A4
- 7712 A3
- 7713 G10
- 7714 F4
- 7715 F3
- 7716 G11
- 7717 F11
- 7718 F11
- 7719 F11
- 7720 F11
- 7721 F11
- 7722 F11
- 7723 F11
- 7724 F11
- 7725 F11
- 7726 F11
- 7727 F11
- 7728 C6
- 7729 D6
- 7730 D6
- 7731 D6
- 7732 D6
- 7733 D6
- 7734 D6
- 7735 D6

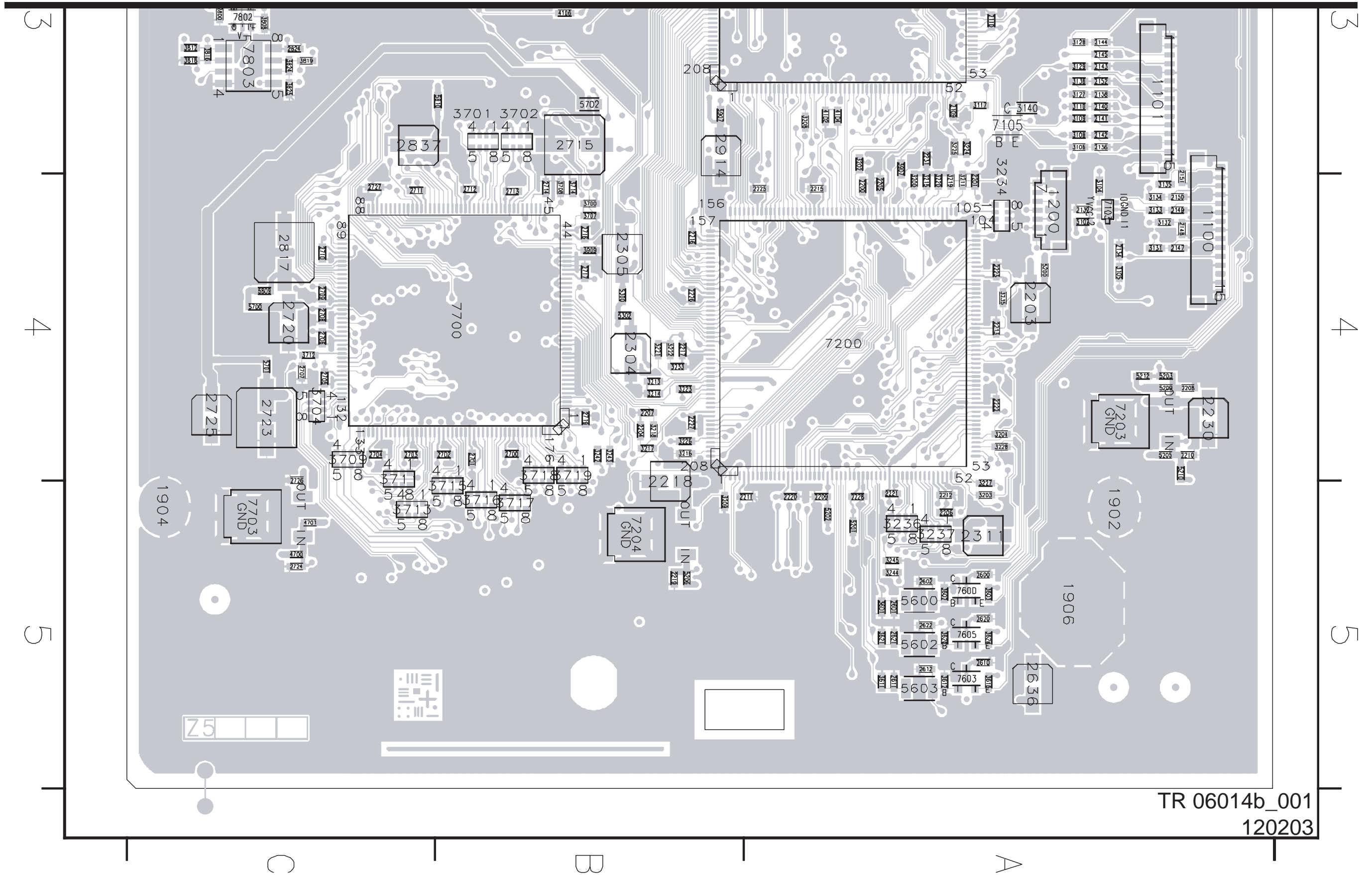
TR 06044_001
050203

Digital Board 1.5: Progressive Scan

1800 D15	2806 B3	2812 B3	2818 C7	2824 C14	2832 E12	3800 G4	3806 B8	3812 D14	3818 E14	3824 F14	5801 B12	5807 E12	7802 B14	I803 F6	I810 E13	I816 F6	I822 D15	I828 D6	I834 E6	I840 G7	I846 E6	I852 G4	I873 C8	I879 D13
2800 B14	2807 B3	2813 B3	2819 C8	2826 D11	2833 E12	3801 C14	3807 C14	3813 D13	3819 E14	3825 F14	5802 B13	5808 E13	7803-A D14	I805 F6	I811 E14	I817 F6	I823 E15	I829 D6	I835 E6	I841 G7	I847 F6	I853 G4	I874 C8	I880 E12
2802 B2	2808 B2	2814 C11	2820 C9	2827 D12	2834 F14	3802 B8	3808 C14	3814 D13	3820 E11	3826 F11	5803 D12	5809 F12	7803-B E14	I806 D13	I812 E10	I818 F12	I824 C6	I830 E6	I836 D2	I842 G7	I848 F6	I854 G4	I875 C8	I881 E12
2803 B2	2809 B3	2815 C12	2821 C14	2828 D12	2835 F11	3803 C13	3809 D11	3815 E11	3821 E13	3827 F11	5804 D12	5810 B8	I800 B13	I807 D14	I813 F10	I819 B9	I825 C6	I831 E6	I837 G7	I843 G7	I849 G6	I855 G4	I876 C13	I882 F13
2804 B2	2810 B3	2816 C12	2822 C9	2829 D14	2836 G11	3804 C13	3810 D6	3816 D14	3822 E13	3828 G4	5805 D13	5811 B8	I801 B13	I808 E10	I814 D2	I820 G6	I826 D6	I832 E6	I838 G7	I844 G8	I850 G6	I856 G4	I877 B12	I883 F10
2805 B2	2811 B3	2817 F12	2823 C9	2831 E11	2837 B8	3805 C8	3811 D11	3817 E11	3823 F11	5800 B12	5806 E12	7801 C6	I802 C14	I809 E10	I815 F6	I821 C15	I827 D6	I833 E6	I839 G7	I845 G8	I851 G4	I857 B12	I878 C12	I884 G10

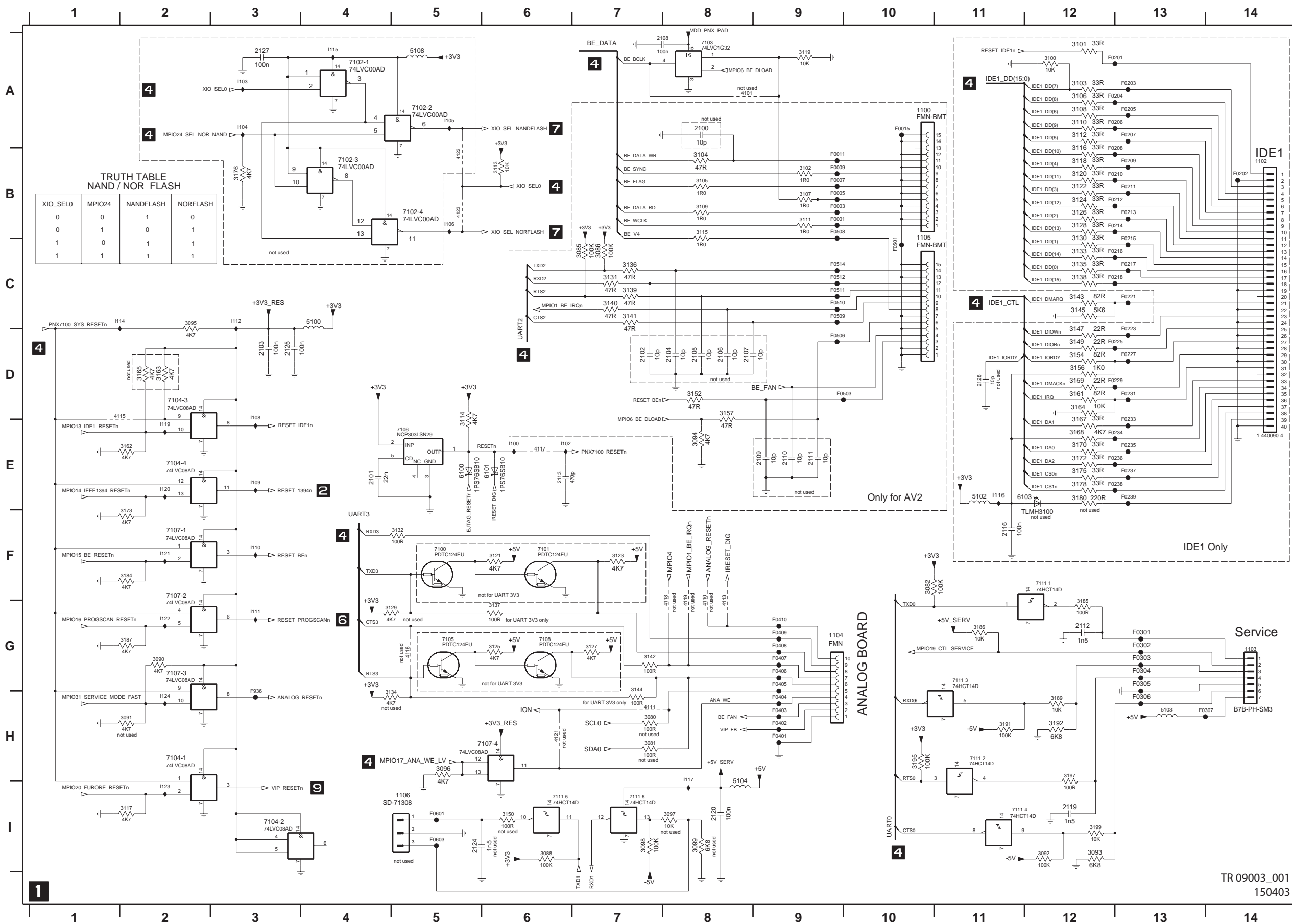


Layout Digital Board 1.5 (Part 2 Top View)



TR 06014b_001
120203

Digital Board Chrysalis 2.1: IDE, UARIS, RESET, BE



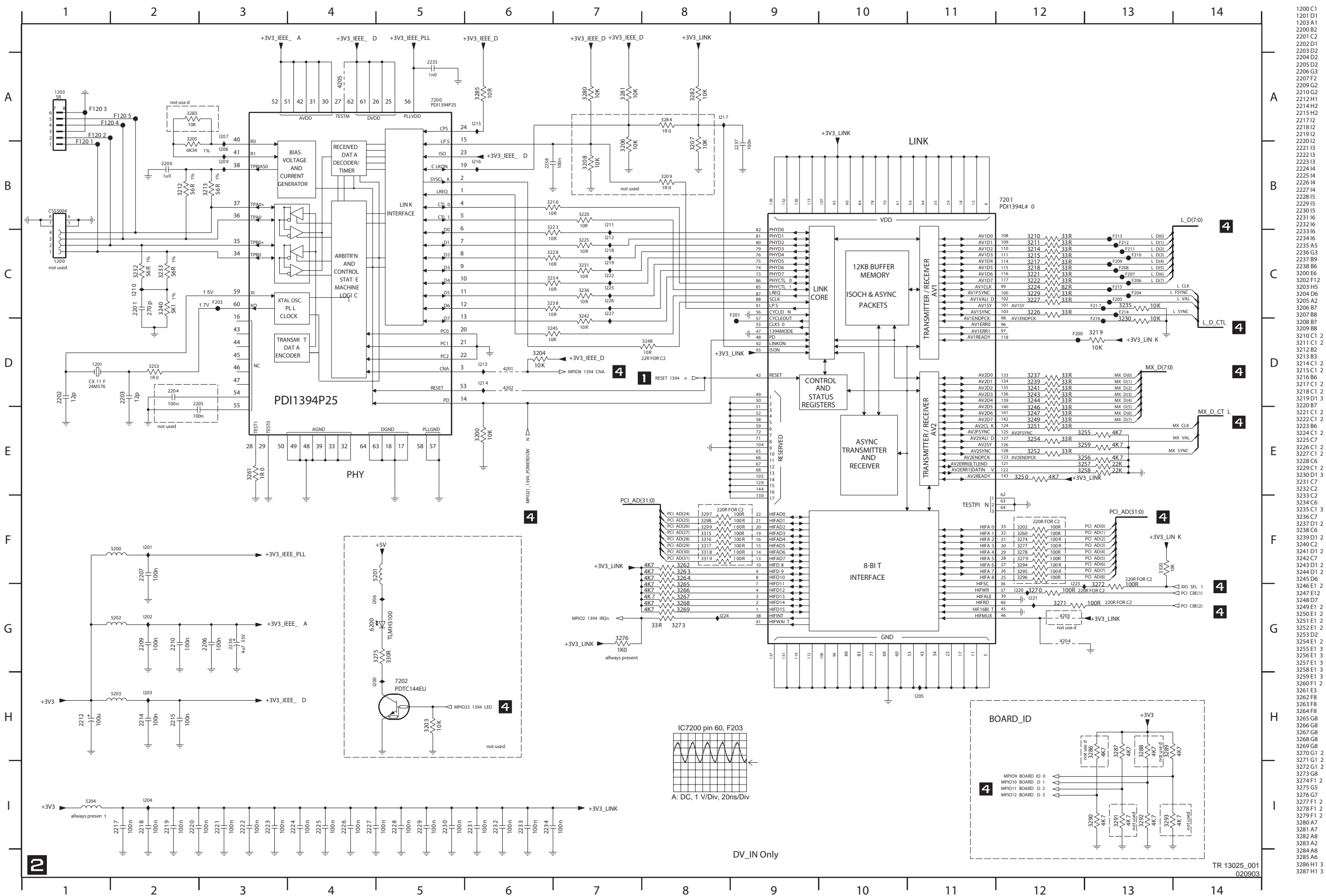
**TRUTH TABLE
NAND / NOR FLASH**

XIO_SEL0	MPIO24	NANDFLASH	NORFLASH
0	0	1	0
0	1	0	1
1	0	1	1
1	1	1	1

- 1100 A10
- 1102 B14
- 1103 G14
- 1104 G9
- 1105 C10
- 1106 I5
- 1106 I5
- 2100 A8
- 2101 E4
- 2102 D7
- 2103 D3
- 2104 D8
- 2105 D8
- 2106 D8
- 2107 D8
- 2108 A7
- 2109 E9
- 2110 E9
- 2111 E9
- 2112 G12
- 2113 E6
- 2119 I12
- 2120 I8
- 2121 D3
- 2122 D3
- 2128 D11
- 3080 H7
- 3081 H7
- 3082 F10
- 3085 C7
- 3086 C7
- 3088 I6
- 3090 G2
- 3091 H2
- 3092 I2
- 3093 I2
- 3094 E8
- 3095 C2
- 3095 H5
- 3097 B8
- 3098 I7
- 3099 I8
- 3100 A12
- 3101 A12
- 3102 B9
- 3103 A12
- 3104 B8
- 3105 B8
- 3106 A12
- 3107 B9
- 3108 A12
- 3109 B8
- 3110 A12
- 3111 B9
- 3112 A12
- 3113 B6
- 3114 D5
- 3115 B8
- 3116 B12
- 3117 I2
- 3118 B12
- 3119 A9
- 3120 B12
- 3121 F6
- 3122 D13
- 3123 F7
- 3124 B12
- 3125 G6
- 3126 B12
- 3127 G7
- 3128 B12
- 3129 G4
- 3130 C12
- 3131 C7
- 3132 F5
- 3133 C12
- 3134 H4
- 3135 C12
- 3136 C7
- 3137 G6
- 3138 C12
- 3139 C7
- 3140 C7
- 3141 C7
- 3142 G7
- 3143 C12
- 3144 G7
- 3145 C12
- 3147 D12
- 3149 D12
- 3150 H6
- 3152 D8
- 3154 D12
- 3156 D12
- 3157 D8
- 3159 D12
- 3161 D12
- 3162 E2
- 3163 D2
- 3164 D12
- 3165 D2
- 3167 E12
- 3168 E12
- 3170 E12
- 3172 E12
- 3173 F2
- 3175 E12
- 3176 B3
- 3178 B3
- 3180 E12
- 3184 F2
- 3185 G12
- 3186 G11
- 3187 G2
- 3189 H12
- 3191 H11
- 3192 H12
- 3195 H10
- 3197 H12
- 3199 H12
- 4101 A8
- 4110 F8
- 4111 H7
- 4113 F8
- 4115 D1
- 4116 G5
- 4117 E6
- 4118 F8
- 4119 F8
- 4121 H6
- 4122 B5
- 4123 B5
- 5100 C4
- 5102 E11
- 5103 H13
- 5104 I8
- 5108 A5
- 6100 E5
- 6101 E6
- 6106 E11
- 7100 F5
- 7101 F5
- 7102-1 A4
- 7102-2 A5
- 7111 E9
- 7102-3 B4
- 7104-1 H2
- 7104-13
- 7104-3 D2
- 7104-4 E2
- 7105 G3
- 7107-1 F2
- 7107-2 F2
- 7107-3 G2
- 7108 G6
- 7111-1 F12
- 7111-2 H11
- 7111-3 G11
- 7114 H11
- 7111-5 I6
- 7111-6 I7
- F0001 B9
- F0003 B9
- F0005 B9
- F0007 B9
- F0009 B9
- F0011 B9
- F0015 A10
- F0016 A12
- F0020 B14
- F0203 A13
- F0204 A13
- F0205 A13
- F0206 A13
- F0207 A13
- F0208 B13
- F0209 B13
- F0210 B13
- F0211 B13
- F0212 B13
- F0213 B13
- F0214 B13
- F0215 C13
- F0216 C13
- F0217 D13
- F0218 C13
- F0221 C13
- F0223 D13
- F0225 D13
- F0227 D13
- F0229 D13
- F0231 D13
- F0233 E13
- F0234 E13
- F0235 E13
- F0236 E13
- F0237 E13
- F0238 E13
- F0239 E13
- F0301 F13
- F0302 G13
- F0303 G13
- F0304 G13
- F0305 G13
- F0306 H13
- F0307 H14
- F0401 H9
- F0402 H9
- F0403 H9
- F0404 H9
- F0405 G9
- F0406 G9
- F0407 G9
- F0408 G9
- F0409 G9
- F0410 G9
- F0501 C10
- F0503 D10
- F0506 D9
- F0508 B9
- F0509 C9
- F0510 C9
- F0511 C9
- F0512 C9
- F0514 D12
- F0515 A4
- F0516 E11
- F0517 H8
- F0518 E2
- F0519 F2
- F0520 E2
- F0521 F2
- F0522 G2
- F0523 I2
- F0524 H2

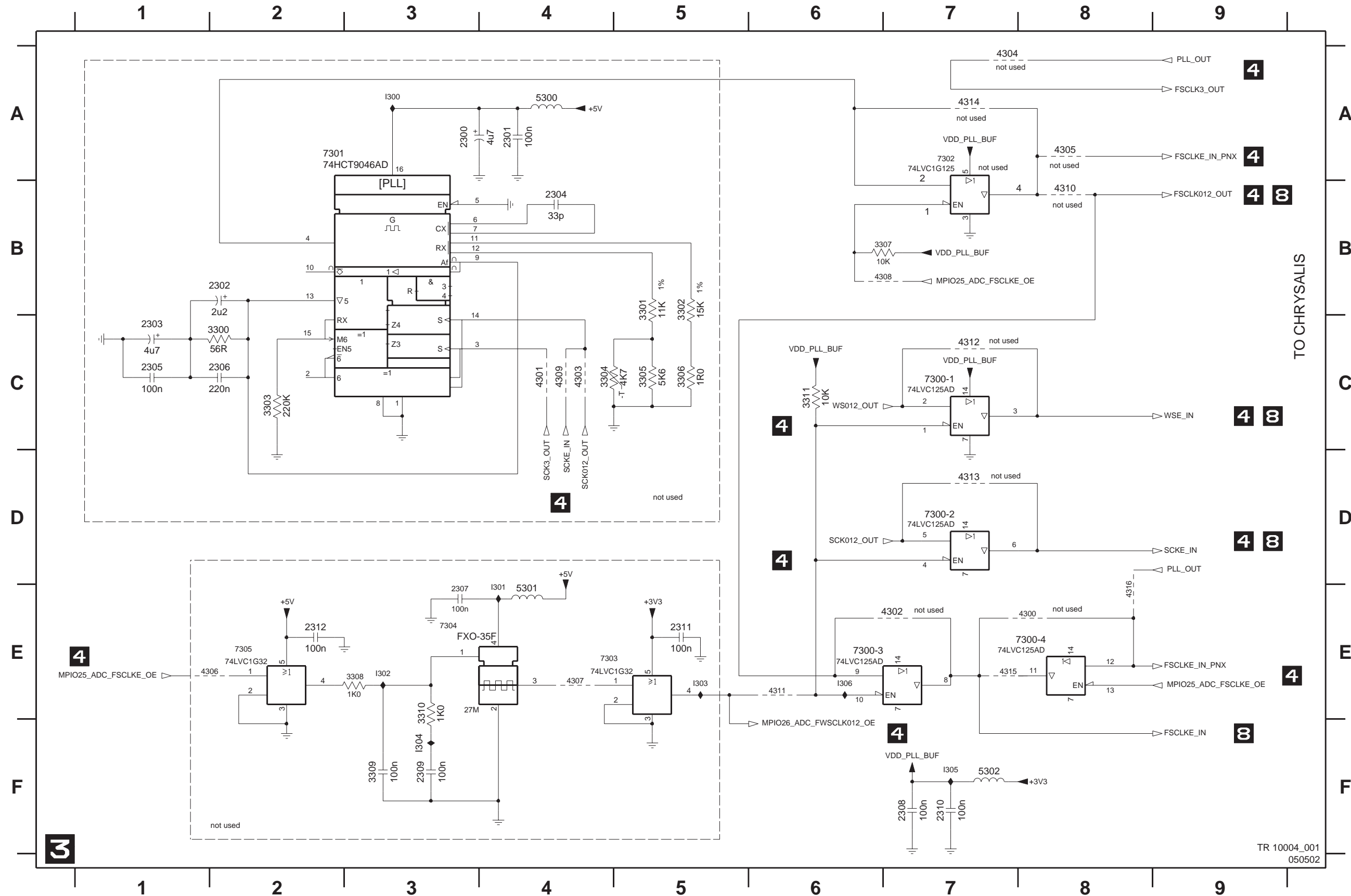
TR 09003_001
150403

Digital Board Chrysalis 2.1: 1394



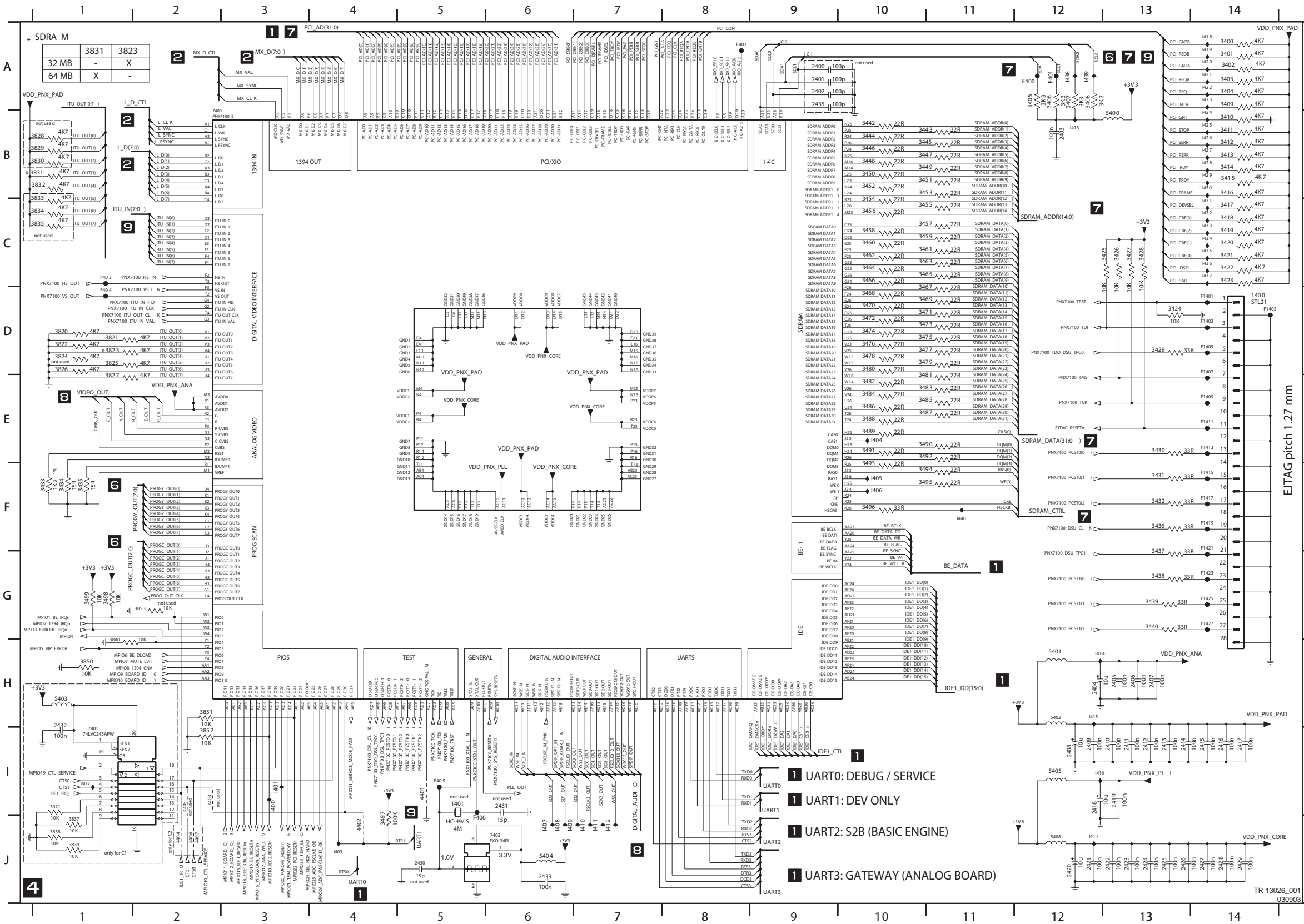
1200C1	3288H1 3
1201D1	3289H1 3
1203A1	3290I1 3
2200B2	3291I1 3
2201C2	3292I1 3
2202D1	3293I1 3
2203D2	3294F1 2
2204D2	3295F1 2
2205D2	3296F1 2
2206G3	3297F8
2207F2	3298F8
2209G2	3299F8
2210G2	3300F2
2211H1	3301F8
2212H2	3302F8
2213H2	3303F1 3
2214H2	3304F1 2
2215H2	3305F1 2
2217I2	3306F1 3
2218I2	3307F1 3
2219I2	4201D6
2220I2	4202D6
2221I3	4203G1 2
2222I3	4204G1 2
2223I3	4205A4
2224I4	5200F1 3
2225I4	5201F5
2226I4	5202G2
2227I4	5203H2
2228I5	5204I1
2229I5	6200G4
2230I5	7200A5
2231I6	7201B1 2
2232I6	7202H5
2233I6	7203H5
2234I6	F1201B1
2235A5	F1202A1
2236G3	F1203A1
2237B9	F1204A2
2238B6	F200D1 2
3200E6	F201C9
3202F12	F203C3
3203H5	F204C1 3
3204D6	F204D6
3205A2	F206C1 3
3206B7	F207C1 3
3207B8	F208C1 3
3208B7	F209C1 3
3209B8	F210C1 3
3210C1 2	F211C1 3
3211C1 2	F212C1 3
3212B2	F213C1 3
3213B3	F214C1 3
3214C1 2	F215C1 3
3215C1 2	F216D1 3
3216B6	F217C1 3
3217C1 2	I200H4
3218C1 2	I201F2
3219D1 3	I202G2
3220B7	I203H2
3221C1 2	I204I2
3222C1 2	I205H11
3223B6	I206G4
3224C1 2	I207A3
3225C7	I208B3
3226C1 2	I209B3
3227C1 2	I210C2
3228C6	I211B7
3229C1 2	I212C7
3230D1 3	I213D6
3231C7	I214D6
3232C2	I215A6
3233C2	I216B6
3234C6	I217A8
3235C1 3	I218C7
3236C7	I219C7
3237D1 2	I220G1 2
3238C6	I221G1 2
3239D1 2	I222C7
3240C2	I223G1 2
3241D1 2	I224G8
3242C7	I225C7
3243D1 2	I226C7
3244D1 2	I227C7
3245D6	
3246E1 2	
3247I2	
3248D7	
3249E1 2	
3250E1 2	
3251E1 2	
3252E1 2	
3253D2	
3254E1 2	
3255E1 3	
3256E1 3	
3257E1 3	
3258E1 3	
3259E1 3	
3260F1 2	
3261E3	
3262F8	
3263F8	
3264F8	
3265G8	
3266G8	
3267G8	
3268G8	
3269G8	
3270G1 2	
3271G1 2	
3272G1 2	
3273G8	
3274F1 2	
3275G5	
3276G7	
3277F1 2	
3278F1 2	
3279F1 2	
3280A7	
3281A7	
3282A8	
3283A2	
3284A8	
3285A6	
3286H1 3	
3287H1 3	

Digital Board Chrysalis 2.1: Audio PLL



- 2300 A3
- 2301 A4
- 2302 B2
- 2303 C1
- 2304 B4
- 2305 C1
- 2306 C2
- 2307 E3
- 2308 F7
- 2309 F3
- 2310 F7
- 2311 E5
- 2312 E2
- 3300 C2
- 3301 B5
- 3302 B5
- 3303 C2
- 3304 C4
- 3305 C5
- 3306 C5
- 3307 B6
- 3308 E3
- 3309 F3
- 3310 E3
- 3311 C6
- 4300 E8
- 4301 C4
- 4302 E7
- 4303 C4
- 4304 A7
- 4305 A8
- 4306 E1
- 4307 E4
- 4308 B6
- 4309 C4
- 4310 B8
- 4311 E6
- 4312 C7
- 4313 D7
- 4314 A7
- 4315 E7
- 4316 E8
- 5300 A4
- 5301 E4
- 5302 F7
- 7300-1 C7
- 7300-2 D7
- 7300-3 E6
- 7300-4 E8
- 7301 A2
- 7302 A7
- 7303 E5
- 7304 E3
- 7305 E2
- I300 A3
- I301 E4
- I302 E3
- I303 E5
- I304 F3
- I305 F7
- I306 E6

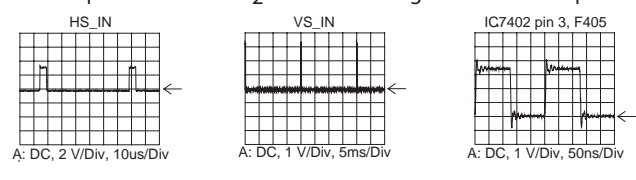
Digital Board Chrysalis 2.1: Chrysalis



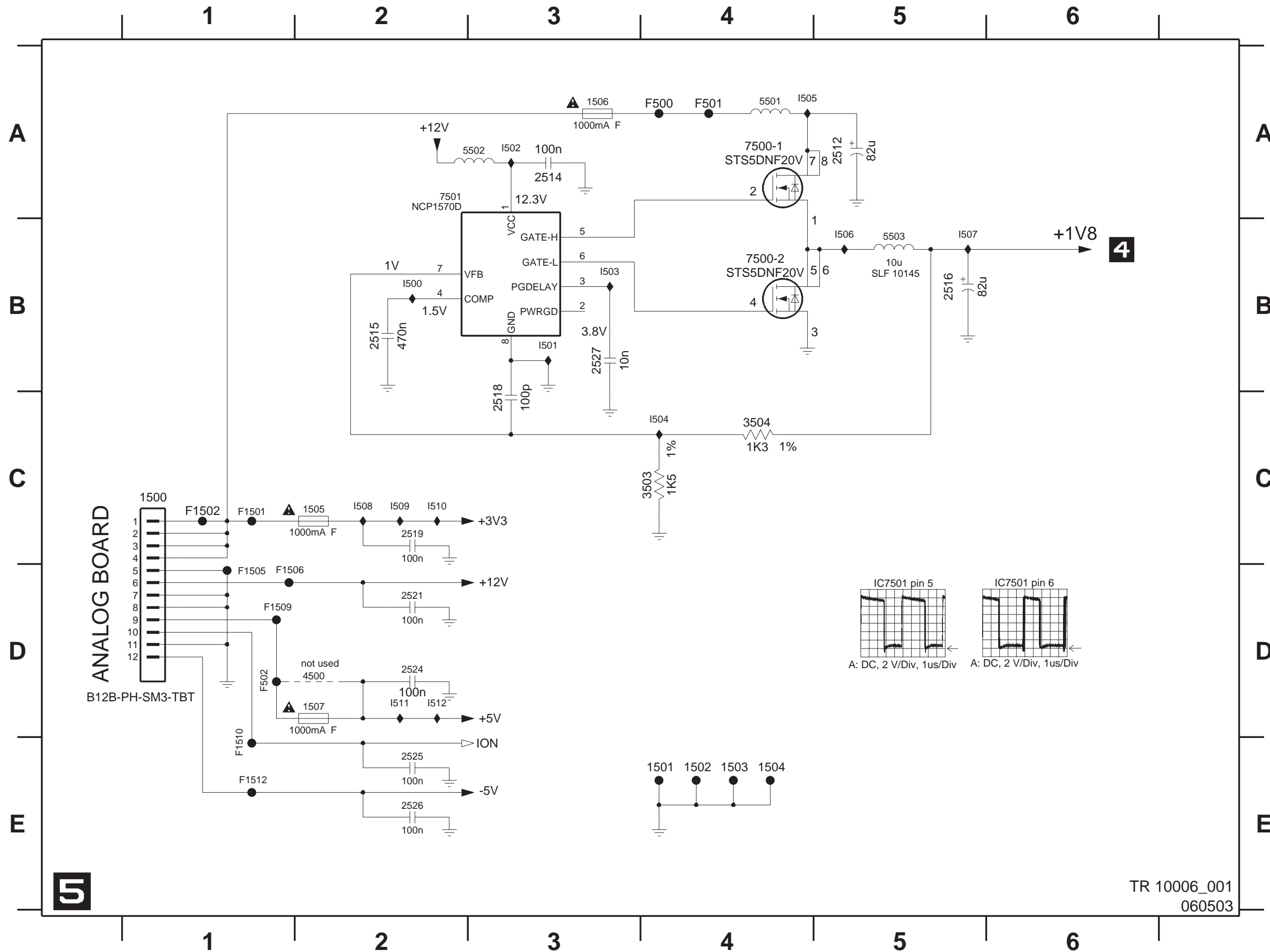
1400 D14	3447 B11	5400 B13
1401 I5	3448 B10	5401 H12
2400 A9	3449 B11	5402 H12
2401 A9	3450 B10	5403 H1
2402 A9	3451 B11	5404 J6
2403 B12	3452 B10	5405 I2
2404 H12	3453 B11	5406 J12
2405 H13	3454 C10	7400 B2
2406 H13	3455 C11	7401 I1
2407 H13	3456 C10	7402 J6
2408 I12	3457 C11	F1401 D14
2409 I12	3458 C10	F1402 D14
2410 I13	3459 C11	F1403 D14
2411 I13	3460 C10	F1405 D14
2412 I13	3461 C11	F1407 D14
2413 I13	3462 C10	F1409 E14
2414 I13	3463 C11	F1411 E14
2415 I14	3464 C10	F1413 E14
2416 I14	3465 C11	F1415 F14
2417 I14	3466 C10	F1427 G14
2418 I12	3467 D11	F1419 F14
2419 I13	3468 D10	F1421 F14
2420 J12	3469 D11	F1423 G14
2421 J12	3470 D10	F1425 G14
2422 J13	3471 D11	F1427 G14
2423 J13	3472 D10	F400 A12
2424 J13	3473 D11	F401 A12
2425 J13	3474 D10	F402 A8
2426 J13	3475 D11	F403 C1
2427 J14	3476 D10	F404 D1
2428 J14	3477 D11	F405 I5
2429 J14	3478 D10	F406 I5
2430 J5	3479 D11	I400 I3
2431 I6	3480 D10	I401 I3
2432 I1	3481 E11	I402 I1
2433 J6	3482 E10	I403 J4
2435 A9	3483 E11	I404 E10
3021 I1	3484 E10	I405 F10
3400 A14	3485 E11	I406 F10
3401 A14	3486 E10	I407 J6
3402 A14	3487 E11	I408 J6
3403 A14	3488 E10	I409 J6
3404 A14	3489 E10	I410 J7
3405 A12	3490 E11	I411 J7
3406 A12	3491 E10	I412 J7
3407 A12	3492 E11	I413 B12
3408 A12	3493 F10	I414 H12
3409 A14	3494 F11	I415 H12
3410 B14	3495 F11	I416 I12
3411 B14	3496 F10	I417 J12
3412 B14	3497 J4	I418 A14
3413 B14	3498 G1	I419 A14
3414 B14	3499 G1	I420 A14
3415 B14	3820 D1	I421 A14
3416 B14	3821 D1	I422 A14
3417 C14	3822 D1	I423 A14
3418 C14	3823 D1	I424 B14
3419 C14	3824 D1	I425 B14
3420 C14	3825 D1	I426 B14
3421 C14	3826 D1	I427 B14
3422 C14	3827 E1	I428 B14
3423 C14	3828 B1	I429 B14
3424 D13	3829 B1	I430 B14
3425 C13	3830 B1	I431 C14
3426 C13	3831 B1	I432 C14
3427 C13	3832 B1	I433 C14
3428 C13	3833 C1	I434 C14
3429 D13	3834 C1	I435 C14
3430 E13	3835 C1	I436 C14
3431 F13	3837 J1	I437 C14
3432 F13	3838 J1	I438 A12
3433 F1	3839 J1	I439 A12
3434 F1	3840 H1	I440 F11
3435 F1	3850 H1	
3436 F13	3851 H2	
3437 G13	3852 I2	
3438 G13	3853 G2	
3439 G13	4401 I5	
3440 G13	4402 J4	
3442 B10	4403 I2	
3443 B11	4404 J2	
3444 B10	4405 J2	
3445 B11	4406 J2	
3446 B10	4407 J2	

EJTAG pitch 1.27 mm

- 1 UART0: DEBUG / SERVICE
- 1 UART1: DEV ONLY
- 1 UART2: S2B (BASIC ENGINE)
- 1 UART3: GATEWAY (ANALOG BOARD)

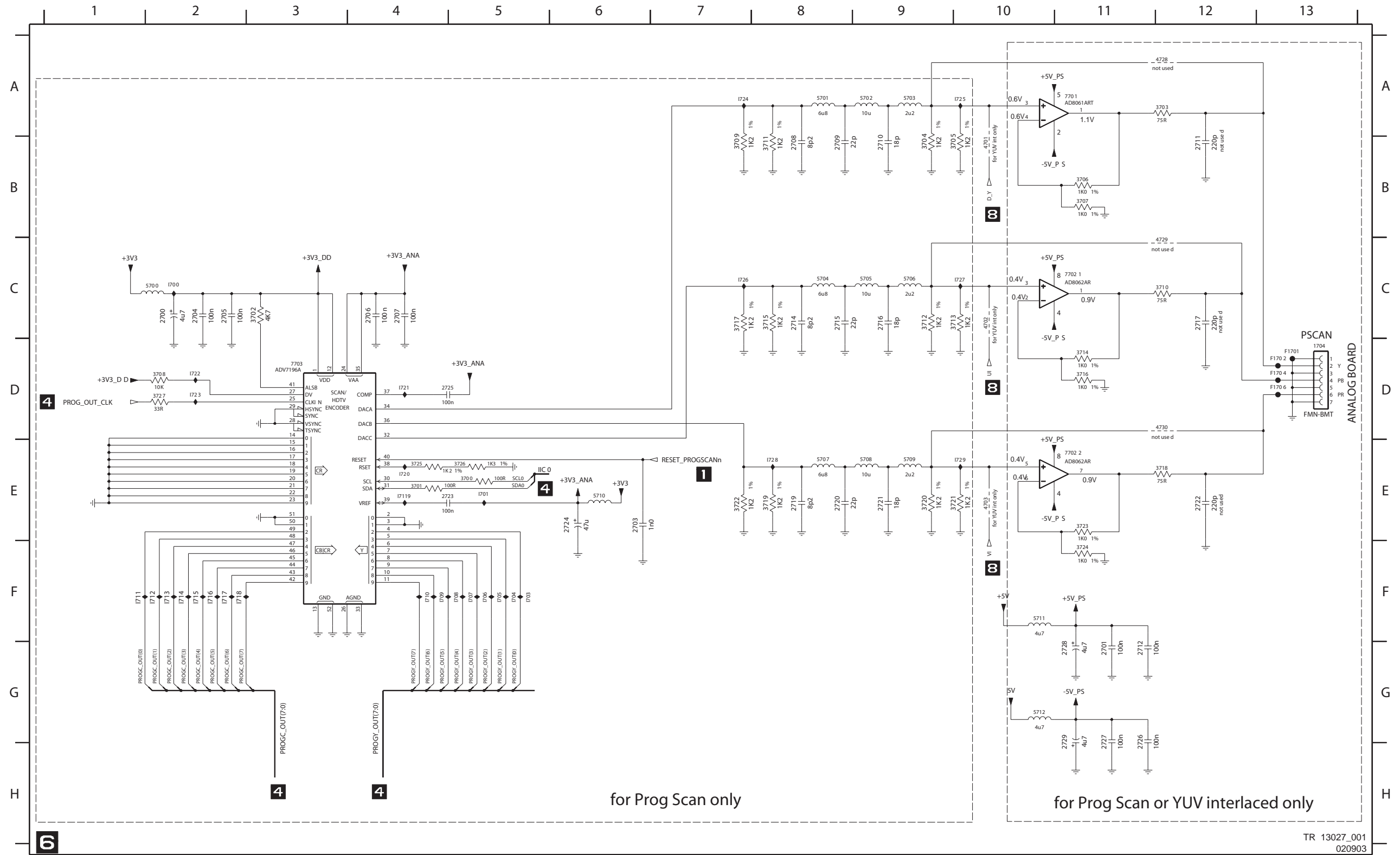


Digital Board Chrysalis 2.1: 1.8V Power

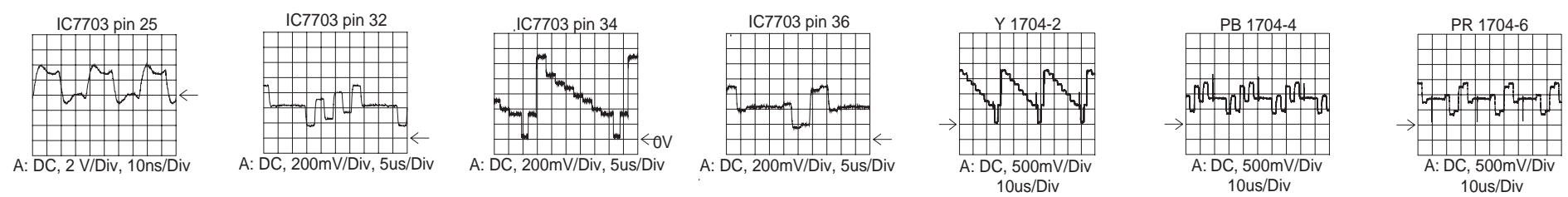


- 1500 C1
- 1501 E4
- 1502 E4
- 1503 E4
- 1504 E4
- 1505 C2
- 1506 A3
- 1507 D2
- 2512 A5
- 2514 A3
- 2515 B2
- 2516 B5
- 2518 C3
- 2519 C2
- 2521 D2
- 2524 D2
- 2525 E2
- 2526 E2
- 2527 B3
- 3503 C4
- 3504 C4
- 4500 D2
- 5501 A4
- 5502 A3
- 5503 B5
- 7500-1 A4
- 7500-2 B4
- 7501 A2
- F1501 C1
- F1502 C1
- F1505 D1
- F1506 D1
- F1509 D1
- F1510 E1
- F1512 E1
- F500 A4
- F501 A4
- F502 D1
- I500 B2
- I501 B3
- I502 A3
- I503 B3
- I504 C4
- I505 A4
- I506 B5
- I507 B5
- I508 C2
- I509 C2
- I510 C2
- I511 D2
- I512 D2

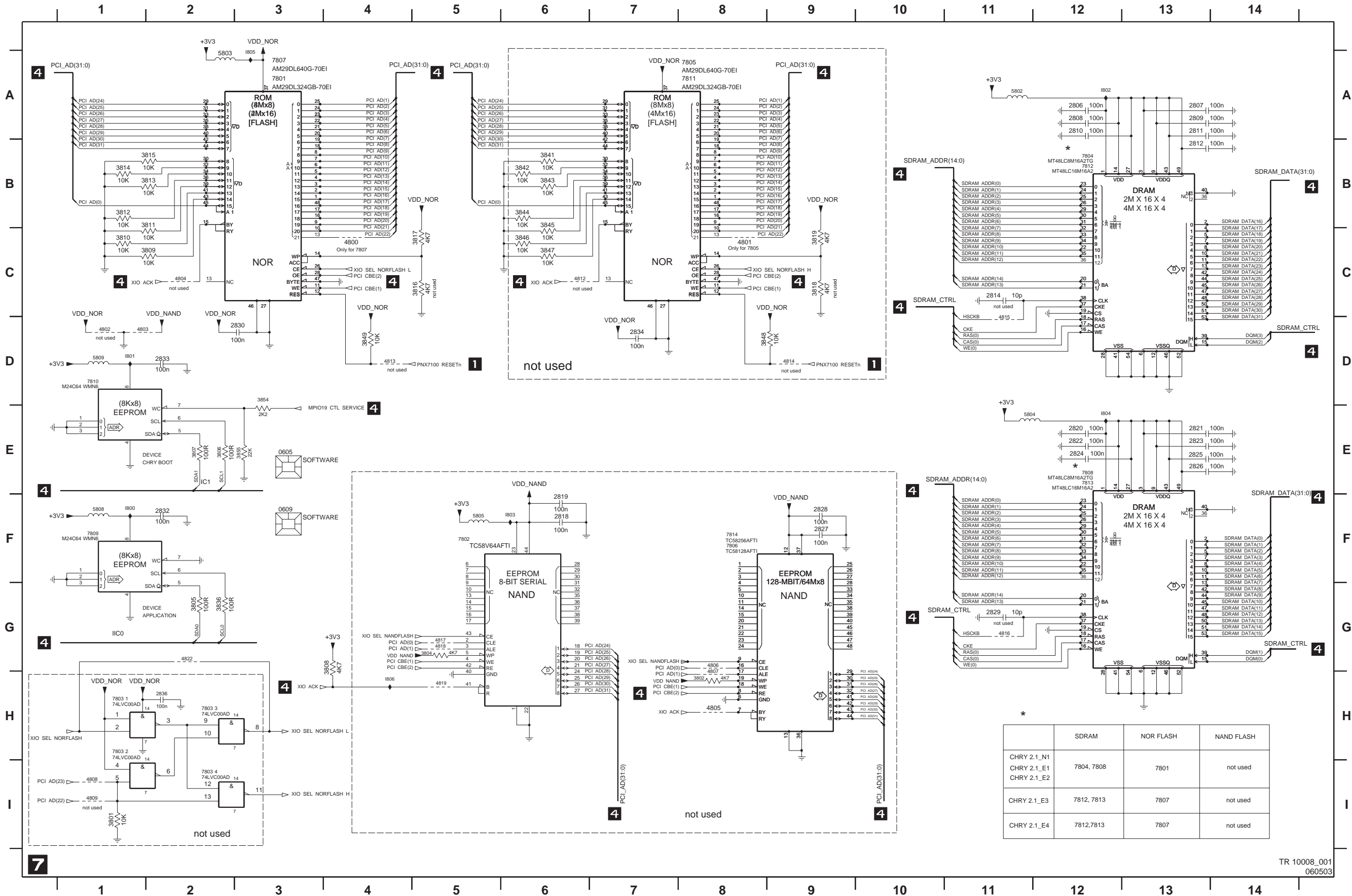
Digital Board Chrysalis 2.1: Prog. scan DAC



- 1704 D1 3
- 1715 F2
- 2700 C2
- 1716 F2
- 2701 G1 1
- 1717 F2
- 2703 E6
- 1718 F2
- 2704 C2
- 1720 E4
- 2705 C2
- 1721 D4
- 2706 C4
- 1722 D2
- 2707 C4
- 1723 D2
- 2708 B8
- 1724 A7
- 2709 B8
- 1725 A10
- 2710 B9
- 1726 C7
- 2711 B12
- 1727 C10
- 2712 G11
- 1728 E8
- 2714 C8
- 1729 E10
- 2715 C8
- 2716 C9
- 2717 C12
- 2719 E8
- 2720 E8
- 2721 E9
- 2722 E1 2
- 2723 E4
- 2724 E6
- 2725 D4
- 2726 G11
- 2727 G11
- 2728 G11
- 2729 G11
- 3700 E5
- 3701 E4
- 3702 C3
- 3703 A12
- 3704 B9
- 3705 B10
- 3706 B11
- 3707 B11
- 3708 D2
- 3709 B7
- 3710 C12
- 3711 B8
- 3712 C9
- 3713 C10
- 3714 D11
- 3715 C8
- 3716 D1 1
- 3717 C7
- 3718 E12
- 3719 E8
- 3720 E9
- 3721 E10
- 3722 E7
- 3723 E1 1
- 3725 E4
- 3726 E5
- 3727 D2
- 4701 B10
- 4702 C10
- 4703 E10
- 4704 C10
- 4705 C12
- 4706 D12
- 5700 C2
- 5701 A8
- 5702 A9
- 5703 A9
- 5704 C8
- 5705 C9
- 5706 C9
- 5707 E8
- 5708 E9
- 5709 E9
- 5710 E6
- 5711 F10
- 5712 G10
- 7701 A11
- 7702-1 C11
- 7702-2 E11
- 7703 D3
- F1701 D13
- F1702 D13
- F1704 D13
- F1706 D13
- I700 C2
- I701 E5
- I703 F5
- I704 F5
- I705 F5
- I706 F5
- I707 F5
- I708 F5
- I709 F4
- I710 F4
- I711 F1
- I7119 E4
- I712 F2
- I713 F2
- I714 F2



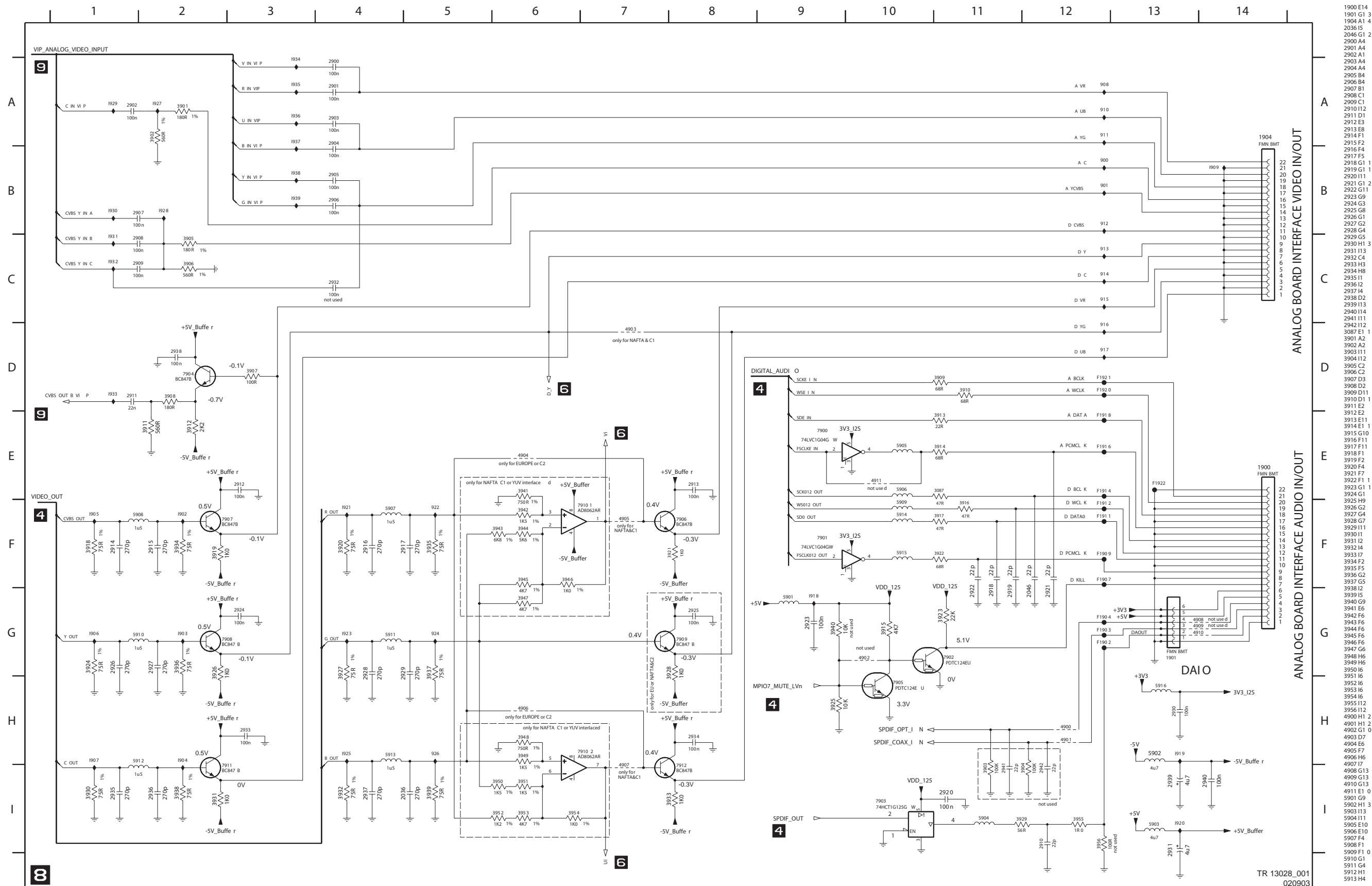
Digital Board Chrysalis 2.1: Flash SDRAM EEPROM



- 0605 E3
- 0609 F3
- 2806 A12
- 2807 A13
- 2808 A12
- 2809 A13
- 2810 A12
- 2811 A13
- 2812 B13
- 2814 C11
- 2818 F6
- 2819 F6
- 2820 E12
- 2821 E13
- 2822 E12
- 2823 E13
- 2824 E12
- 2825 E13
- 2826 E13
- 2827 F9
- 2828 F9
- 2829 G11
- 2830 D3
- 2832 F2
- 2833 D2
- 2834 D7
- 2836 H2
- 3801 I1
- 3802 H8
- 3804 G5
- 3805 G2
- 3806 E2
- 3807 E2
- 3808 G4
- 3809 C2
- 3810 C1
- 3811 B2
- 3812 B1
- 3813 B2
- 3814 B1
- 3815 B2
- 3816 C5
- 3817 C5
- 3818 C9
- 3819 C9
- 3836 G2
- 3841 B6
- 3842 B6
- 3843 B6
- 3844 B6
- 3845 B6
- 3846 C6
- 3847 C6
- 3848 D8
- 3849 D4
- 3854 D3
- 3855 E3
- 4800 C4
- 4801 C8
- 4802 D1
- 4803 D1
- 4804 C2
- 4805 H8
- 4806 G8
- 4807 H8
- 4808 I1
- 4809 I1
- 4812 C6
- 4813 D4
- 4814 D9
- 4815 D11
- 4816 G11
- 4817 G5
- 4818 G5
- 4819 H5
- 4822 G2
- 5802 A11
- 5803 A2
- 5804 E11
- 5805 F5
- 5808 F1
- 5809 D1
- 7801 A3
- 7802 F5
- 7803-1 H1
- 7803-2 H1
- 7803-3 H2
- 7803-4 I2
- 7804 B12
- 7805 A8
- 7806 F8
- 7807 A3
- 7808 E12
- 7809 F1
- 7810 D1
- 7811 A8
- 7812 B12
- 7813 E12
- 7814 F9
- 8000 F1
- 8001 D1
- 8002 A12
- 8003 F6
- 8004 E12
- 8005 A3
- 8006 H4

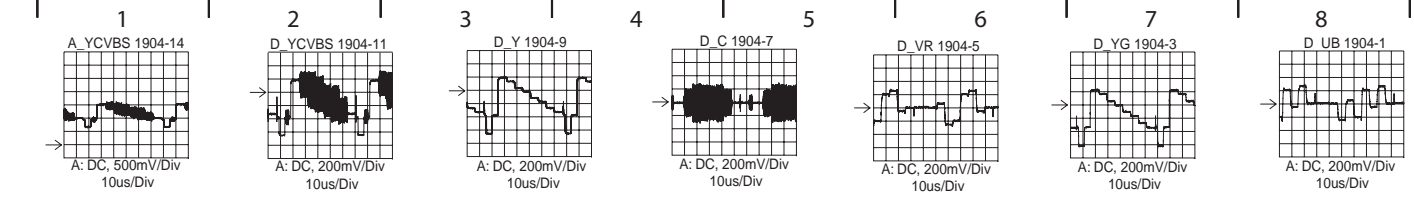
	SDRAM	NOR FLASH	NAND FLASH
CHRY 2.1_N1	7804, 7808	7801	not used
CHRY 2.1_E1			
CHRY 2.1_E2			
CHRY 2.1_E3	7812, 7813	7807	not used
CHRY 2.1_E4	7812, 7813	7807	not used

Digital Board Chrysalis 2.1: Video IO

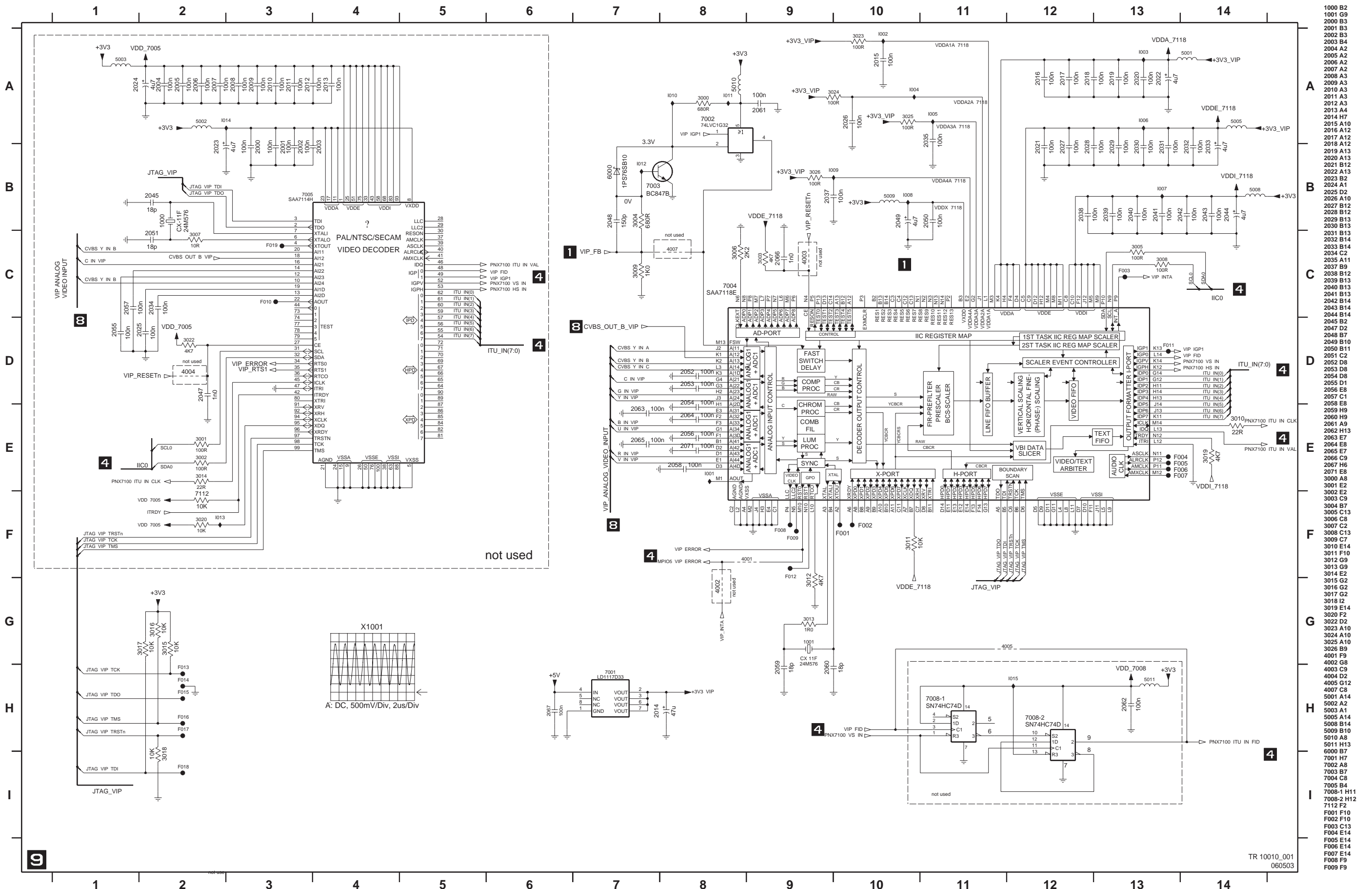


1900 E14	5914 F1 0
1901 G1 3	5915 F1 0
1904 A1 4	5916 H1 3
2036 I5	7900 E9
2046 G1 2	7901 F9
2900 A4	7902 G11
2901 A4	7903 I10
2902 A1	7904 D2
2903 A4	7905 H1 0
2904 A4	7906 F8
2905 B4	7907 F2
2906 B4	7908 G2
2907 B1	7909 G8
2908 C1	7910-1 F6
2909 C1	7910-2 H6
2910 I12	7911 I2
2911 D1	7912 I8
2912 E3	F1902 G1 2
2913 E8	F1903 G1 2
2914 F1	F1904 G1 2
2915 F2	F1907 F1 2
2916 F4	F1909 F1 2
2917 F5	F1911 F1 2
2918 G1 1	F1912 F1 2
2919 G1 1	F1914 E1 2
2920 I11	F1916 E1 2
2921 G1 2	F1918 E1 2
2922 G11	F1920 D1 2
2923 G9	F1921 D1 2
2924 G3	F1922 E13
2925 G8	1900 B12
2926 G1	1901 B12
2927 G2	1902 F2
2928 G4	1903 G2
2929 G2	1904 H2
2930 H1 3	1905 F1
2931 I13	1906 G1
2932 C4	1907 H1
2933 H3	1908 A12
2934 H8	1909 B14
2935 I1	1910 A12
2936 I2	1911 A12
2937 I4	1912 B12
2938 D2	1913 C12
2939 I13	1914 C12
2940 I14	1915 C12
2941 I11	1916 D12
2942 I12	1917 D12
3087 E1 1	1918 G9
3901 A2	1919 H13
3902 A2	1920 I1 3
3903 I11	1921 F4
3904 I12	1922 F5
3905 C2	1923 G4
3906 C2	1924 G5
3907 D3	1925 H4
3908 D2	1926 H2
3909 D11	1927 A2
3910 D1 1	1928 B2
3911 E2	1929 A1
3912 E2	1930 B1
3913 E11	1931 C1
3914 E1 1	1932 C1
3915 G10	1933 D1
3916 F11	1934 A3
3917 F11	1935 A3
3918 F1	1936 A3
3919 F2	1937 A3
3920 F4	1938 B3
3921 F7	1939 B3
3922 F1 1	
3923 G1 1	
3924 G1	
3925 H9	
3926 G2	
3927 G4	
3928 G7	
3929 I11	
3930 I1	
3931 I2	
3932 I4	
3933 I7	
3934 F2	
3935 F5	
3936 G2	
3937 G5	
3938 I2	
3939 I5	
3940 G9	
3941 E6	
3942 F6	
3943 F6	
3944 F6	
3945 F6	
3946 F6	
3948 H6	
3949 H6	
3950 H6	
3951 H6	
3952 I6	
3953 I6	
3954 I6	
3955 I12	
3956 I12	
4900 H1 2	
4901 H1 2	
4902 G1 0	
4903 D7	
4904 E6	
4905 F7	
4906 H6	
4907 I7	
4908 G13	
4909 G13	
4910 G13	
4911 E1 0	
5901 G9	
5902 H1 3	
5903 I13	
5904 I11	
5905 E10	
5906 E10	
5907 F4	
5908 F1	
5909 F1 0	
5910 G1	
5911 G4	
5912 H1	
5913 H4	

TR 13028_001
020903

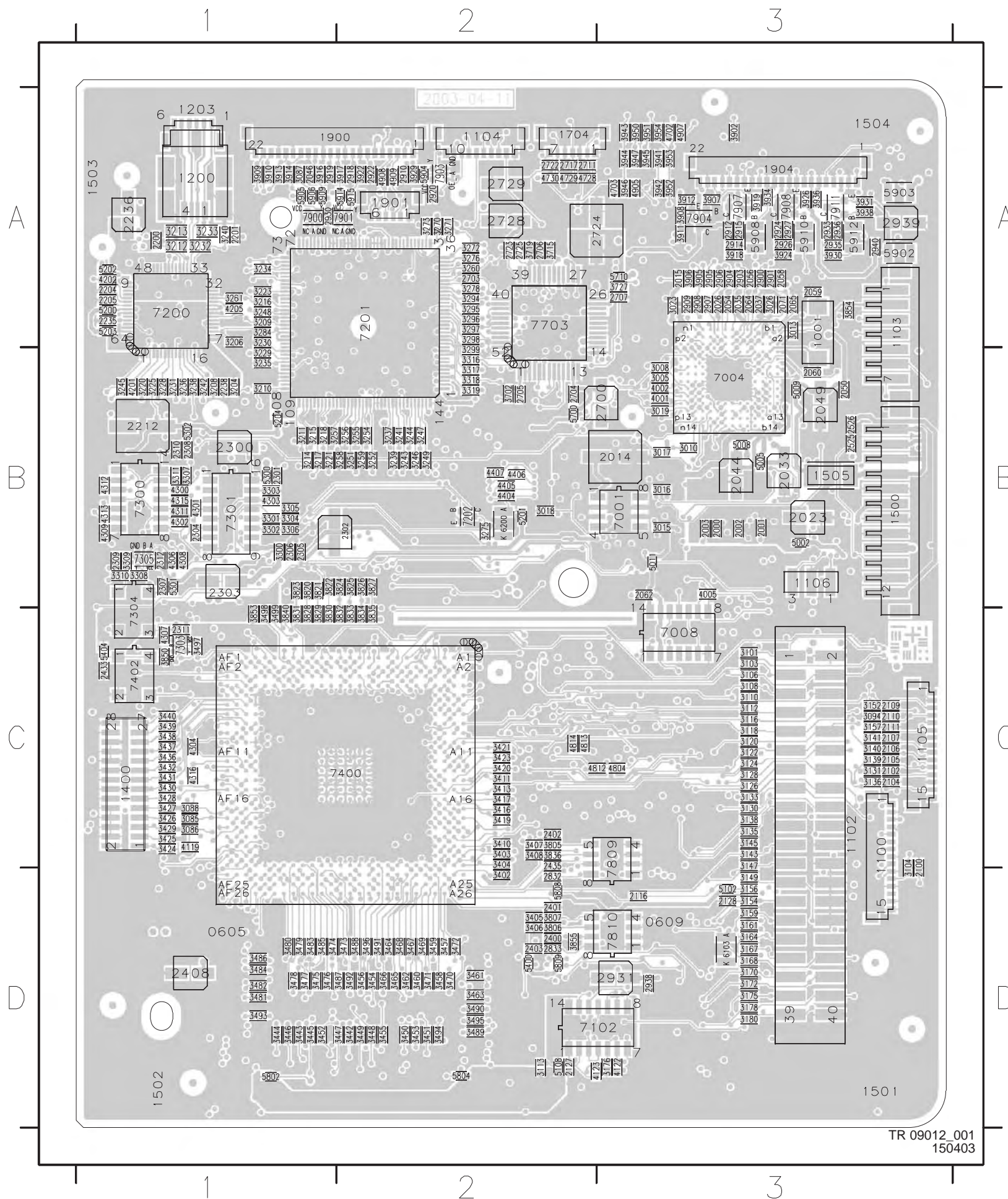


Digital Board Chrysalis 2.1: VIPs



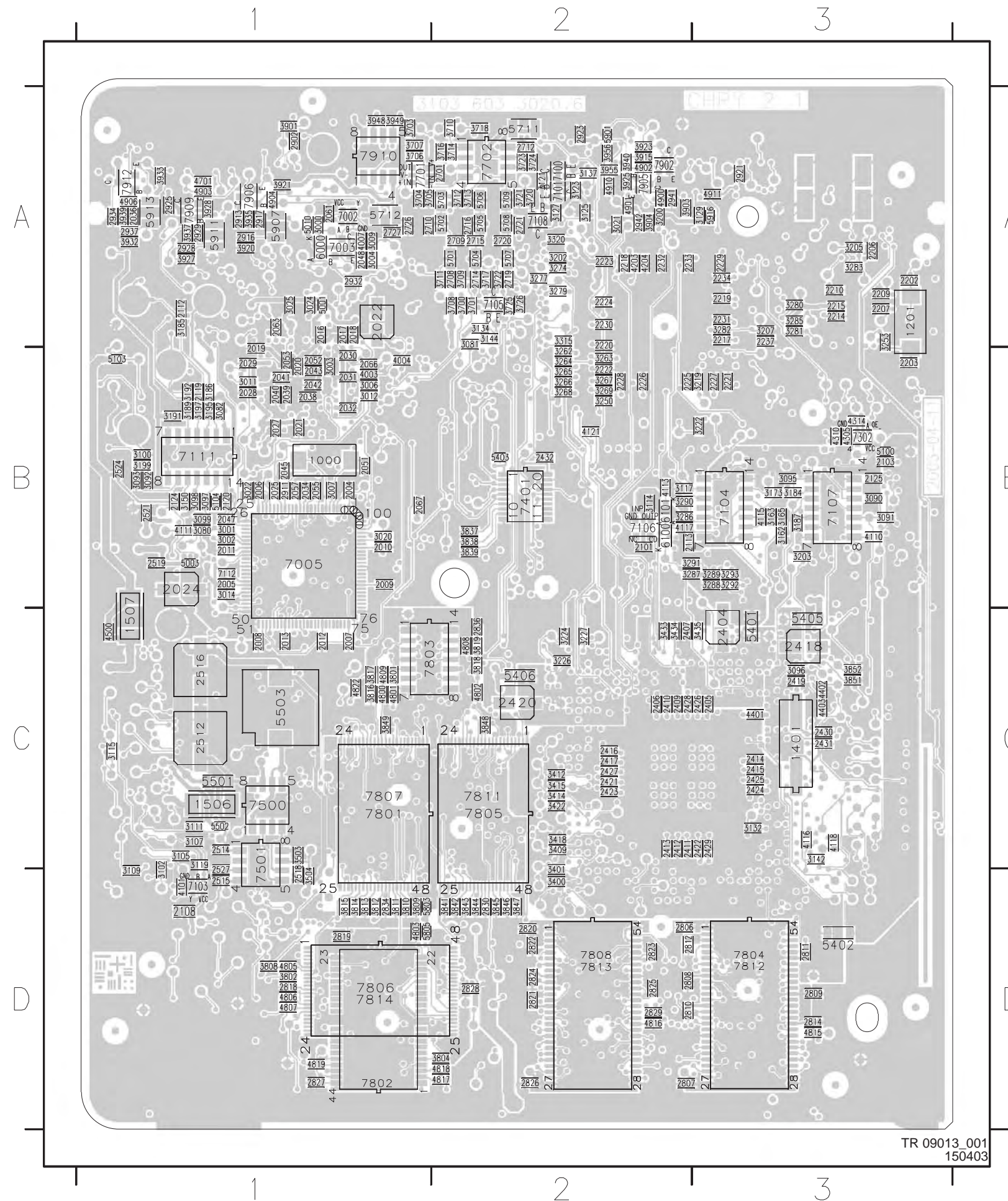
- 1000 B2
- 1001 G9
- 2000 B3
- 2001 B3
- 2002 B3
- 2003 B4
- 2004 A2
- 2005 A2
- 2006 A2
- 2007 A2
- 2008 A3
- 2009 A3
- 2010 A3
- 2011 A3
- 2012 A3
- 2013 A4
- 2014 H7
- 2015 A10
- 2016 A12
- 2017 A12
- 2018 A12
- 2019 A13
- 2020 A13
- 2021 B12
- 2022 A13
- 2023 B2
- 2024 A1
- 2025 D2
- 2026 A10
- 2027 B12
- 2028 B12
- 2029 B13
- 2030 B13
- 2031 B13
- 2032 B14
- 2033 B14
- 2034 C2
- 2035 A11
- 2037 B9
- 2038 B12
- 2039 B13
- 2040 B13
- 2041 B13
- 2042 B14
- 2043 B14
- 2044 B14
- 2045 B2
- 2047 D2
- 2048 B7
- 2049 B10
- 2050 B11
- 2051 C2
- 2052 D8
- 2053 D8
- 2054 D8
- 2055 D1
- 2056 E8
- 2057 C1
- 2058 E8
- 2059 H9
- 2060 H9
- 2061 A9
- 2062 H13
- 2063 E7
- 2064 E8
- 3001 E2
- 3002 E2
- 3003 C9
- 3004 B7
- 3005 C13
- 3006 C8
- 3007 C2
- 3008 C13
- 3009 C7
- 3010 E14
- 3011 F10
- 3012 G9
- 3013 G9
- 3014 E2
- 3015 G2
- 3016 G2
- 3017 G2
- 3018 I2
- 3019 E14
- 3020 F2
- 3022 D2
- 3023 A10
- 3024 A10
- 3025 A10
- 3026 B9
- 4001 F9
- 4002 B8
- 4003 C9
- 4004 D2
- 4005 G12
- 4007 C8
- 5001 A14
- 5002 A2
- 5003 A1
- 5005 A14
- 5008 B14
- 5009 B10
- 5010 A8
- 5011 H13
- 6000 B7
- 7001 H7
- 7002 A8
- 7003 B7
- 7004 C8
- 7005 B4
- 7006-1 H11
- 7006-2 H12
- 7112 F2
- F001 F10
- F002 F10
- F003 C13
- F004 E14
- F005 E14
- F006 E14
- F007 E14
- F008 F9
- F009 F9

Layout Digital Board Chrysalis 2.1 (Top View)



0605 D1	2707 A3	3164 D3	3403 C2	3719 A2	4407 B2
0609 D3	2711 A2	3167 D3	3404 C2	3727 A3	4702 A3
1001 A3	2717 A2	3168 D3	3405 D2	3805 C2	4703 A3
1100 C3	2722 A2	3170 D3	3406 D2	3806 D2	4728 A2
1102 C3	2723 A2	3172 D3	3407 C2	3807 D2	4729 A2
1103 A3	2724 A2	3175 D3	3408 C2	3820 B1	4730 A2
1104 A2	2725 A2	3176 D3	3410 C2	3821 B1	4804 C3
1105 C3	2728 A2	3178 D3	3411 C2	3822 B1	4812 C3
1106 B3	2729 A2	3180 D3	3413 C2	3823 B1	4813 C2
1200 A1	2832 D2	3204 B1	3416 C2	3824 B2	4814 C2
1203 A1	2833 D2	3206 A1	3417 C2	3825 B2	4905 A3
1400 C1	2900 A3	3208 B1	3419 C2	3826 B2	4907 A3
1500 B3	2901 A3	3209 A1	3420 C2	3827 B2	4908 A2
1505 B3	2903 A3	3210 B1	3421 C2	3828 C1	4909 A2
1704 A2	2904 A3	3211 B1	3423 C2	3829 C1	5002 B3
1900 A1	2905 A3	3212 A1	3424 C1	3830 C1	5005 B3
1901 A2	2906 A3	3213 A1	3425 C1	3831 C1	5008 B3
1904 A3	2907 A3	3214 B1	3426 C1	3832 C2	5009 B3
2000 B3	2908 A3	3215 B1	3427 C1	3833 C2	5011 B3
2001 B3	2909 A3	3216 A1	3428 C1	3834 C2	5102 D3
2002 B3	2910 A2	3217 B1	3429 C1	3835 C2	5108 D2
2003 B3	2912 A3	3218 B1	3430 C1	3836 C2	5200 A1
2014 B3	2914 A3	3220 B1	3431 C1	3840 C1	5201 B2
2015 A3	2915 A3	3221 B1	3432 C1	3850 C1	5202 A1
2023 B3	2918 A2	3223 A1	3436 C1	3853 C1	5203 A1
2026 A3	2919 A1	3225 B1	3437 C1	3854 A3	5204 B1
2033 B3	2920 A2	3228 B1	3438 C1	3855 D2	5300 B1
2035 A3	2922 A2	3229 B1	3439 C1	3902 A3	5301 B1
2037 A3	2924 A3	3230 A1	3440 C1	3905 A3	5302 B1
2044 B3	2926 A3	3231 B1	3442 D2	3906 A3	5400 D2
2046 A1	2927 A3	3232 A1	3443 D1	3907 A3	5404 C1
2049 B3	2930 A1	3233 A1	3444 D1	3908 A3	5700 B2
2050 B3	2931 D3	3234 A1	3445 D1	3909 A1	5710 A3
2054 A3	2933 A3	3235 B1	3446 D1	3910 A1	5802 D1
2056 A3	2935 A3	3236 B1	3447 D2	3911 A3	5804 D2
2058 A3	2936 A3	3237 B2	3448 D2	3912 A3	5808 D2
2059 A3	2938 D3	3238 B1	3449 D2	3913 A1	5809 D2
2060 B3	2939 A3	3239 B2	3450 D2	3914 A1	5902 A3
2062 B3	2940 A3	3240 A1	3451 D2	3916 A1	5903 A3
2064 A3	3005 B3	3241 B2	3452 D1	3917 A2	5904 A2
2065 A3	3008 B3	3242 B1	3453 D2	3918 A3	5905 A1
2071 A3	3010 B3	3243 B2	3454 D2	3919 A3	5906 A1
2100 D3	3013 A3	3244 B2	3455 D2	3922 A2	5908 A3
2102 C3	3015 B3	3245 B1	3456 D2	3924 A3	5909 A1
2104 C3	3016 B3	3246 B2	3457 D2	3926 A3	5910 A3
2105 C3	3017 B3	3247 B2	3458 D2	3929 A2	5912 A3
2106 C3	3018 B2	3248 A1	3459 D2	3930 A3	5914 A2
2107 C3	3019 B3	3249 B2	3460 D2	3931 A3	5915 A2
2109 C3	3023 A3	3251 B2	3461 D2	3934 A3	6103 D3
2110 C3	3026 A3	3252 B2	3462 D2	3936 A3	6200 B2
2111 C3	3085 C1	3254 B2	3463 D2	3938 A3	7001 B3
2116 D3	3086 C1	3255 B2	3464 D2	3941 A3	7004 B3
2127 D2	3087 A1	3256 B2	3465 D2	3942 A3	7008 C3
2128 D3	3088 C1	3257 B1	3466 D2	3943 A3	7102 D3
2200 A1	3094 C3	3258 B2	3467 D2	3944 A3	7200 A1
2201 A1	3101 C3	3259 B2	3468 D2	3945 A3	7201 A2
2204 A1	3103 C3	3260 A2	3469 D2	3946 A3	7202 B2
2205 A1	3104 D3	3261 A1	3470 D2	3947 A3	7300 B1
2212 B1	3106 C3	3270 A2	3471 D2	3950 A3	7301 B1
2235 A1	3108 C3	3271 A2	3472 D2	3951 A3	7303 C1
2236 A1	3110 C3	3272 A2	3473 D2	3952 A3	7304 C1
2238 B1	3112 C3	3273 A2	3474 D1	3953 A3	7305 B1
2300 B1	3113 D2	3275 B2	3475 D1	3954 A3	7400 C2
2301 B1	3116 C3	3276 A2	3476 D1	4001 B3	7402 C1
2302 B2	3118 C3	3278 A2	3477 D1	4002 B3	7703 A2
2303 B1	3120 C3	3284 A1	3478 D1	4005 B3	7809 C3
2304 B1	3122 C3	3294 A2	3479 D1	4119 C1	7810 D3
2305 B1	3124 C3	3295 A2	3480 D1	4122 D3	7900 A1
2306 B1	3126 C3	3296 A2	3481 D1	4123 D2	7901 A2
2307 B1	3128 C3	3297 A2	3482 D1	4201 B1	7903 A2
2308 B1	3130 C3	3298 A2	3483 D1	4202 A1	7904 A3
2309 B1	3131 C3	3299 B2	3484 D1	4205 A1	7907 A3
2310 B1	3133 C3	3300 B1	3485 D1	4300 B1	7908 A3
2311 C1	3135 C3	3301 B1	3486 D1	4301 B1	7911 A3
2312 B1	3136 C3	3302 B1	3487 D2	4302 B1	
2400 D2	3138 C3	3303 B1	3488 D2	4303 B1	
2401 D2	3139 C3	3304 B1	3489 D2	4304 C1	
2402 C2	3140 C3	3305 B1	3490 D2	4306 B1	
2403 D2	3141 C3	3306 B1	3491 D2	4307 C1	
2408 D1	3143 C3	3307 B1	3492 D2	4308 B1	
2433 C1	3145 C3	3308 B1	3493 D1	4309 B1	
2435 C2	3147 C3	3309 B1	3494 D2	4311 B1	
2525 B3	3149 D3	3310 B1	3495 D2	4312 B1	
2526 B3	3152 C3	3311 B1	3496 D2	4313 B1	
2700 B3	3154 D3	3316 B2	3497 C1	4315 B1	
2703 A2	3156 D3	3317 B2	3498 C1	4316 C1	
2704 B2	3157 C3	3318 B2	3499 C1	4404 B2	
2705 B2	3159 D3	3319 B2	3702 B2	4405 B2	
2706 A2	3161 D3	3402 D2	3715 A2	4406 B2	

Layout Digital Board Chrysalis 2.1 (Bottom View)



1000 B1	2409 C2	3007 B1	3291 B2	3956 A2	7107 B3
1201 A3	2410 C2	3009 A1	3292 B3	4003 B1	7108 A2
1401 C3	2411 C2	3011 B1	3293 B3	4004 B1	7111 B1
1506 C1	2412 C2	3012 B1	3315 A2	4007 A1	7112 B1
1507 C1	2413 C2	3014 B1	3320 A2	4101 D1	7302 B3
2004 B1	2414 C3	3020 B1	3400 D2	4110 B3	7401 B2
2005 B1	2415 C3	3021 A2	3401 D2	4111 B1	7500 C1
2006 B1	2416 C2	3022 B1	3409 C2	4113 B2	7501 C1
2007 C1	2417 C2	3024 A1	3412 C2	4115 B3	7701 A1
2008 C1	2418 C3	3025 A1	3414 C2	4116 C3	7702 A2
2009 B1	2419 C3	3080 B1	3415 C2	4117 B2	7801 C1
2010 B1	2420 C2	3081 A2	3418 C2	4118 C3	7802 D1
2011 B1	2421 C2	3082 B1	3422 C2	4121 B2	7803 C1
2012 C1	2422 C3	3090 B3	3433 C2	4203 A2	7804 D3
2013 C1	2423 C2	3091 B3	3434 C2	4204 A2	7805 C2
2016 A1	2424 C3	3092 B1	3435 C3	4305 B3	7806 D1
2017 A1	2425 C3	3093 B1	3503 C1	4310 B3	7807 C1
2018 A1	2426 C3	3095 B3	3504 D1	4314 B3	7808 D2
2019 B1	2427 C2	3096 C3	3700 A2	4401 C3	7811 C2
2020 B1	2428 C2	3097 B1	3701 A2	4402 C3	7812 D3
2021 B1	2429 C3	3098 B1	3703 A1	4403 C3	7813 D2
2022 A1	2430 C3	3099 B1	3704 A1	4500 C1	7814 D1
2024 B1	2431 C3	3100 B1	3705 A1	4701 A1	7902 A2
2025 B1	2432 B2	3102 D1	3706 A1	4800 C1	7905 A2
2027 B1	2512 C1	3105 C1	3707 A1	4801 C1	7906 A1
2028 B1	2514 C1	3107 C1	3708 A2	4802 C2	7909 A1
2029 B1	2515 D1	3109 D1	3709 A2	4803 D1	7910 A1
2030 B1	2516 C1	3111 C1	3710 A2	4805 D1	7912 A1
2031 B1	2518 D1	3114 B2	3711 A2	4806 D1	
2032 B1	2519 B1	3115 C1	3712 A2	4807 D1	
2034 B1	2521 B1	3117 B2	3713 A2	4808 C2	
2036 A1	2524 B1	3119 C1	3714 A2	4809 C1	
2038 B1	2527 D1	3121 A2	3716 A2	4815 D3	
2039 B1	2701 A2	3123 A2	3717 A2	4816 D2	
2040 B1	2708 A2	3125 A2	3718 A2	4817 D2	
2041 B1	2709 A2	3127 A2	3720 A2	4818 D2	
2042 B1	2710 A1	3129 A3	3721 A2	4819 D1	
2043 B1	2712 A2	3132 C3	3722 A2	4822 C1	
2045 B1	2714 A2	3134 A2	3723 A2	4900 A2	
2047 B1	2715 A2	3137 A2	3724 A2	4901 A2	
2048 A1	2716 A2	3142 C3	3725 A2	4902 A2	
2051 B1	2719 A2	3144 A2	3726 A2	4903 A1	
2052 B1	2720 A2	3150 B1	3801 C1	4904 A1	
2053 B1	2721 A2	3162 B3	3802 D1	4906 A1	
2055 B1	2726 A1	3163 B3	3804 D2	4910 A2	
2057 B1	2727 A1	3165 B3	3808 D1	4911 A3	
2061 A1	2806 D2	3173 B3	3809 D1	5001 A1	
2063 A1	2807 D2	3184 B3	3810 D1	5003 B1	
2066 B1	2808 D2	3185 A1	3811 D1	5010 A1	
2067 B1	2809 D3	3186 B1	3812 D1	5100 B3	
2101 B2	2810 D2	3187 B3	3813 D1	5103 B1	
2103 B3	2811 D3	3189 B1	3814 D1	5104 B1	
2108 D1	2812 D2	3191 B1	3815 D1	5401 C3	
2112 A1	2814 D3	3192 B1	3816 C1	5402 D3	
2113 B2	2818 D1	3195 B1	3817 C1	5403 B2	
2119 B1	2819 D1	3197 B1	3818 C2	5405 C3	
2120 B1	2820 D2	3199 B1	3819 C2	5406 C2	
2124 B1	2821 D2	3200 A2	3837 B2	5501 C1	
2125 B3	2822 D2	3202 A2	3838 B2	5502 C1	
2202 A3	2823 D2	3203 B3	3839 B2	5503 C1	
2203 B3	2824 D2	3205 A3	3841 D2	5701 A2	
2206 A3	2825 D2	3207 A3	3842 D2	5702 A2	
2207 A3	2826 D2	3219 B3	3843 D2	5703 A2	
2209 A3	2827 D1	3222 B3	3844 D2	5704 A2	
2210 A3	2828 D2	3224 C2	3845 D2	5705 A2	
2214 A3	2829 D2	3226 C2	3846 D2	5706 A2	
2215 A3	2830 D2	3227 C2	3847 D2	5707 A2	
2217 A3	2834 D1	3250 B2	3848 C2	5708 A2	
2218 A2	2836 C2	3253 A3	3849 C1	5709 A2	
2219 A3	2902 A1	3262 B2	3851 C3	5711 A2	
2220 A2	2911 B1	3263 B2	3852 C3	5712 A1	
2221 B3	2913 A1	3264 B2	3901 A1	5803 D1	
2222 B2	2916 A1	3265 B2	3903 A2	5805 D1	
2223 A2	2917 A1	3266 B2	3904 A2	5901 A2	
2224 A2	2921 A3	3267 B2	3915 A2	5907 A1	
2225 B2	2923 A2	3268 B2	3920 A1	5911 A1	
2226 B2	2925 A1	3269 B2	3921 A1	5913 A1	
2227 B3	2928 A1	3274 A2	3923 A2	5916 A3	
2228 B2	2929 A1	3277 A2	3925 A2	6000 A1	
2229 A3	2932 A1	3279 A2	3927 A1	6100 B2	
2230 A2	2934 A1	3280 A3	3928 A1	6101 B2	
2231 A3	2937 A1	3281 A3	3932 A1	7002 A1	
2232 A2	2941 A2	3282 A3	3933 A1	7003 A1	
2233 A2	2942 A2	3283 A3	3935 A1	7005 B1	
2234 A3	3000 A1	3285 A3	3937 A1	7100 A2	
2237 A3	3001 B1	3286 B2	3939 A1	7101 A2	
2404 C3	3002 B1	3287 B2	3940 A2	7103 D1	
2405 C3	3003 B1	3288 B3	3948 A1	7104 B3	
2406 C2	3004 A1	3289 B3	3949 A1	7105 A2	
2407 C2	3006 B1	3290 B2	3955 A2	7106 B2	

TR 09013_001
150403

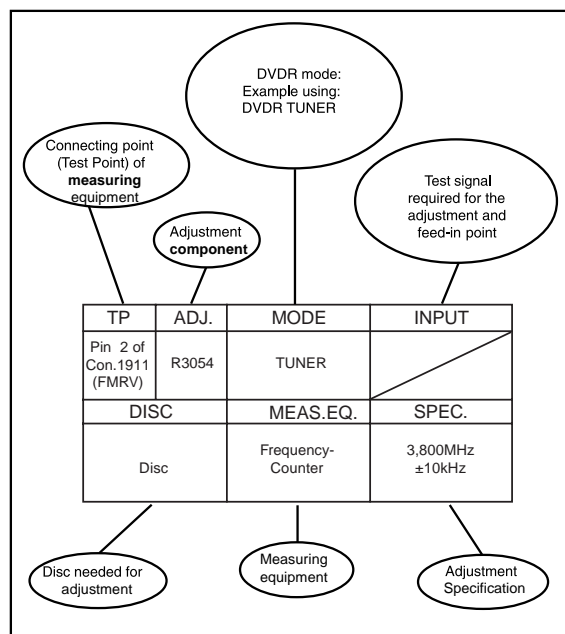
8. Alignments

8.1 Alignment Instructions Analog Board

Test equipment:

- Dual-trace oscilloscope
Voltage range : 0.001 ~ 50 V/div
Frequency : DC ~ 50 MHz
Probe : 10:1, 1:1
- DVM (Digital voltmeter)
- Frequency counter
- Sinus generator
Sinus : 0 ~ 50 MHz
- Test pattern generator

How to read the adjustment procedures:



Front End (FV)

Service tasks after replacement of IC 7710, coil L5710 and L5711:

1 AFC Adjustment:

Purpose: Correct adjustment of demodulator AFC - circuit

Symptom, if incorrectly set:

Bad or disturbed TV channel reception.

PAL - AFC adjustment [5711]:

TP	ADJ.	MODE	INPUT
IC 7710 Pin 17 (F708)	L5711	TUNER	38,9MHz 500mV _{pp} at Tuner 1705, Pin 11 (F710, IF-out)
DISC		MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,1V

Storage in NVRAM via command mode interface of DSW:

After adjustment, the AFC reference value has to be stored in the NVRAM.

This reference value is 256 * measured voltage/Ucc. Ucc is 5.0V.

Store the reference value via command 732, followed by the ref. value.

Example: DD:> 732 128

2 HF - AGC adjustment [3724]:

Service tasks after replacement of IC 7710:

Purpose: Set amplifier control.

Symptom, if incorrectly set:

Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F710, IF-out)	R3707	Set tuned to channel 25 503.25 MHz	5mV(74dBμV) on aerial input PAL white picture, audio IF on, no modulation
DISC		MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	500mV _{pp} +/-0.5dB (use a 10:1 probe)

3 Attenuating the 40.4 MHz [5710]: (SECAM only)

Service tasks after replacement of coil 5710:

Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:

Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1701 Pin 1 (F709)	L5710	TUNER	40.4 MHz, 200mV _{rms} at Tuner 1705, Pin 11 (F710, IF-out)
DISC		MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjust minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1701] must be smaller than the input signal amplitude by at least 6 dB.

8.2 Reprogramming Procedure of NVM on the Microprocessor Sub PCB

The NVM, item 7808, on the Microprocessor Sub board contains the following factory settings:

1. Clock correction factor
2. AFC reference value
3. Slash version

The settings 1,2 and 3 are stored in the NVM during the production of the analogue board.

The slash version is stored at the end of the production line of the set.

In case of failure, the NVM must be replaced by an empty device. By way of commands via the Diagnostic Software or via ComPair, the factory settings must be restored in the NVM.

8.2.1 Clock Correction Adjustment

To guarantee an exact function of the real time clock, an adjustment of the clock frequency is possible. The adjustment value is stored in the NVM.

Procedure:

- put the set in service command mode
- execute command 722 for Digital Board 1.5 Empress or 1117 for Chrysalis to initiate that a signal with 32768 Hz is available on pin 3 of connector 1988
example:
DD:>722 or DD:>1117
- measure the frequency fmeas of the Clock Crystal with an accuracy of 0.1 Hz.
- Calculate the parameter to be entered: $32768/fmeas * 106$
- Normally the parameter must be between 999902 and 1000097. If the parameter and therefore the frequency of the crystal is outside this range, the crystal must be replaced.
- Execute command 721 for Empress or 1118 for Chrysalis with the parameter as input
example:
DD:>721 1000023 (Empress)
or DD:>1118 1000023 (Chrysalis)

8.2.2 AFC Reference Voltage Tuner

This function stores the reference voltage for the tuner in the NVM. Before this value can be stored, the AFC adjustment, described in the adjustment instructions of the analogue board, must be carried out.

Procedure:

- Adjust AFC circuit
- Calculate the reference value
- Execute command 732 for Empress or 1119 for Chrysalis and use the calculated reference value as parameter
example: DD:>732 128 (Empress)
or DD:>1119 128 (Chrysalis)

8.2.3 Slash Version

The slash version is stored with command 715 for Empress or 1217 for Chrysalis, followed by the slash version as parameter. The slash versions used in DVDR75 and DVDR80 are the following:

- DVDR80/00x/02x: SV 65
- DVDR80/05x: SV 66
- DVDR75/00x/02x: SV 67
- DVDR75/05x: SV 68
- DVDR70/00x/02x: SV 69
- DVDR70/05x: SV 70

Example:

DD:>715 65 (Empress)

or DD:>1217 65 (Chrysalis)

Reset of Slash Version

Use command 729 for Empress or 1115 for Chrysalis to reset the analogue board to the default setting.

Procedure:

- Put the set in DSW command mode
- Execute command 729 (Empress) or 1115 (Chrysalis) with the following parameters:
DD:> 729 w 0xAE 2 0xD0 0x00 (Empress)
DD:> 1115 w 0xAE 2 0xD0 0x00 (Chrysalis)
- Leave the DSW command mode and start up the set in application mode
No background is visible on the TV screen. The analogue board is ready to accept the appropriate slash version

8.3 Rework Procedure IEEE Unique Number

8.3.1 Scope:

The procedure describes how to upgrade sets with a unique number after repair. This unique number is stored in the NVRAM (item 7201) of the digital board at the end of the production line.

This procedure is only valid or necessary when:

- The digital board is replaced
- NVRAM on the digital board is replaced
- NVRAM is cleared

In all other cases the repaired set retains its unique number.

The procedure defines several means to re-assure the unique number depending on the possibilities of repair or the state the faulty set is in.

8.3.2 Handling:

State of original (defective) board:

1. The digital board starts up in Diagnostics Mode: follow procedure A to retrieve the valid unique number
2. The digital board does NOT start up in Diagnostics Mode: follow procedure B.

8.3.3 Procedure A

1. Connect defective digital board to PC via serial cable (3122 785 90017)
2. start up hyper terminal or any other serial terminal via the correct settings (DSW command mode interface)
3. read out existing unique number via nucleus 403 (Empress) or 1208 (Chrysalis)
example:
DD:> 403 40300: DV Unique ID = 00D7A1FC6C Test OK @
4. note read out
5. program new digital board via nucleus 410 (Empress) or 1207 (Chrysalis)
example:
DD:> 410 00D7A1FC6C 41000: Test OK @

The set has now the original unique number

8.3.4 Procedure B

- Note the serial number of the set example:
VN050136130156
 - VN = production centre (VN...Szekesfehervar).
According to UAW-500: V=22 and N=14
 - 05 = change code (this is not used for this calculation)
 - 01 = YEAR
 - 36 = Production WEEK
 - 130156 = Lot and SERIAL number
- Calculate the unique number: this number always exists out of 10 hexadecimal numbers.
- First 5 numbers: First we calculate a decimal number according to the formula below: $35828 * \text{YEAR} + 676 * \text{WEEK} + 26 * A + H + 8788$ The figures are fixed, YEAR + WEEK + factory code (A + H) are variable Example: $35828 * 01 + 676 * 36 + 26 * 1 + 8 + 8788 = 68986$ (decimal) Then we translate the decimal number to a hexadecimal number. example: 68986 (decimal) = 10D7A (hex)
- Last 5 numbers: The last 5 numbers exist out of the Lot and SERIAL number.
We have to translate the decimal number to the next 5 hexadecimal numbers: Example: 130156 (decimal) = 1FC6C (hex)
- Program new digital board via nucleus 410 (Empress) or 1207 (Chrysalis). Therefore we use the 10 hexadecimal numbers we calculated above:
example:
DD:> 410 10D7A1FC6C
or DD:>1207 10D7A1FC6C
41000: Test OK @

The set has now its original unique number

8.4 Adjustment DVIO 1.8 PCB

This adjustment sets the free running frequency of the VCO of the audio PLL. It should be carried out after replacement of IC 7604.

- Disconnect DVD+RW set from the mains.
- Plug DVIO1.8 board via edge-connector onto Digital Board (DVIO board is vertically oriented, so that both sides of the PCB are accessible for measurements).
- Connect DVD+RW set to the mains.
- Turn DVD+RW set on and select any video input source except the DV input.
- Check the signal at test point F611 with an oscilloscope. The signal should be 5V digital with 50% duty-cycle.
- Measure the frequency of the signal at test point F610 and adjust the potentiometer 3605 to get a frequency of 12.288MHz 50kHz (after removing the screwdriver from the potentiometer).
 - In case the frequency can not be increased sufficiently, replace capacitor 2618 by NPO-type capacitor with 18pF. Adjust afterwards again the frequency with the potentiometer.
 - In case the frequency can not be decreased sufficiently, add (3pF-10pF) trim-capacitor in parallel to capacitor 2618 or replace capacitor 2618 by NPO-type capacitor with 27pF. Adjust afterwards again the frequency with the potentiometer (and/or trim-capacitor).
- Switch DVD+RW set to Stand-by mode.
- Disconnect the DVD+RW set from the mains.
- Plug DVIO1.8 board directly (without edge connector) onto Digital Board.
- Connect DVD+RW set to the mains.
- Connect a DV-source that transmits DV-video data with audio to the DVD+RW set.
- Turn DVD+RW set on, select DV input, and switch DVD+RW set appropriately to output the decoded signal. Audio should be output without distortion.

8.5 Alignments after replacing the Boot EEPROM 7810 in sets with Digital Board Chrysalis

The NVM, item 7810, on the Digital Board Chrysalis contains the "Diversity String" that tells the software during startup which hardware version is present.

The setting is stored in the NVM during the production of the Digital Board Chrysalis

In case of a fault the NVM must be replaced by a programmed device containing the boot script.

Via the Diagnostic Software the Diversity String is stored with command 1226, followed by the Diversity String as parameter.

The diversity strings used in DVDR70/0x1 and DVDR75/0x1 are the following:

Chrysalis Board Type	String
E1	44424849A8E92001453100000000000230303000101020100000020040000
E1_AV3	444248492721200145315F4156330000320303000101020001000020040000
E2	44424849BAE92001453200000000000024030300000000020100000020040000
E2_AV3	444248493921200145325F4156330000330303000000020001000020040000

Example:

```
DD:> 1226 44424849A8E9200145310000000000023030300000101020100000020040000
122600
Test OK @
```

E1 ...Digital Board Chrysalis version Euro 1 (with DV input) for DVDR75/0x1 with Basic Engine VAE8020.

E1_AV3...Digital Board Chrysalis version Euro 1 (with DV input) for DVDR75/0x1 with Basic Engine VAD8031.

E2 ...Digital Board Chrysalis version Euro 2 (without DV input) for DVDR70/0x1 with Basic Engine VAE8020.

E2_AV3...Digital Board Chrysalis version Euro 2 (without DV input) for DVDR70/0x1 with Basic Engine VAD8031.

With command 1228 the settings can be displayed.

9. Circuit-, IC descriptions and list of abbreviations

9.1 Display Board

9.1.1 Microcontroller

The core element of the Display Control unit is the microcontroller TMP87CH74AF [7110]. The TMP87CH74AF is an 8 bit microcontroller fitted with 32kB ROM and 1kB RAM. It requires 5V supply and is responsible for the following functions:

- Interface to Central Controller-P
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver
- Activation and control of the local display
- Heater voltage generation

The 8 MHz resonator (Pos. 1111) generates the system clock. The reset is generated by the CC-P via "POR_DC"-signal where the transistor [7106] is used as a level-shifter from 3V3 to 5V.

9.1.2 Interface to the Central Control μ P

The communication to the main microcontroller (CC) on the P-Sub-PCB is done via I2C-Interface, where the TMP87CH74AF acts in slave-mode.

An additional wire ("INT"-line) is used to signal the Central controller that data are ready, e.g. when a key has been pressed.

9.1.3 Evaluation of the keyboard matrix

There are 12 different keys on the display board. A resistor network is used to generate a specific direct voltage value, depending on the pressed key. Via the resistors 3107 and 3102 on the analog/digital (A/D) ports (7103 pin 37 and 38) the evaluation is done.

9.1.4 IR receiver and signal evaluation

The IR receiver [7107] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received infra red transmission (approx. 940nm) to electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7107], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is fed into the controller for further processing via port TC1 [7103, pin20].

9.1.5 Vacuum Fluorescence Display

The VFD "BJ900GNK" [POS 7100] is fully controlled by the microcontroller. The μ C also includes the driving stages. Only two additional drivers [POS 7101 and 7102] are necessary for the grids 8 and 9 because of their large size.

9.1.6 VFD Heater Voltage Generator

The circuit around POS [7106, 7108 and 7109] is used to generate a proper AC-Voltage for the filament of the VFD. For this the microcontroller generates an appropriate rectangular signal with 50% duty-cycle and a frequency of 30 kHz at pin 19. Pos. [5104] and [2113] are acting as a resonance-circuit. Via Zener-Diode (POS[6100]) and resistors [3119, 3122 and 3123] the two heater-pins of the VFD ("FIL1" and "FIL2") are clamped so that the grids and segments can be fully switched off.

9.1.7 REC-LED

The REC-LED-ring is made with 3 red LED, controlled via pin 3 (only for flashing) and pin 12 for on/off switching, of the microcontroller. The POS [7105] is used as a driver for the led.

9.1.8 EPG-LED

The EPG led is a white led and controlled from the pin 14 from the microcontroller. The POS [7110] is used as a driver for the led.

9.1.9 TRAY-LED

There are 6 leds (chip) necessary to illuminate the tray, these 6 leds are located on a little sub-pcb connected over a 4 pin connector POS [1911] from the DC-print. The leds are controlled from pin 11 of the microcontroller.

9.2 Microcontroller Sub Board (UP SUB Board)

9.2.1 General

This small PCB is directly soldered in on top of the Analogue-Board.

It is used with no diversity in all three different basic versions (Europe, NAFTA and APAC-Pal). Only the software being loaded into the external Flash-memory is not the same.

9.2.2 Microcontroller

The main part of the Sub-PCB is the central controller (CC) μ P [7804] TMP91CW12AF, which is a 16-bit CPU with 128kBROM and 4kB RAM.

It works with a 3V3 supply and a system clock of 24,576MHz [1801].

The 3V3-supply is made out of the "5VSTBY" by the circuit around [7816].

After connecting the set to the mains (power-up) the IC [7806] generates a reset pulse. This signal ("IPOR") is directly fed to first priority interrupt input (pin 63) for power fail detection and also to the Reset-Input of the CC (Pin30) via [7802], which is necessary to generate a reset only during power-up. In case of power fail pin 30 of the CC must be kept high (3V3).

The internal memory of the CC is too small for all necessary demands. Therefore an external Flash-ROM [7805] with 1MByte in size and a RAM [7803] with 128kByte are necessary. Both parts are connected to the μ P via a parallel address-/data-bus. The lower eight bus-lines (AD0 to AD7) are multiplexed by [7801] and the "ALE"-signal of the CC.

For updating of the software the external Flash-ROM can be reprogrammed by the μ P. During this process [7807] is switched on by the "WE"-signal.

When no mains is connected, the CC is supplied via Gold-Cap [2816] during the power backup period. The diode [6802] prevents unwanted current consumption of other components. The internal ROM of the μ P holds the program code for the Real-Time-Clock. Only the microprocessor is supplied by the backup cell, not the external memories and the μ P operates in a low frequency mode with the clock crystal [1805] only (32.768 kHz). To adjust the clock the frequency can be measured at pin 87 of the μ P in a special test-mode.

9.2.3 Control-Interfaces

The CC is communicating with the digital board via a serial connection, which operates at a speed of 19,4 kbit/s ("D_DATA"-, "A_DATA", "D_RDY"- and "A_RDY"-signal on

[1986]). By generating a high level on pin 16 of the CC the digital PCB can be reset (inverter [7817] in between). Most of the other parts are controlled by the μ P via I2C-bus ("SDA"- and "SCL"-signal). The FETs [7821] and [7822] are used for adaptation of the 3V3-level on CC-side to the components supplied with 5V. The CC can also reset the display-board- μ P by pulling pin 39 to high.

The transistor [7819] acts as a level shifter for the "INT"-signal. In the European sets a bi-directional interface is established between the recording unit and the TV device at pin 10 of the Scart ("P50"-line/Easy Link). The processing is done via pin 14 (output) and pin 38 (input) of the CC and the circuit around [7813], [7814] and [7815].

9.2.4 EEPROM

The EEPROM M24C16 [7808] is an electrical erasable and programmable, non-volatile memory. The EEPROM stores data specific to the device, such as the AFC-reference value of the Europe IF-part, the clock-correction-factor, etc. It is accessed by the μ P via the I2C-bus.

9.2.5 Sync Separator

To detect whether a video signal is available or not a separate IC [7825] is used to extract the sync information out of the video signal that is also routed to the digital board for recording. While on the input a low-pass-filter ([2823] and [3869]) limits the bandwidth an additional filter (circuit around [7818]) on the output avoids distortions. Afterwards the sync-signal is routed to pin11 of the CC.

9.2.6 Fan Control

To avoid unwanted temperatures inside the set (especially the Laser on the OPU of the drive is very sensitive) a fan is located on top of the basic engine. The speed control is dependent on the ambient temp. A NTC resistor [3134] located on the display board measures the temperature. An operational amplifier [7902-B] generates a proper voltage, which is then fed to the engine ("BE_FAN"-line). Below 28°C ambient temp. the fan-voltage is approx. 5V and is increased to 10V when the ambient temperature goes up to approx. 38°C. The second part of the Op-Amp. [7902-A] prevents damage of any temperature-sensitive part in case the NTC or the wire in between is damaged. It acts as a comparator and pulls the "BE_FAN"-signal to 10V. As the fan has to be stopped in case the tray of the drive is open this voltage is "killed" by the CC ("FAN_OFF"-signal). The double-diode [6901] acts for both Op.-Amp.-circuits. The circuit is also prepared for a set-fan (circuit around the Op-Amp. [7902-C]).

9.3 Analog board Europe

9.3.1 General

This PCB consists out of the following parts:

- Power-Supply-Unit
- Frontend (Audio & Video)
- Input-/Output-switching
- Audio ADC- & DAC-processing
- VPS/PDC- and Text-Data slicer
- Analog Follow-Me Circuit

All functional groups are either controlled via I2C-bus or via separate signal lines by the Central-Controller on the μ P-Sub-Board. This sub board is directly soldered in onto the analog PCB. During Stand-By mode of the set, several parts are not supplied (Tuner, MSP, ...). The microprocessor is running and maintains the clock of the set.

To avoid bus blockades the I2C-bus ("SCLSW" & "SDASW") to/from these units is decoupled via transistors [7419], [7420] from the general bus ("SCL" & "SDA").

9.3.2 Power Supply Unit

Functional principle:

This power supply works in the way of a flyback converter. In the mains input part [1931 to 2309], the mains voltage is rectified and buffered in the capacitor [2309]. From this direct voltage at [2309] energy is transferred into the transformer [5300, pins 7-5] during the conductive phase of the switching transistor [7307] and is stored there as magnetic energy. This energy is passed to the secondary outputs of the power supply in the blocking phase of the switching transistor [7307]. With the switch-on time of the switching transistor [7307], the energy transferred in every cycle is regulated in such a way that the output voltages remain constant regardless of changes in the load or mains voltage. The power transistor is driven by the integrated circuit [7313].

Mains input part:

The mains input part extends from the mains socket [1931] to the capacitor [2309]. The diodes [6301, 6302, 6305 and 6306] rectify the AC supply voltage, which is then buffered by the capacitor [2309]. The common mode coil [5302] and capacitor [2302] work as a filter to block interference arising in the power supply from the mains. Components [1302], [3306] and [3304] protect the power supply against short-term over voltages in the mains, e.g. caused by indirect lightning.

Start-up with Mains-on:

After connecting the power cord to the mains, the capacitor [2325] is loaded via a current source between pin 8 and pin 1 in the IC [7313]. Once the voltage on [2325] and therefore the supply voltage V_{cc} of the IC [7313] has reached approx. 11V, the IC starts up and provides pulses at its output pin 5. These pulses are used to drive the gate of the power transistor [7307]. The frequency of these pulses is depending on load and mains voltage. The current consumption of the IC is approx. 5 mA at V_{cc} in normal mode.

If V_{cc} drops to below approx. 9V (e.g. with power limitation) or if V_{ac} exceeds approximately 16V (e.g. interruption of the control loop), the output of the IC [7313, pin 5] is blocked and a new start-up cycle begins. (See also "Overload, Power Limitation, Burst Mode" section)

Normal operation:

With the power supply in normal mode, the periodic sequences in the circuit are divided primarily into the conductive and blocking phase of the switching transistor [7307]. During the conductive phase of the switching transistor [7307], current flows from the rectified mains voltage at capacitor [2309] through the primary coil of the transformer [5300, pins 7-5], the transistor [7307] and resistors [3321, 3352] to ground. The positive voltage on pin 7 of the transformer [5300] can be assumed as constant for a switching cycle. The current in the primary coil of the transformer [5300] increases linearly. A magnetic field representing a certain value of the primary current is formed inside the transformer. In this phase, the voltages on the secondary coils are polarized such that the diodes [6300, 6303, 6307, 6308, 6310, 6313, 6317 and 6319] block. From the controller [7315] a current is supplied into the CTRL input on the IC [pin 3, 7313] via optocoupler [7314]. Once the switch on time of the switching transistor [7307] - that corresponds to the current supplied into the CTRL input - has been reached, the switching transistor [7307] is switched off. When the switching transistor has been switched off, the blocking phase begins. No more energy will be transferred into the transformer. The inductivity of the transformer will still attempt to keep the current flowing at a constant level ($U=L \cdot di/dt$). Switching off transistor [7307] interrupts the primary current circuit. The polarity of the voltages on the transformer is reversed, which means that the diodes [6300, 6303, 6307, 6308, 6310, 6313, 6317 and 6319] become conductive and current flows into the capacitors [2305, 2312, 2319, 2322, 2326 and 2328] and the load. This current is also ramp-shaped (di/dt negative, therefore decreasing).

The feedback control for the switched-mode power supply is done by changing the conductive phase of the switching transistor so that either more or less energy is transferred from the rectified mains voltage at [2309] into the transformer. The regulation information is provided by voltage reference [7315]. This element compares the 5V-output voltage via voltage divider [3332, 3333, 3334] with an internal 2.5V reference voltage. The output voltage of [7315] passes via an optocoupler [7314] for insulation of primary and secondary parts as a current value into pin 3 on the IC [7313]. The switch-on time of the transistor [7307] is inversely proportional to the value of this current.

Overload, power limitation, burst mode:

With increasing load on one or more of the power supply outputs, the switch-on time for the power transistor [7307] increases, and thus also the peak value of the delta-shaped current through this power transistor. The equivalent voltage of this current profile is passed from resistors [3321] and [3352] via [3365] to pin 5 of the IC [7313]. If the voltage on pin 2 reaches approx. 0.4V in one switching cycle, the conductive phase of the switching transistor is ended immediately. The check is done in each individual switching cycle. This process ensures that no more than approx. 60W can be taken out from the mains (= power limitation).

If the power supply reaches the power limit, the output voltages and the supply voltage Vcc on pin 1 of the IC [7313] will be reduced following further loading. If Vcc is less than approx. 9V at any point during this process, the output of the IC [7313, pin 6] is blocked. All output voltages and Vcc decrease and a new start-up cycle begins. If the overload status or short-circuit remains, the power limitation will be activated immediately and the voltages will again decrease, followed by another start-up cycle (Burst Mode). The amount of power taken up from the mains in burst mode is low.

Standby modes:

In the 'AV-Standby' operating mode of the set, the 'ION' control line is primarily used to switch off all output voltages for Basic Engine and Digital Board (supplies 3V3, 5V, 12V, 5N and 4V6 at Connectors 1932 and 1933) of the power supply. This reduces the amount of power taken from the mains. In Low Power Standby mode additionally the 'STBY' control line is used to switch off output voltages 5SW and 8SW. This reduces power consumption to less than 3W, if additionally the display is switched off. The power supply will continue operating in Standby mode with a switching frequency of approx. 25 kHz.

9.3.3 Frontend

This unit is designed to support two basic versions, which are distinguished by a different assembly variant only (one for multistandard and the second for Pal-I only) and comprises the following parts:

- Tuner UV1316K [1705]
- IF amplifier & video demodulator IC TDA 9818/9817 [7710]
- Sound processor MSP3415G [7600]

Tuner and IF selection

The Tuner [1705] converts the RF-signal coming from the antenna input to an IF-signal. The tuner is fully controlled via I²C-bus of the CC-μP. [1705] is also equipped with a "passive-loop-through" between antenna-in and -out to save power in stand-by of the set, when the complete part is not supplied. The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (34,0 MHz).

A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1701], [1703] for video, [1702] for audio. [1701] is switched into the signal path for DK/I-SECAM L/L' reception, if the signal "SFS_TS" is "high". In this case the switches [7704], [7705] are open and the diode [6703] is conducting. [1703] is switched into the signal path for BG reception ("SFS_TS" is "low"). Then the switch [7712] is open and the diode [6704] is conducting. For DK/I-SECAM L/L'

reception, an additional circuit for suppressing the audio carrier of the adjacent channel is used. This circuitry is adjusted by coil [5710] for maximum suppression at 40.4MHz.

IF demodulator

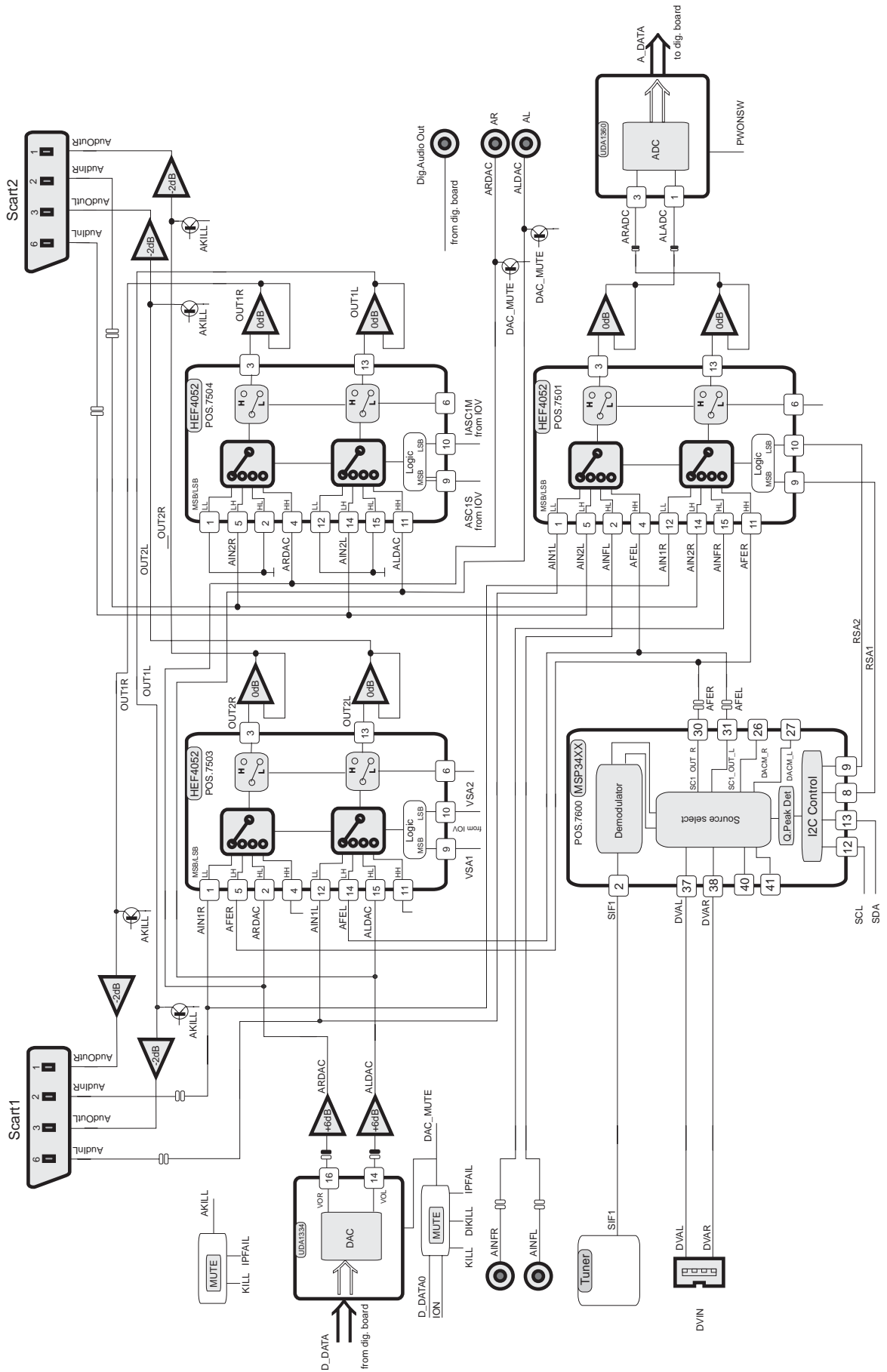
The signal from the tuner and IF-selection circuit is processed by the demodulator IC TDA 9818/9817 [7710]. The signal "PSS" to pin 3 switches between demodulation of positive (SECAM only) or negative modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L'. If the signal "SB1" is "high", the switch [7714] is closed and the diode [6705] is not conducting. For all other standards the diode [6705] is conducting and the switch [7714] is open. The output signal of this SAW filter is firstly processed in the TDA 9818. Audio carriers are converted from the tuner IF level to the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5711] on the TDA 9818/9817 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of [7710] is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3710] to ground. The switch [7701] and the signal "SB1" do this. The HF-AGC is set using the potentiometer [3724] so that, with a sufficiently large antenna input signal (74 dBμV), the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out when the audio carrier is switched off. The demodulated video signal appears on pin 16 of [7710]. The AGC voltage at pin 4 is used to determine the antenna signal strength after a buffer [7717] with the signal "AGC" and an analog input port of the CC-P. The trap [1704] reduces the sound carrier remainders in the video for BG standards. The trap [1706] works in the same way for the Pal-I standard only. For all other standards the switch [7713] is closed via [7706] and "SFS_TS"-line set "high" to bypass this trap. In these cases the selectivity of the SAW filter [1701] is sufficient. The coil [5713] for non-BG standards realizes a frequency response correction. This correction is not desired for SECAM L' and therefore short-circuited by [7716] (signal SB1 is "high" and [7702] has on-status). The demodulated video signal "VFV" is available after the buffer and limiting stage for noise peaks [7711]. The FM-PLL demodulator function of TDA 9818 is not necessary and therefore deactivated by the resistor [3739].

Audio demodulator

The sound demodulation is done by the MSP3415 [7600], which is also fully controlled via I²C-bus by the CC-P (determination of bandwidth, amplitude, standard, ...). The audio signals are available at pin 30 and pin 31 of [7600] and fed as "AFER"- & "AFEL"-line to the audio-I/O for further processing.

9.3.4 Audio routing

Audio IO Europa Overview



11.03.2002 Vers. (

The processing of audio is always done in stereo (e.g. separate left- and right-channel) and the complete switching is realized by using HEF4052, which is a dual four-to-one multiplexer. In principle there are three independent selectors:

a) Scart 1-Output-Path:

Pos [7504] is used to select either Scart 2-Input ("AIN2L"/"AIN2R") or the signal directly from the audio DAC [7004] ("ALDAC"/"ARDAC") as the output source for Scart 1 ("AOUT1L"/"AOUT1R").

The control is done by means of the lines "ASC1S" coming from [7408] (IC [7408] acts as a port expander for the CC-P) and "IASC1M", which is directly coming from the CC. Pos [7412] is used for level adaptation (3V3 to 5V) for the "IASC1M"-signal.

b) Scart 2-Output-Path:

Pos [7503] selects between Scart 1-Input ("AIN1L"/"AIN1R"), signals from the internal frontend ("AFEL"/"AFER") via MSP [7600] or audio directly from the DAC [7004] ("ALDAC"/"ARDAC"). The outputs of this switch are routed to Scart 2 ("AOUT2L"/"AOUT2R"). This switch is controlled via "VSA1"- and "VSA2"-line. These lines come from [7408] that is acting as a port expander for the CC-P.

c) Record-Path:

Pos [7501] selects either signals from Scart 1 ("AIN1L"/"AIN1R") or Scart 2 ("AIN2L"/"AIN2R") or Cinch-Front ("AINFL"/"AINFR") or the MSP [7600] ("AFEL"/"AFER") and routes to the audio ADC [7007] ("ALADC"/"ARADC") for record purposes. The switch is controlled via "RSA1"- and "RSA2"-signals.

These signals come from the MSP [7600], which acts as a port expander of the CC-P. As there can also exist a fifth input in case of DV-In is present the corresponding analog audio signals from the DVIO-board are firstly routed via extra cable and connector [1960] to the MSP. The MSP acts as a preselector between audio from internal frontend or the DV-Input.

Each of these three selectors ([7501], [7503] & [7504]) has a separate Op-Amp on the output for level-adaptation-, performance- and line-driving-reasons. [7505-A & -B] for record, [7502-C & -D] for Scart 1-Output and [7502-A & -B] respectively for Scart 2. Every audio output line on the two Scart connectors can be "killed" (muted) by an extra transistors ([7506], [7508], [7509] & [7511]), which can be activated by the "AKILL"-line. This signal is generated by the circuit around [7404]/[7421] and is a combination of the "KILL"- from the CC-P and the "IPFAIL" of the power-supply-unit.

d) Line-Out-Path:

see chapter 9.3.5

e) Digital Audio Output-Path without IOE-Print:

Additionally to analog audio the set is also equipped with a digital output via cinch plug [1951]. The signal is generated on the dig. board and routed via audio interface cable and connector [1900] to the Ana-PCB. Here the "DAOUT"-line first passes a 6-fold inverter [7580] being used as a driver and for performance reasons (noise reduction, jitter, etc.). Afterwards a transformer [5580] is necessary to achieve the correct level and also to have a floating output with isolated ground before the signal is fed via [3580] to cinch plug [1951]. The capacitor [2580] performs an AC-coupling between connector- and set-ground.

f) Digital Audio Output-Path with IOE-Print:

In case of usage of the IOE-print the digital audio signals (input and output) are directly routed from digital board via interface cable to plug [1920] on the IOE-print. The "DAOUT"-line is splitted into two signals, one for cinch out and one for optical out. The signal to cinch out first passes a 5-fold inverter [7250] being used as a driver and for performance reasons (noise reduction, jitter, etc.). Afterwards a transformer [5250] is necessary to achieve the correct level and also to have a floating output with isolated ground before the signal is fed via [3259] to the cinch plug [1925] (or [1926-B] in case of option

"DIGITAL IN"). The capacitors [2256] and [2266] perform an AC-coupling between connector- and set-ground. The second "DAOUT"-signal is fed directly via [3264] to the optical out transmitter [6255].

g) Digital Audio Input-Path with IOE-Print:

There are two possibilities for a digital audio input signal in case of option "DIGITAL IN". One is the signal from the optical receiver [6259], which is routed via [3269] directly to plug [1920]. The second is the signal from the cinch plug [1926-A]. This signal then passes an inverting amplifier [7250-6] and is then routed via [2253] to the plug [1920].

9.3.5 Audio ADC/DAC

a) PCBs with AD1852 [7004]:

The conversion of analog audio signals from the record-selector [7501] in the I/O ("ALADC"- & "ARADC") is done via UDA1361TS [7007]. This IC can process input signals up to 2Vrms by using external resistors [3047], [3053] in series to the input pins. As the level from the DVIO-Board is only 1Vrms a 6dB step can be performed by setting pin 7 of [7007] to 3,3V via [7008] and the "PWONSW"-line controlled by the CC-P to use the whole dynamic range of the ADC. All required clock signals are generated on the dig. board and only the audio data ("A_DAT"-line) are routed from Ana- to Dig.-PCB for further processing.

The transformation of dig. audio back into the analog domain is done by AD1852 [7004]. All necessary clock signals are coming from the dig. board and dig. audio data ("D_DATA0"-line) are converted into analog signals, which are available at pin 17/16 and pin 12/13 of [7004] as symmetrical signals.

Afterwards an Op-Amp. [7003] (line driver & converting to unsymmetrical signal, gain = 1), which is also working as low-pass-filter to increase signal performance (noise, distortions,...), is passed. Then both signals ("ALDAC" & "ARDAC") are directly routed to the rear cinch output and also used in the audio-I/O for further processing. The DAC has also a mute possibility, which can be activated by setting pin 23 to 5V via [7001]. This mute is controlled either by the dig. board ("D_IKILL"-line) or the "IPFAIL"-signal from power-supply-unit (in this case it's the combination of "A_KILL" and "IPFAIL").

If the DAC is muted externally via pin 23 or if there are no audio data available (e.g. "D_DATA0"-line zero), the output pins 8 and 22 of the DAC change to high (+ 5V). These two signals are then combined with diode pos. 6006. After decoupling via [7009] the signal "DAC_MUTE" is used as mute signal for the mute transistors [7415], [7416] for cinch rear out.

b) PCBs with UDA1334BTS [7001]:

The conversion of analog audio signals from the record-selector [7501] in the I/O ("ALADC"- & "ARADC") is done via UDA1361TS [7005]. This IC can process input signals up to 2Vrms by using external resistors [3039], [3041] in series to the input pins. As the level from the DVIO-Board is only 1Vrms a 6dB step can be performed by setting pin 7 of [7005] to 3,3V via [7006] and the "PWONSW"-line controlled by the CC-P to use the whole dynamic range of the ADC. All required clock signals are generated on the dig. board and only the audio data ("A_DAT"-line) are routed from Ana- to Dig.-PCB for further processing.

The transformation of dig. audio back into the analog domain is done by UDA1334BTS [7001]. All necessary clock signals are coming from the dig. board and dig. audio data ("D_DATA0"-line) are converted into analog signals, which are available at pin 14 and pin 16 of [7001]. Afterwards an Op-Amp. [7002] (line driver & level adaptation, gain = 2) which is also working as low-pass-filter to increase signal performance (noise, distortions,...), is passed. Then both signals ("ALDAC" & "ARDAC") are directly routed to the rear cinch output and also used in the audio-I/O for further processing. The DAC has also a mute possibility, which can be activated by setting pin 8 to 3,3V via [7003]. This mute is controlled either by the dig. board

("D_IKLL"-line) or the "IPFAIL"-signal from power-supply-unit (in this case it's the combination of "A_KILL" and "IPFAIL"). In addition to that the DAC [7001] and the cinch outputs can be killed (muted) in case of "digital silence" by the circuit around [7008], [7009] and [7010], when no audio data are available (e.g. "D_DATA0"-line zero).

This function can be also activated via the "ION"-line (set to high during any stand-by mode). To avoid signal distortions (clipping) the mute transistors for cinch rear out [7415], [7416] are decoupled via [7011].

The Video-I/O-switching is basically realized by the matrix switch STV6618 [7408], which is controlled via I²C-bus by the CC. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6 dB-amplification and a 75 Ohms driver-stage inside. This IC includes also several digital outputs, which are used for switching purposes on the analog board. The record selector inside the switch selects between the CVBS from frontend ("VFV"), the input from Scart 1 ("YCVBSIN1") or the signal from Scart 2 ("YCVBSIN2"). Afterwards the signal passes another switch [7411] in which a selection between signals from the front or the preselected ones are done. The output signals of [7411] are fed as "A_YCVBS"- and "A_C"-line to the digital board for further processing.

To reduce the number of external presets there exists only one preset for CVBS- and Y/C-front. The set automatically detects between the two inputs depending on the presence of a video signal (sync separator-circuit on μ P-sub-board) where Y/C has higher priority.

The R/G/B-inputs and the Fast-Blanking-line from Scart 2 are routed over the optional EPG board to the digital PCB. Also all other video signal from the analog board are routed through the EPG board if present. These signals are also available on the corresponding input-pins of the STV6618 to enable a loop-through in AV-Standby. In this mode the set has to behave like a cable between the two Scart-connectors. AV-Standby is activated either by a "high" level on pin 8 of Scart 2 ("active device is present") or by the "WU"-line (wake up). This signal is generated out of the circuit around [7401], [7402] & [7403] and will become "high" if there is a signal on pin 20 of Scart 1- or Scart 2. The detection of the input level on pin 8 of Scart 2 ("8SC2") is done via an analog input of the CC-P (less than 2V means inactive; 4,5V to 7V determines a source with 16:9 picture-ratio and greater than 9,5V is an active 4:3 source). All signals from the digital board ("D_R", "D_G", "D_B", "D_C", "D_Y" and "D_CVBS") are routed to the proper inputs of the STV6618 for amplification and driving purpose before they can be seen on the appropriate Scart outputs. In case of EPG the signals from the digital board are routed through the EPG board where the selection between digital board video or EPG OSD is taken.

The "D_CVBS"- and the "D_Y"-line are passing a 6 dB-amplifier and driver-IC [7410] and are then routed to the CVBS-Cinch and Y/C-out rear. The chroma signal for this Y/C out is coming from the STV6618 - which makes the 6 dB-amplification - and a driver [7406] in between.

The detection of the picture ratio information on the Y/C-input front is made by measuring the DC-level on the Chroma signal via analog input of the CC-P ("WSFI"-line). In case the level is higher than 3,5V the input signal is a 16:9 source. If the level is lower than 2,4V the picture ratio is 4:3.

For generation of the appropriate DC-voltage on the Y/C-out rear the "WSRO"-line is controlled via pin 18 of [7408] by the CC-P (Pin 18 set to low means 4:3, pin 18 set to high determines 16:9).

The control of the switching voltage (Pin 8 of Scart 1) is done via 3-level-pin (nr.2) of the STV6618 [7408] and the transistors [7405], [7407] & [7409]. A "low" on pin 2 of [7408] causes around 11V on pin 8-Scart 1 (e.g. source with 4:3 picture-ratio active). Medium level (2,5V) on pin 2 of the STV6618 generates medium level (approx. 6V) on pin 8-Scart 1 (e.g. active source with 16:9) and a "high" on pin 2 of the STV6618 pushes pin 8-Scart 1 to "low" (e.g. inactive).

9.3.7 VPS/PDC- and Text-Dataslicer

For extraction of relevant information out of the video signal (time controlled recording, net-name-identification, time- & date- download) the STV5348 [7931] is used. Data transfer to/ from the CC is fully done via I²C-bus and the input signal for decoding is the same as the one being routed to the digital board for recording purposes ("A_YCVBS"-line).

9.3.8 Analog Follow-Me

This circuit compares the video signal from the internal frontend ("VFV") of the recorder with that one of the connected TV-set ("CVBS1"). The TV set delivers the signal via Scart-cable. A comparator [7934] and several additional parts ([7932], [7933], ...) are used to compare the two video signals. In case of both input signals are equal the output-line of this circuit ("FOME") is set to low. Detection is made via an input port of the CC-P.

9.4 Analog board NAFTA- & APAC-Pal- version

9.4.1 Frontend NAFTA

[1701] demodulates the video signal from the antenna input. Tuner and IF-demodulator are in one unit. Also a modulator is included in that part. The audio- and video-signal to the modulator are the ones from the selected input or the playback path of the set ("AMCO"- and "D_CVBS"-line). The control of the tuner is fully done via I²C-bus by the CC-P. Via the "MSW"-signal and [7701] the modulator is switched on and off. In opposite to this the antenna loop-through is opened or closed. In the APAC-Pal version POS [1700] is used with the difference that it demodulates only PAL- instead of NTSC-signals and has also no modulator. The "CSW_SSW" line switches the modulator between CH3 or CH4 in the NTSC-version. To achieve optimal tuning the "AFC"-signal is detected by the CC via an analog input; [3701], [3702] and [3703] are used for level adaptation (5V to 3V3). Pos [7700] is a driver for the video signal.

The sound demodulation is realized by the MSP34x5 [7600], which is also fully controlled via I²C-bus by the CC-P (determination of bandwidth, amplitude, standard, ...). The audio signals are available at pin 30 and pin 31 of [7600] and fed as "AFER"- & "AFEL"-line to the audio-I/O for further processing. As this PCB is used for different regions (NAFTA and APAC) either MSP3425 or MSP3415 are assembled.

9.4.2 Audio routing

Audio IO NAFTA / APAC Overview

12.03.2002 Vers. 05

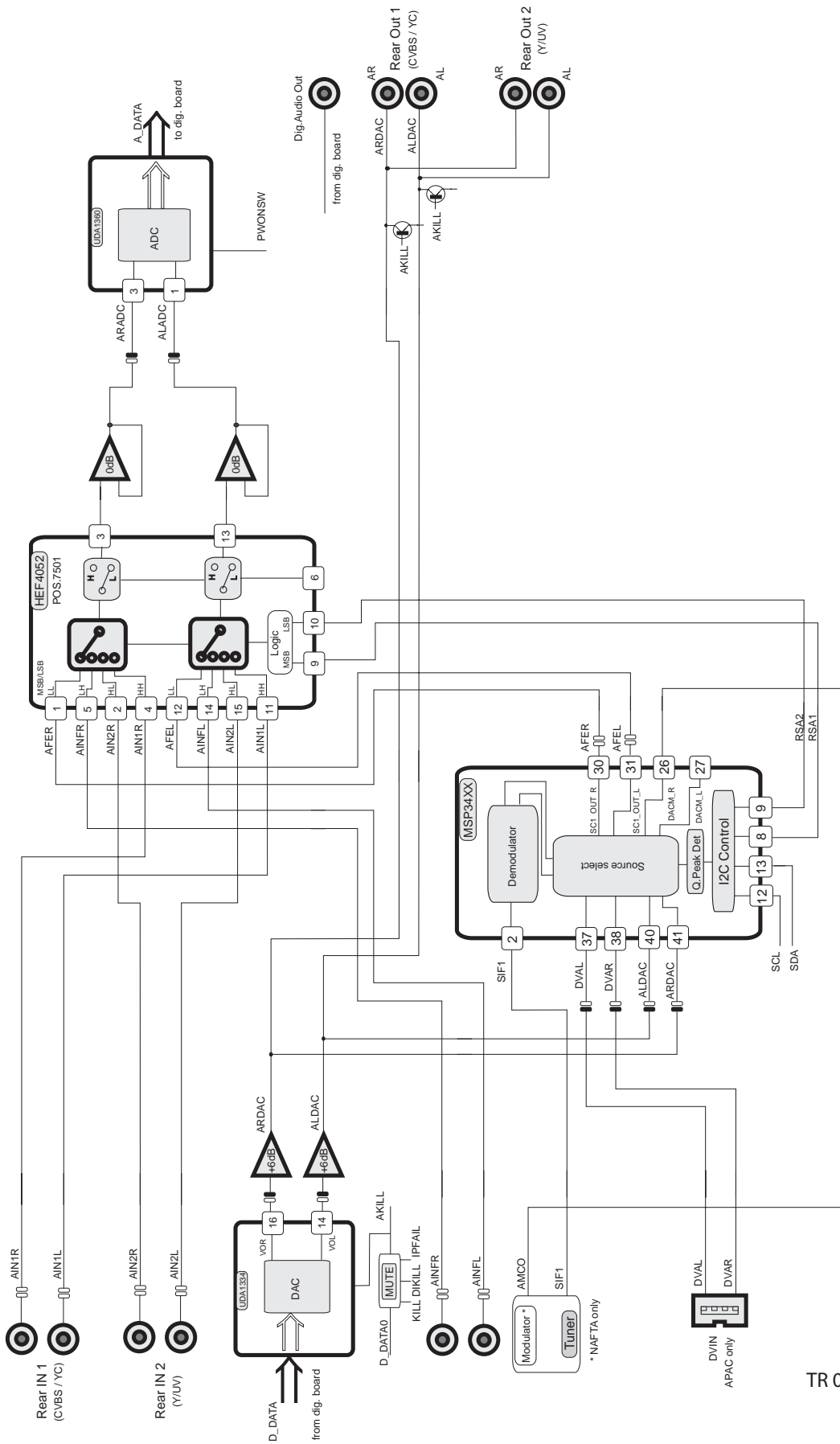


Figure 9-2

TR 01057_001
170502

The sound processing is always done in stereo (that means separate left- and right-channel).

a) Record-Path:

The complete selection of the audio signal for recording is done by a HEF4052 [7501], which is a dual four-to-one multiplexer. The input lines for the selector [7501] are coming either from MSP [7600] ("AFEL"/"AFER") or cinch rear in 1 ("AIN1L"/"AIN1R") or cinch rear in 2 ("AIN2L"/"AIN2R") or the cinch in front ("AINFL"/"AINFR"). The [7501] is controlled via "RSA1"- and "RSA2"-signals coming from the MSP [7600]. The MSP acts as a port expander of the CC-P. The Op-Amp on the output [7504] is necessary for performance reasons and acts also as a driver. The selected signals "ARADC" and "ALADC" are directly fed to the Audio-ADC.

As there can exist also a fifth input in case of DV-In is present the corresponding analog audio signals from the DVIO-board are firstly routed via extra cable and connector [1960] to the MSP, which acts as a preselector between audio from internal frontend or the DV-Input.

b) Line-Out-Path:

see chapter 9.4.3

c) Digital Audio Output-Path without IOE-Print:

Additionally to analog audio the set is also equipped with a digital output via cinch plug [1951]. The signal is generated on the dig. board and routed via audio interface cable and connector [1900] to the Ana-PCB. Here the "DAOUT"-line first passes a 6-fold inverter [7580] being used as a driver and for performance reasons (noise reduction, jitter, etc.). Afterwards a transformer [5580] is necessary to achieve the correct level and also to have a floating output with isolated ground before the signal is fed via [3580] to cinch plug [1951]. The capacitors [2580], [2582] and [2583] perform an AC-coupling between connector- and set-ground.

d) Digital Audio Output-Path with IOE-Print:

see chapter 9.3.4.f

e) Digital Audio Input-Path with IOE-Print:

see chapter 9.3.4.g

9.4.3 Audio ADC/DAC

The conversion of analog audio signals from the record-selector [7501] in the I/O ("ALADC"- & "ARADC") is done via UDA1361TS [7005]. This IC can process input signals up to 2Vrms by using an external resistor [3039], [3041] in series to the input pins. As the level from the DVIO-Board is only 1Vrms a 6dB step can be performed by setting pin 7 of [7005] to 3,3V via [7006] and "PWONSW"-line controlled by the CC-P to use the whole dynamic range of the ADC. All required clock signals are generated on the dig. board and only the audio data ("A_DAT"-line) are routed from Ana- to Dig.-PCB for further processing.

The transformation of dig. audio back to the analog domain is done by UDA1334BTS [7001]. All necessary clock signals are coming from the dig. board and dig. audio data ("D_DATA0"-line) are converted into analog signals, which are available at pin 14 and pin 16 of [7001]. Afterwards an Op-Amp. [7002] (line driver & level adaptation) which also works as a low-pass-filter to increase signal performance (noise, distortions,...) is passed. Then both signals ("ALDAC" & "ARDAC") are directly routed to the rear cinch output. The DAC has also a mute possibility, which can be activated by setting pin 8 to 3,3V via [7003]. This mute is controlled either by the dig. board ("D_IKLL"-line) or the "IPFAIL"-signal from power-supply-unit. In addition to that the DAC [7001] and the cinch outputs can be killed (muted) in case of "digital silence" by the circuit around [7008], [7009] and [7010], when no audio data are available (e.g. "D_DATA0"-line zero).

The signals from the audio DAC part ("ARDAC"/"ALDAC") are directly routed to both cinch rear outputs, which are connected

in parallel. To avoid plops and any other audible noise on the output there is a mute-stage implemented [7509], [7511] for each channel. The activation is done via "AKILL"-line, which is a combination of the "KILL" from CC-P, "DAC_MUTE" from DAC-part and "IPFAIL" from the power-supply-unit. The circuit around [6430], [6431], [7430] and [7404] generates this signal.

The Video-I/O-switching is basically realized by the matrix switch STV6618 [7408], which is controlled via I²C-bus by the CC. All used outputs excluding pin 21 (Y/CVBS-REC) have a 6dB-amplification and a 75 Ohms-driver-stage inside. This IC also includes several digital outputs, which are used for switching purposes on the analog board. The record selector inside the switch selects between the CVBS from frontend, the CVBS from Cinch-Rear or Y from the S-Video-input rear. Afterwards the signal passes another switch [7411] in which a selection between signals from the front or the preselected ones is done. The output signals of [7411] are fed as "A_YCVBS"- and "A_C"-line to the digital board for further processing.

To reduce the number of external presets there is only one station for CVBS or Y/C (front and rear). The set automatically detects between the two inputs depending on the presence of a video signal (sync separator-circuit on μ P-sub-board) where Y/C has higher priority.

The Y/U/V-inputs are routed over the optional EPG board to the digital PCB. Only the Y-line has to be present additionally on pin 4 of [7408] for video recognition. Also all other video signal from the analog board are routed through the EPG board if present.

The signals "D_C" and "D_Y" are fed through [7408] (6dB amplification) and via [7406], [7409] used as driver to the S-Video output connector. The "D_CVBS" line is directly routed to the modulator and via the circuit around [7431] and [7432] amplified by 6dB before it is fed to the CVBS output plug. In case of EPG the signals from the digital board are routed through the EPG board where the selection between digital board video or EPG OSD is taken.

The Y/U/V signals from the digital board are also passing [7408] for 6dB amplification and driving purpose.

To achieve optimal picture quality the set is equipped with a simple progressive scan function based on a so-called line doubler. The complete generation of the signal is done on the digital board and via a separate cable and connector [1946] the corresponding Y/U/V lines are routed to the analog PCB. Also the YUVprogressive signals are switchable to EPG OSD on the EPG board if implemented. As there is only one Y/U/V output available a switching between interlaced and progressive output is necessary. While the transistors [7421], [7422], [7424], [7425], [7427] and [7428] are used as driver for Y/U/V progressive, [7423], [7426] and [7429] together with [7405] are necessary for killing these signals via pin 42 of [7408] in case the interlaced is selected ("PSCAN_KILL"-line set to low). If progressive output is active the pins 27, 29 and 31 of [7408] are set to high impedance and "PSCAN_KILL" is also high (e.g. 5V).

The detection of the picture ratio information on the Y/C inputs (rear or front) is done by measuring the DC-level on the Chroma signal via an analog input of the CC-P ("WSRI"- and "WSFI"-line). In case the level is higher than 3,5V the input signal is a 16:9 source, if the level is lower than 2,4V the picture ratio is 4:3.

For generation of the appropriate DC-voltage on the Y/C output the "WSRO"-line is controlled via pin18 of [7408] by the CC-P (Pin 18 set to low means 4:3, pin 18 set to high determines 16:9).

During Stand-By there is also no loop-through of any input to any output performed.

9.5 Digital Board

9.5.1 Record Mode

Video Part

Analog Video input signals CVBS, YC and UV(RGB for EURO and YUV for USA) are routed via the analog board to connector 1601 and sent to IC7500 SAA7118 (Video Input Processor). Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1603 and further also to IC7500.

IC7500 (VIP) encodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7403 SAA6752H (EMPRESS) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.

IC7403 (EMPRESS) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio are sent from the analog board to IC7403 EMPRESS via connector 1602. The EMPRESS compresses I2S audio data into an AC3 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, EMPRESS IC7403, MPEG decoder IC7200 (Sti5508) and buffers the data streams that are coming from or going to these hardware modules. In IC7100 (VSM), the video MPEG2 stream and the audio AC3 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7200 (Sti5508). This IC decodes the MPEG stream into analog video and I2S audio. The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

9.5.2 Playback Mode

During playback, the serial data from the Basic Engine is going directly to the Sti5505 via the serial front-end I2S interface. The Sti5508 is a MPEG & Audio/video decoder and has the following outputs:

- To the analog board:
 - analog video RGB, YC, CVBS
 - I2S audio (PCM format)
 - SPDIF audio (digital audio output)
- To the Progressive scan board:
 - digital video YC(7:0).

9.5.3 S2B Interface

The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

9.5.4 System Clock

System clocks(27MHz) of VSM, Sti5508, EMPRESS and Progressive Scan are generated by oscillator 7906

9.5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7102 (PLL) because then, the audio clock must be synchronized with the incoming video (VIP_FID) from the VIP.

During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7900 (MK2703S). Both ACC_ACLK_OSC(also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock to the STI5508. The EMPRESS IC derives from the incoming ACLK_EMP the I2S audio encoder clocks AE_BCLK and AE_WCLK which are sent to the VSM.

9.5.6 On/Off

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

9.5.7 Reset

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

9.5.8 I2C Bus

Sti5508 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7201 NVRAM
- IC7403 EMPRESS
- IC7500 VIP
- IC7700 FLI2200 Video Deinterlacer Line Doubler
- IC7801 ADV7196 Video Denc

9.5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7301 and 7302: Flash memories which contain the application and diagnostic software
- IC7100: VSM
- IC7200: MPEG AV Decoder

Block Diagram Digital Board

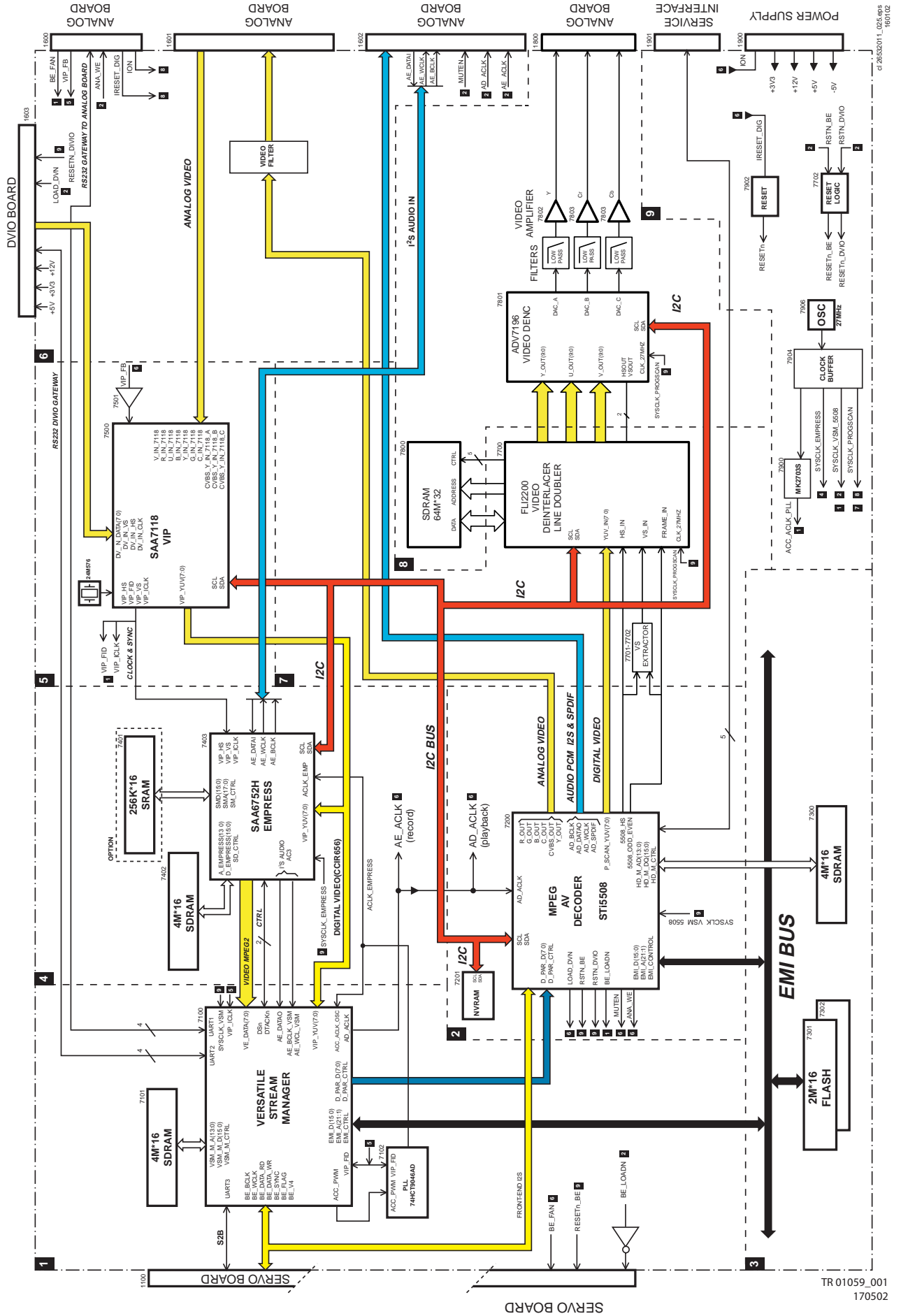


Figure 9-4

9.5.10 Progressive Scan

Description

The progressive scan part is integrated in the Digital Board and built around the SAGE Fli2200 de-interlacer / line doubler (7701). This I2C controlled de-interlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing). The de-interlacer gets his digital YUV input data from the STi5508 (7200). The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz. Because the STi5508 doesn't have a Vsync output the odd/even output of this IC has to be translated to a Vsync signal. Some glue logic has been added to extract the vertical sync. The glue logic circuit consists of Flip-Flop IC 74HC74D (7701) and EXOR 74LVC86 (7702). The next diagram shows how the vertical sync is extracted.

Vertical Sync

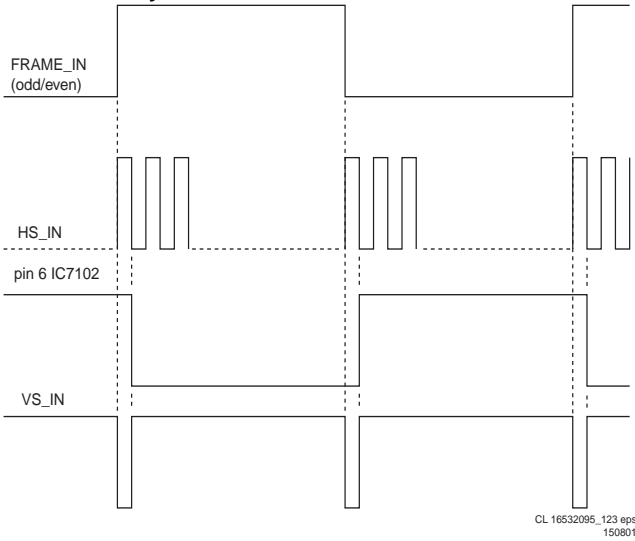


Figure 9-5

The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices ADV71967 MacroVision compliant DENC (7801). The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7802-7803). The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.

9.6 Divio 1.8 Board

9.6.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. Input is a stream from a DV-camcorder via IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present. The following picture shows the location of the DVIO Module inside the DVDR set.

Description DIVIO Module

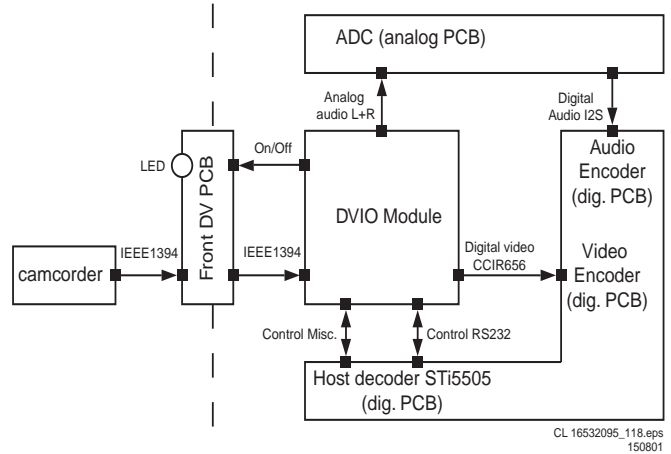
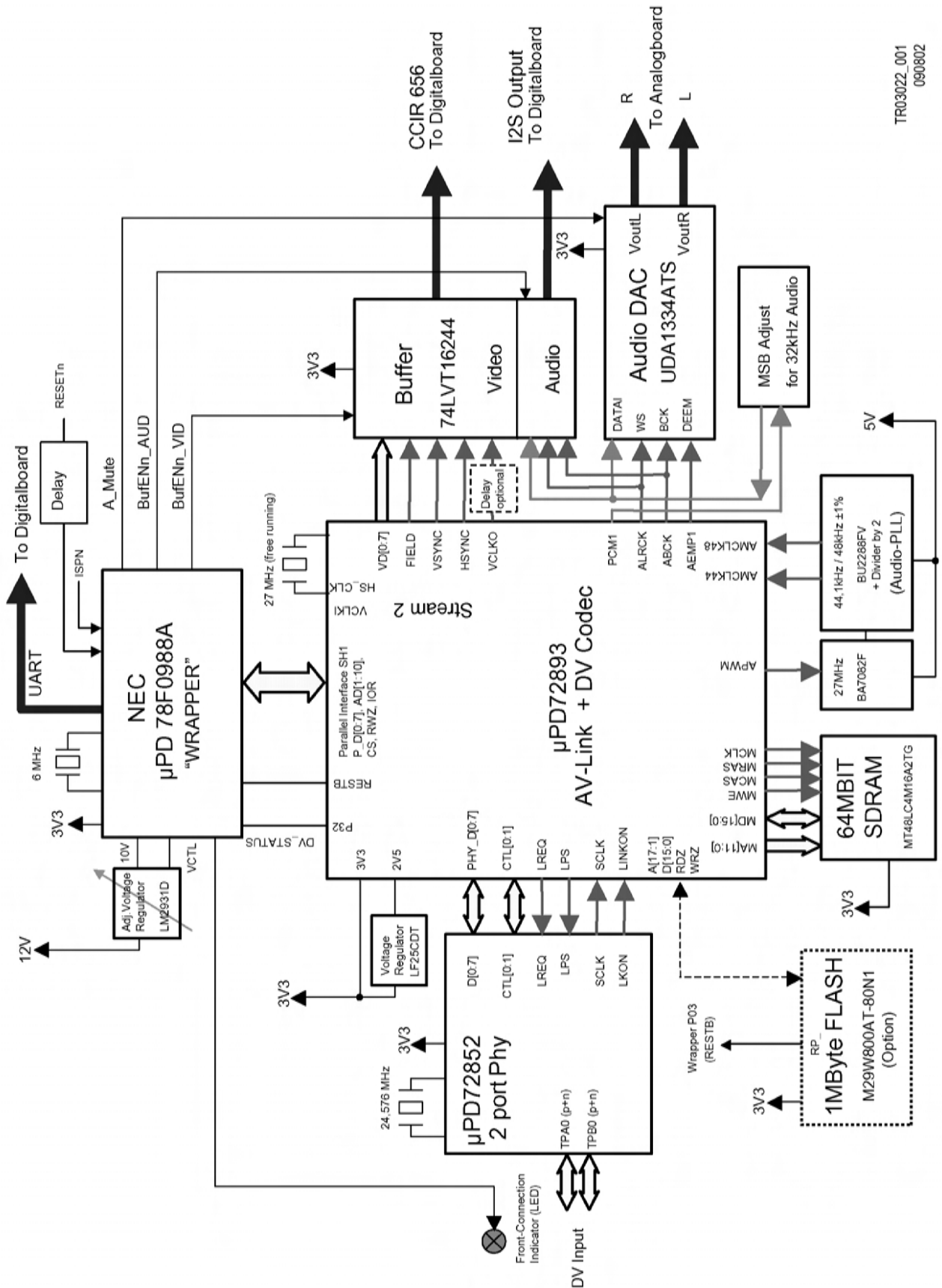


Figure 9-6

9.6.2 Block Diagram

Block Diagram DVIO1.8



TR03022_001
090802

Figure 9-7

9.6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
 - uPD72852 (7400) (Phy)
 - uPD72893 (7431) (Link part)
2. Micro-controller
 - uPD78F0988 (7802)
 - Voltage regulator LM2931 for generation of 10V programming voltage (7801)
3. Reset-circuitry
 - Power-on reset
 - Reset pulse-shortener
4. DV-Decoder
 - uPD72893 (7431) (Codec part)
 - 16MBit SDRAM (7430)
 - optional Flash-Memory M29W800AT for Firmware-Update of uPD72893 (7432)
5. Clocking & Audio PLL
 - Clock oscillator FXO-31FT (7601)
 - Audio-PLL: Voltage controlled oscillator BA7082F (7604), clock generator BU2288FV (7605), and clock divider 74LV74 (7606-A)
6. Audio Format adaption (MSB justified -> I2S), option
 - 74LV74 (7507-A, -B)
7. Audio & Video output
 - Audio DAC UDA1334ATS(7602)
 - Clock delay(7500)
 - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a uPD72852 physical layer and a uPD72893 link layer IC (uPD72893 integrated also DV-Decoder).

It has the following features:

- S400 operation (400 megabit per second)
- Two i.Link ports (4 pin), only one used
- AV link port

Micro-Controller

The uPD78F0988 processor has following extra features:

- 60 kilobyte of flash memory as program memory
- 2 kilobyte of internal data memory
- watchdog timer
- On board ISP(In-System-Programming) functionality

ISP

By use of In-System-Programming, it is possible to update the software of the DVIO board that is in the uPD78F0988. ISP can be made active by resetting the processor and keeping the ISPn pin low during reset. During ISP, the ISPn signal on the board has to be kept low. A programming voltage of 10V is activated by the uPD78F0988 itself at the Vpp pin before programming procedure starts. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Reset-circuitry

The reset-circuitry consists of two parts.

First part (around transistor 7803) generates a reset pulse when the board is powered up.

Second part (around transistors 7804 & 7805) acts as a reset-pulse shortener, i.e. a short reset pulse (4ms) is generated from the input signal RESETn which is much longer (usually 100ms). This is required to ensure correct operation of the Micro-controller after booting-up when RESETn is again deactivated

DV-Decoder

The uPD72893 decodes the stream into video data in 656 format and audio data in I2S format.

The microprocessor has the ability to read the status registers of the uPD72893. By reading these registers, extra data from

the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Clocking and Audio PLL

The FXO-31FT generates the free-running 27MHz system clock. Video part of input DV-stream is in the uPD72893 adapted to the local 27MHz clock domain (skip, repeat frame). Because audio clock (11.2896Mz [fs=44.1kHz] or 12.288MHz [fs=32kHz, 48kHz]).

The uPD72893 integrates the phase comparator that drives the VCO BA7082F to a nominal frequency of 27MHz which in turn is converted by BU2288FV and 74LV74 to 11.2896MHz or 12.288Mhz, respectively.

The uPD72893 controls directly the frequency ratio of the BU2288FV.

Audio Format adaptation (MSB justified -> I2S), option

Due to a bug in 1st version of uPD72893 digital audio output is not correct in I2S mode when in 32kHz operation. As a workaround uPD72893 is generally configured in MSB justified mode and conversion to I2S mode is done externally via a 74LV74 device.

Can be disabled with later versions of uPD72893.

Audio & Video Output

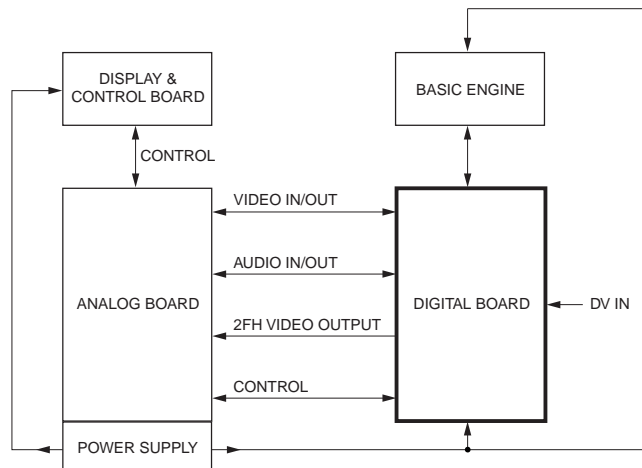
The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board. The tri-state buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.

The clock delay synchronizes the AV clock with the AV data at the output.

9.7 Digital Board Chrysalis 2.1

9.7.1 Introduction

Block diagram 2nd generation DVD recorder



CL 36632004 001 eps
14/02/03

Figure 9-8

This 2nd generation Digital Board is based on the highly integrated 'Chrysalis' IC. Its predecessors, the 'Empire' and 'Empress' based boards, had two PWBs mounted on top of each other (due to separate DVIO board). For this new generation, all functionality is now available on one PWB in one BGA IC (Ball Grid Array) i.s.o. four VLSI ICs.

The board encodes and multiplexes analogue video and digital uncompressed audio (I2S) into an MPEG2 stream. This MPEG2 stream is formatted, to be recorded by the DVD+RW engine. In playback, the board will decode the MPEG2 stream into analogue and digital audio and into analogue video. In addition, a DV stream can be received via IEEE1394 (i-Link), and transformed to MPEG2 format.

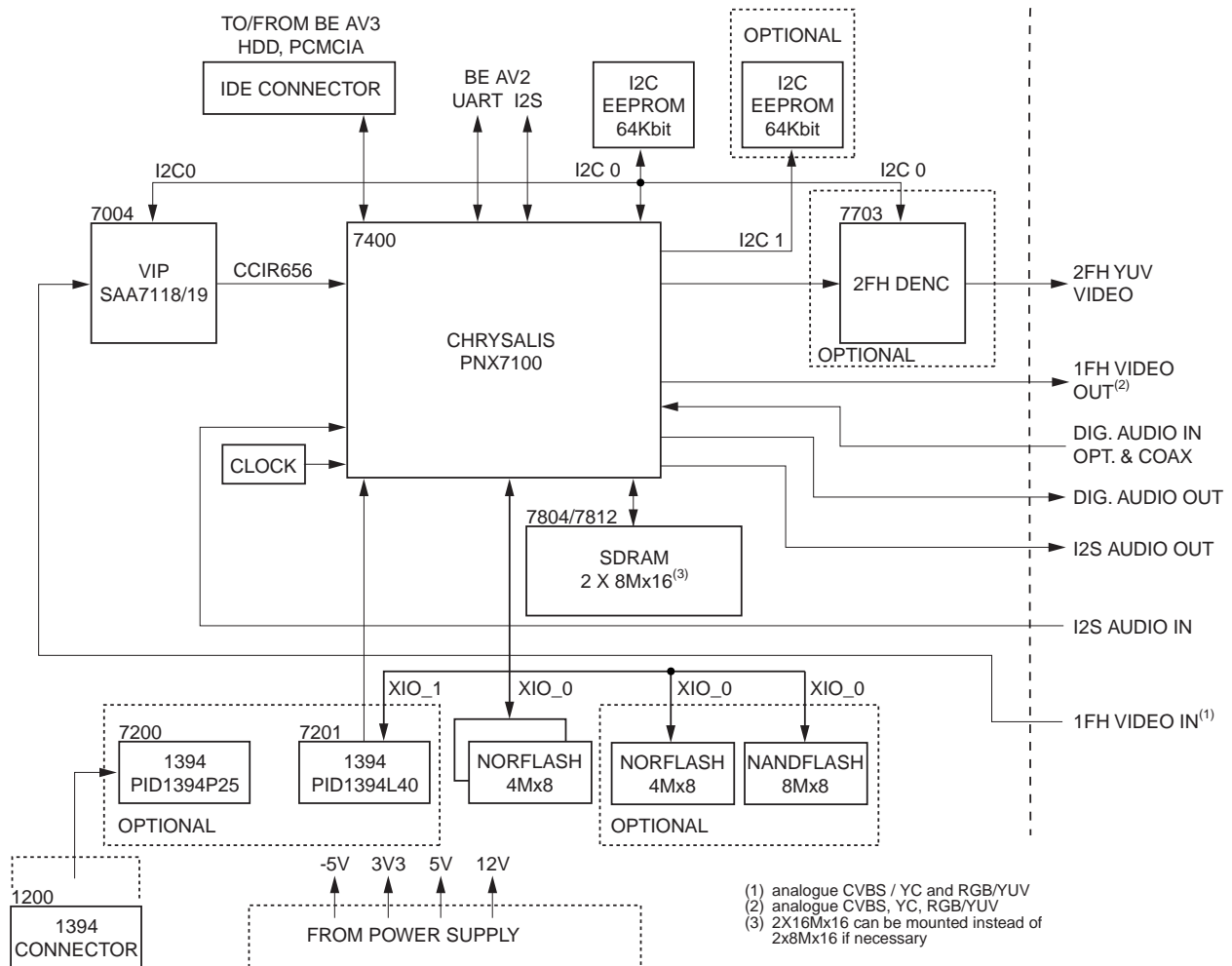
There are versions foreseen, to generate a progressive scan analogue video output. In the standard Chrysalis board, the

progressive video output is generated by the PNX7100. In the Chrysalis 'F' it is generated by the Faroudja FLi2301.

The Chrysalis Digital board is pin compatible with the Empress digital board in terms of A/V IO, BE interface, Power Supply, and Service interface. For functional enhancements, several connectors are added: IDE connector (HDD, AV3, PCMCIA, etc.).

9.7.2 Record Mode

Block diagram Chrysalis Digital Board



CL 36532004_003.eps
140203

Figure 9-9

Video Part

The analogue video input signals CVBS, YC, and YUV/RGB (RGB for EURO and YUV for USA), are routed via the analogue board to connector 1904 and sent to IC7004 (SAA7118, Video Input Processor).

The digital video input signals are routed from the DV-In connector (item 1200) via ICs 7200 (1394 PHY) and 7201 (1394 LINK) to IC7400 (PNX7100, Chrysalis).

The multistandard Video Input Processor (VIP, IC7400) encodes the analogue video to digital video stream (CCIR656 format). It provides filtering of the analogue signals and separation of luminance and chrominance by a comb filter. The output stream, named ITU_IN(7:0), is then routed to the Chrysalis IC (PNX7100). This IC encodes and decodes the digital video stream into/from MPEG2 format.

Audio Part

I2S audio is sent from the analog board to the Chrysalis IC via connector 1900. The Chrysalis compresses the I2S audio data into an MPEG1-L2/AC3 audio stream.

Front-end I2S

IC7400 (Chrysalis) interfaces directly to the Basic Engine (BE) via connectors 1100 (clock and data) and 1105 (control). For future use (with AV3 BE module, HDD, or card reader) it also interfaces to an IDE bus via connector 1102.

It buffers the data streams that are coming from (or going to) these hardware modules.

In the Chrysalis, the video MPEG2 stream and the audio AC3 stream are multiplexed into an I2S stream. The serial data are sent to the Basic Engine for recording.

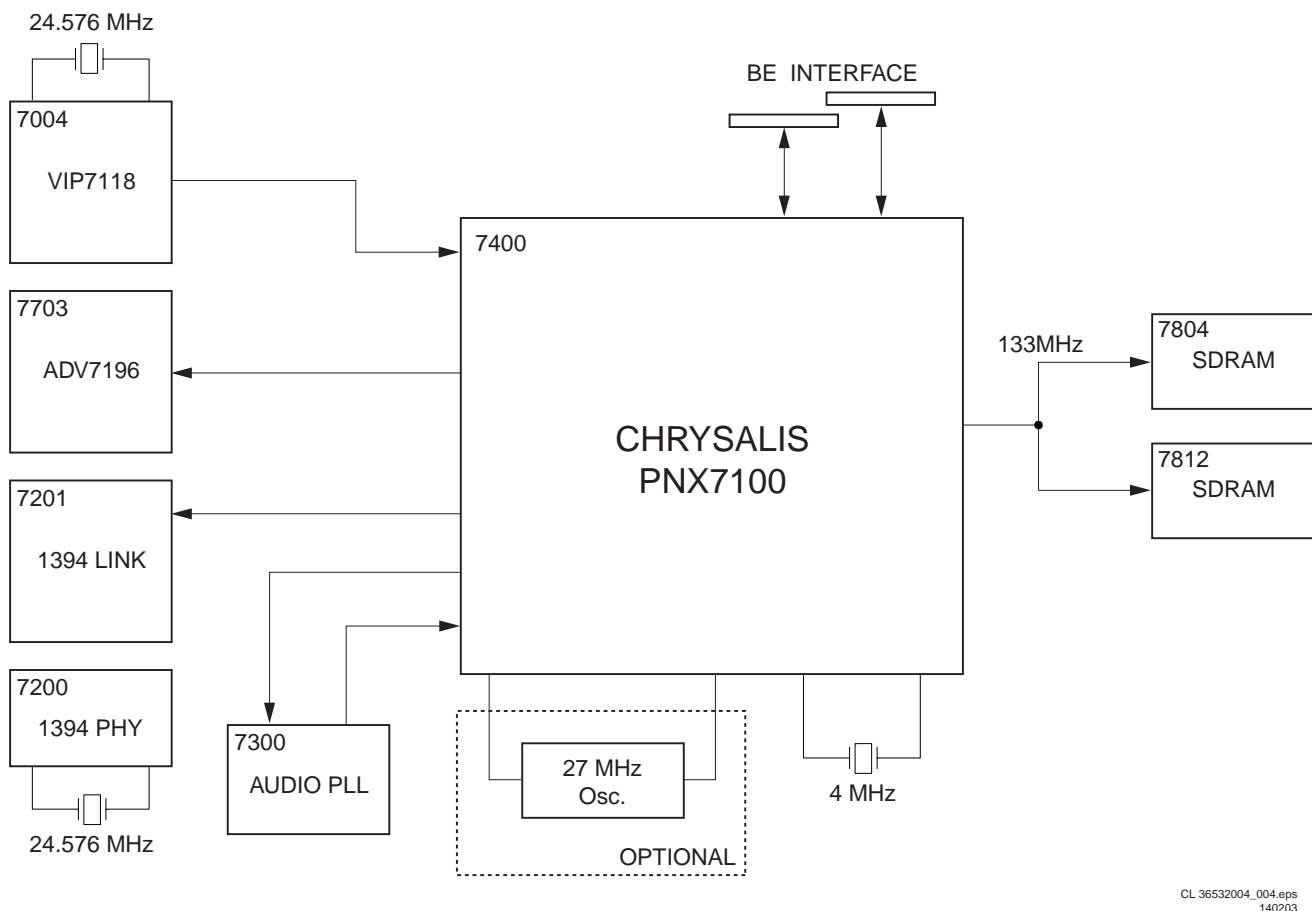
9.7.3 Playback Mode

During playback, the serial data from the Basic Engine is going directly to the PNX7100 via the serial front-end I2S interface. The PNX7100 is an MPEG CoDec and has the following outputs:

- To the analogue board: analogue video RGB, YC, CVBS on connector 1904.
- I2S audio (PCM format) on connector 1900.
- SPDIF audio (digital audio output) on connector 1904.
- Progressive video on connector 1704.
- Communication gateway (RS232) on connector 1104.

9.7.5 Clock Distribution

Clock distribution on Chrysalis board



CL 36532004_004.eps
140203

Figure 9-10

The PNX7100 has a complex clock system, which is needed to support the processes running at different frequencies such as video decoding, audio decoding or peripheral I/O devices etc. To ensure a synchronous initialisation of all the registers and state machines, all the PLLs are switched to their default frequency and the reset sequence is run at 4 MHz. Then when the booting control unit is correctly initialized and once it has captured all the booting parameters, it sets the PLLs to its functional frequency to allow the modules to run at their nominal frequencies. Thanks to a clock blocking mechanism, the frequency switching is glitch free.

9.7.4 Basic Engine Interfaces

AV2 Basic Engine (VAE8015 and VAE8020)

The UART interface (for the S2B commands) between the Chrysalis and the servo processor (MACE3 on the BE module), controls the AV2 Basic Engine during record and playback mode. For data transport, an I2S bus is used. For detailed information on the AV2 BE module, see Service Manual 3122 785 12470.

AV3 Basic Engine (VAE8030)

To be prepared for new developments, the Chrysalis Digital Board is equipped with two IDE busses (ATAPI). They can be used for connecting to the new generation Basic Engine (e.g. the AV3), a Hard Disc Drive (HDD), or a Smart Card Reader.

System clocks:

- PNX7100 (IC7400, pins AF9 and AF10) : 4 MHz provided by the xtal oscillator 7402.
- SAA7118 (IC7004, pins A3 and B4): 24.576 MHz provided by xtal 1001.
- ADV7196 (IC7703, pin 25): 27 MHz provided by PNX7100.
- SDRAM (IC7804 and 7808, pin 38): 133 MHz provided by the PNX7100.
- 1394-LINK (IC7201, pin 88): 49.152 MHz provided by 1394-PHY.
- 1394-PHY (IC7200, pins 59 and 60): 24.576 MHz provided by xtal 1201.

9.7.6 Power Supply

The Digital Board is not powered in standby mode. The control signal 'ION' (Inverse On), coming from the analogue board, will enable the PSU, and power the digital board.

- ION = High: the digital board is in powered down standby mode.
- ION = Low: the power supply to the digital board is enabled.

The 3V3, +5V, -5V, and +12V come from the PSU, while the 1V8 core voltage is generated on the board by a low voltage buck controller (item 7501). It provides the control for a DC-DC power solution producing an 1.8V output voltage over a wide current range. The NCP1570-based solution is powered from

9.7.8 Reset

Reset concept Chrysalis board

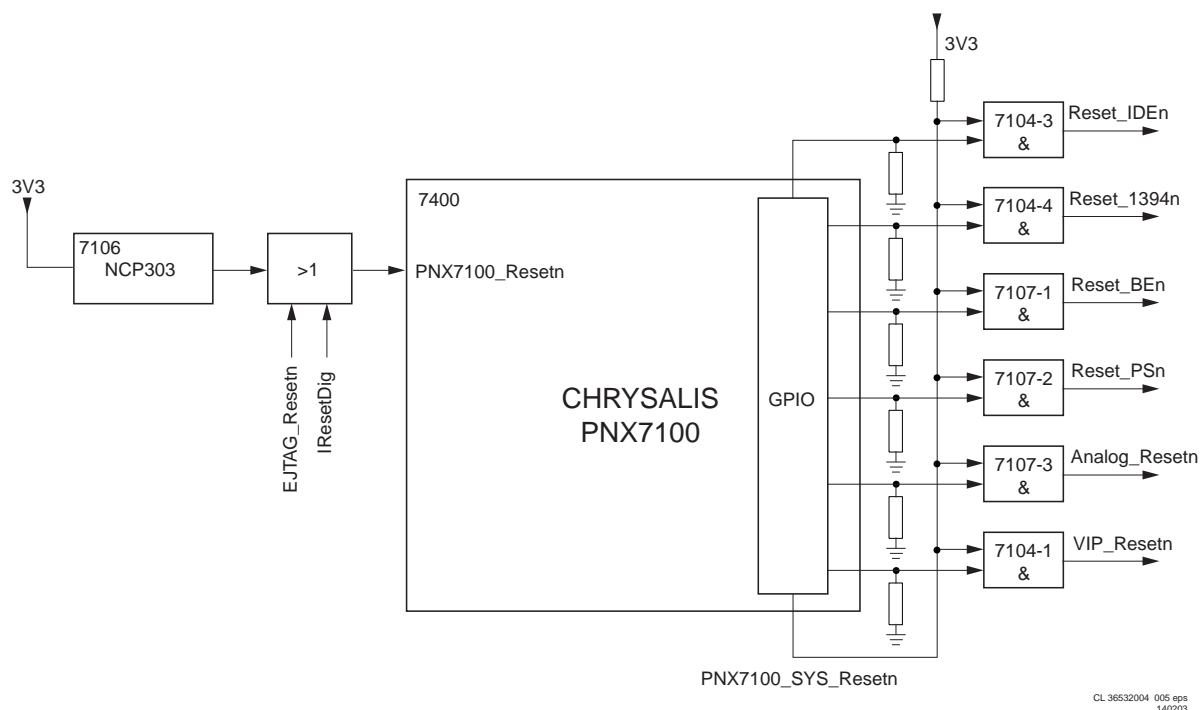


Figure 9-11

The voltage detector NCP303LSN29 (IC7600) provides the reset signal PNX7100_RESETh (active 'low') with the correct timing behavior. This circuitry functions as a Power-On Reset (POR) module, which detects the minimum functional voltage that is needed by the device. It also detects any voltage drop. When the power voltage is outside the nominal range, a reset signal is generated by the POR module and fed to the reset module which controls the individual reset of the different peripherals and processing units.

There are two control lines which can overrule this reset signal:

- IRESET_DIG (controlled by the microprocessor on the Analogue Board).
- EJTAG_RESETh (only for production).

They can pull the output of the NCP303LSN29 (item 7106) down via a shottky diode.

So when the output signal PNX7100_RESETh is 'low', the board will reset. When this signal is 'high', the board is up and running.

The PNX7100_SYS_RESETh is a general enabling signal for the different reset lines. All other reset lines are directly driven from Chrysalis port pins (e.g. MPIO13_IDE1_RESETh). All

12 V with the output derived from the 3V3 supply. It contains all required circuitry for a synchronous NFET (IC7500-1 and -2) buck regulator.

9.7.7 Memory

Several memories are used on the Chrysalis Digital Board:

- EEPROM IC7810: this memory contains all the necessary boot parameters of the board.
- EEPROM IC7809: this memory contains all the necessary parameters for the application.
- FLASH IC7807(05/11): this memory contains the application-, diagnosis-, and service software.

reset lines are logically connected via 74LVC08D (item 7104) and (item 7107) AND-gates. If both reset signals are low, all other external devices are initialised.

9.7.9 I2C Bus

The PNX7100 is the master of the I2C bus (during reset, external I2C masters are allowed). The following ICs are controlled by the I2C bus:

- IC7809.
- IC7810 NVRAMs.
- IC7004 VIP.
- IC7700 FLI2301 Video De-interlacer Line Doubler (for Chrysalis-F boards).
- IC7703 ADV7196 Video Enc (for progressive scan done by Chrysalis).

9.7.10 I/O Connectors

AIO Connector (item 1900)

The Audio In/Out (AIO) connector is used to interchange digital audio signals between Analog- and Digital Board.

DAIO Connector (item 1901)

The Digital Audio In/Out (DAIO) connector is used to interchange digital audio (SPDIF) signals between the IOE-Board and the Digital Board.

VIO Connector (item 1904)

The Video In/Out (VIO) connector is used to interchange analogue video signals between Analog- and Digital-Board.

9.7.11 Progressive Scan

Introduction

There are two versions foreseen, to generate a progressive scan analogue video output:

- In the standard Chrysalis board, the 'low end' progressive video output is generated by the PNX7100.
- In the Chrysalis 'F', the 'high end' progressive output is generated by the Faroudja FLI2301. This IC offers additionally DCDi, upscaling to HDTV, and picture enhancement.

Description

The progressive scan part is integrated in the Digital Board and built around the FLI2301 de-interlace/line doubler (7701). This I2C controlled de-interlace uses a 64Mbit SDRAM (32bit x 2M) to perform high quality de-interlacing (meshing). The de-interlace gets its digital YUV input data from the PNX7100 (7400). The format of the digital YUV input to the FLI2301 is CCIR656 with separated Hsync, Vsync, and odd/even signal running on 27MHz.

9.8 Service UART Interface

Logic IC 74HCT14D (item 7111) is used to make a level conversion from microprocessor (LVTTL) to +/-5V (compatible with most RS232 interfaces) and vice versa. The control line MPIO19_CTL_SERVICE is used to activate service and diagnostic SW at start up procedure. The connectivity is provided via an external service tool.

9.9 EPG Nafta Board

9.9.1 General

Two ASICs from Gemstar, GS501 (item 7100) and GS502 (item 7201), generate the EPG OSD. The host P controls both ICs via the I2C bus (pins 45 and 48). A RAM memory (item 7102) and a Flash memory with the firmware (item 7101) belong also to the periphery of these ASICs. A PIC processor (item 7303) generates the POR_N reset for this system. The POR_DC reset comes from the set, and is active after AC power 'on'. A port expander from the host, controls the EXT_RESET signal. This port expander (item 7200) is also used for switching the video paths on the EPG board.

Either the board works in 'Loop Trough' mode, or (for EPG) the output path is switched to the 'EPG RGB' video.

Blockdiagramm EPG-Modul Nafta

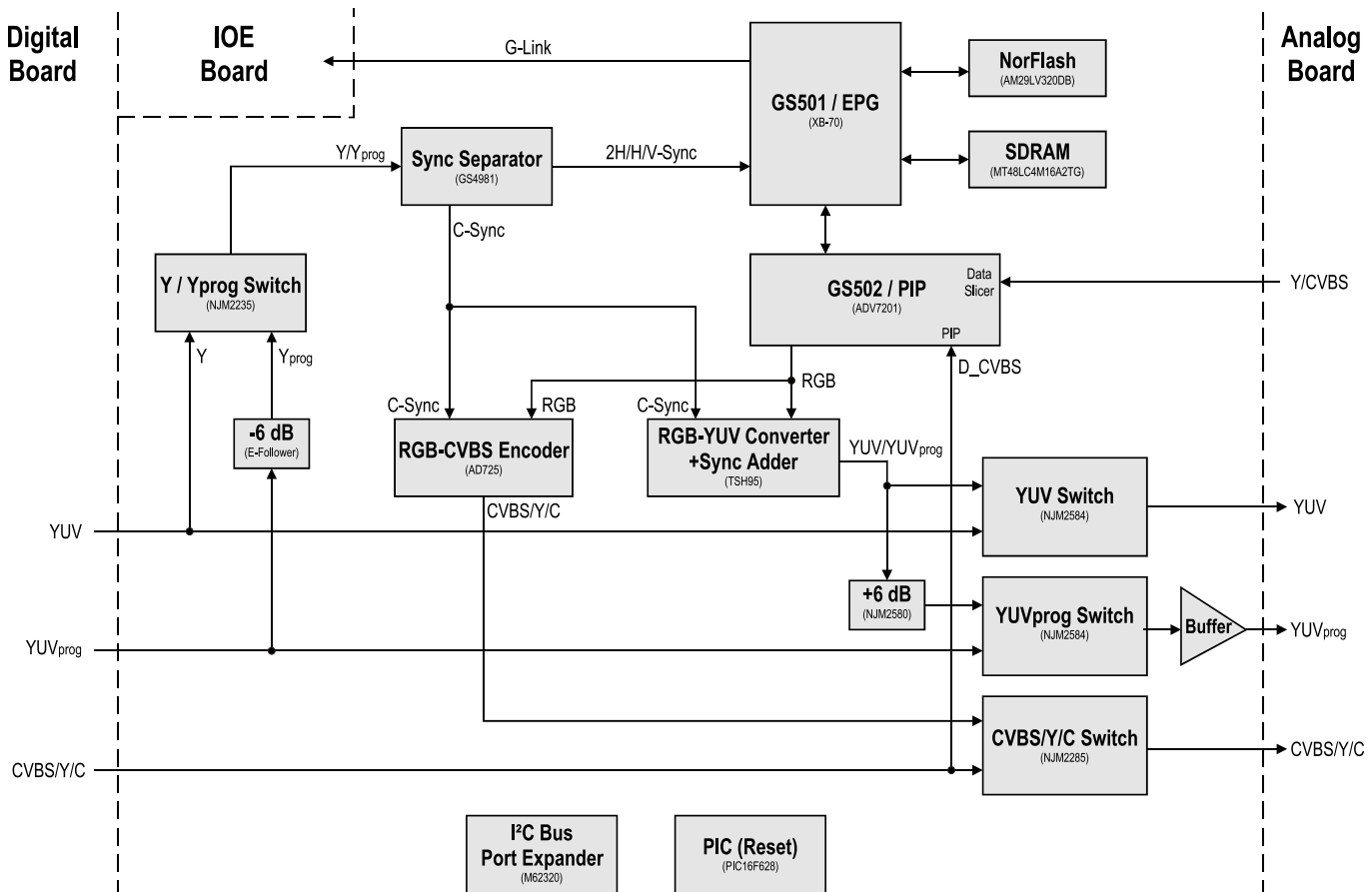


Figure 9-12

9.9.2 Loop trough

For 'Loop Trough' the input video signals (CVBS, YC, YUV, and YUV-progressive) from the Digital board are passing three video switches before going to the Analog board.

- Item 7503 for CVBS and Y/C.
- Item 7502 for YUV-interlaced.
- Item 7501 for YUV-progressive.

9.9.3 EPG RGB Video

A V-sync and H-sync (for progressive = 2H-sync) are necessary for outputting an RGB video. A sync separator (item 7703) generates these syncs. Input for the sync separator is either the 1fh or the 2fh luminance signal from the Digital board. A video switch (item 7700) makes the selection. For progressive video, the signal must be attenuated (item 7701).

The RGB signal goes via emitter followers (items 7202, 7203, and 7204) to an RGB-to-YUV converter and to an RGB-to-CVBS, Y/C converter.

The RGB-to-YUV converter consists of four OpAmp's, which are necessary for RGB/YUV conversion (item 7600-B, -C, and -D) and for adding the C-sync to the Y signal (item 7600-A). The RGB-to-CVBS, Y/C conversion is realized by IC7602. The oscillator (item 7601) is necessary for generating the chroma carrier.

With transistor 7603 the conversion stages can be switched 'off' for power saving.

For the PIP (Picture in Picture) feature, the D_CVBS video signal from the Digital board is used. This signal is fed to Pin 10 of IC7201. For scanning the EPG data, the A_YCVBS signal from the Analogue board is fed to pin 8 of IC7201.

9.9.4 Power supply

The supply for the video stages and the EPG digital part, are generated via DC-DC converters (items 7400, 7401, and 7403) out of the 12STBY.

9.10 EPG Europe Board

9.10.1 General

The ARM7 based microprocessor (item U1) and an ASIC (Gemstar GSA03, item U2) generates the EPG OSD data (RGB or YUV-interl./progr.). The host P on the Digital board, controls both ICs via the I2C bus. A RAM memory (item U7)

and two Flash memories (items U8 and U9) with the firmware and EPG data, belong also to the periphery of the ASIC. A resistor and capacitor (items R1 and C6) generate the reset for this system. The IPOR reset comes from the set and is active after main power 'on'. A port expander from the host, controls the nGCLR reset signal. This port expander (item U31) is also used for switching the video paths on the EPG board.

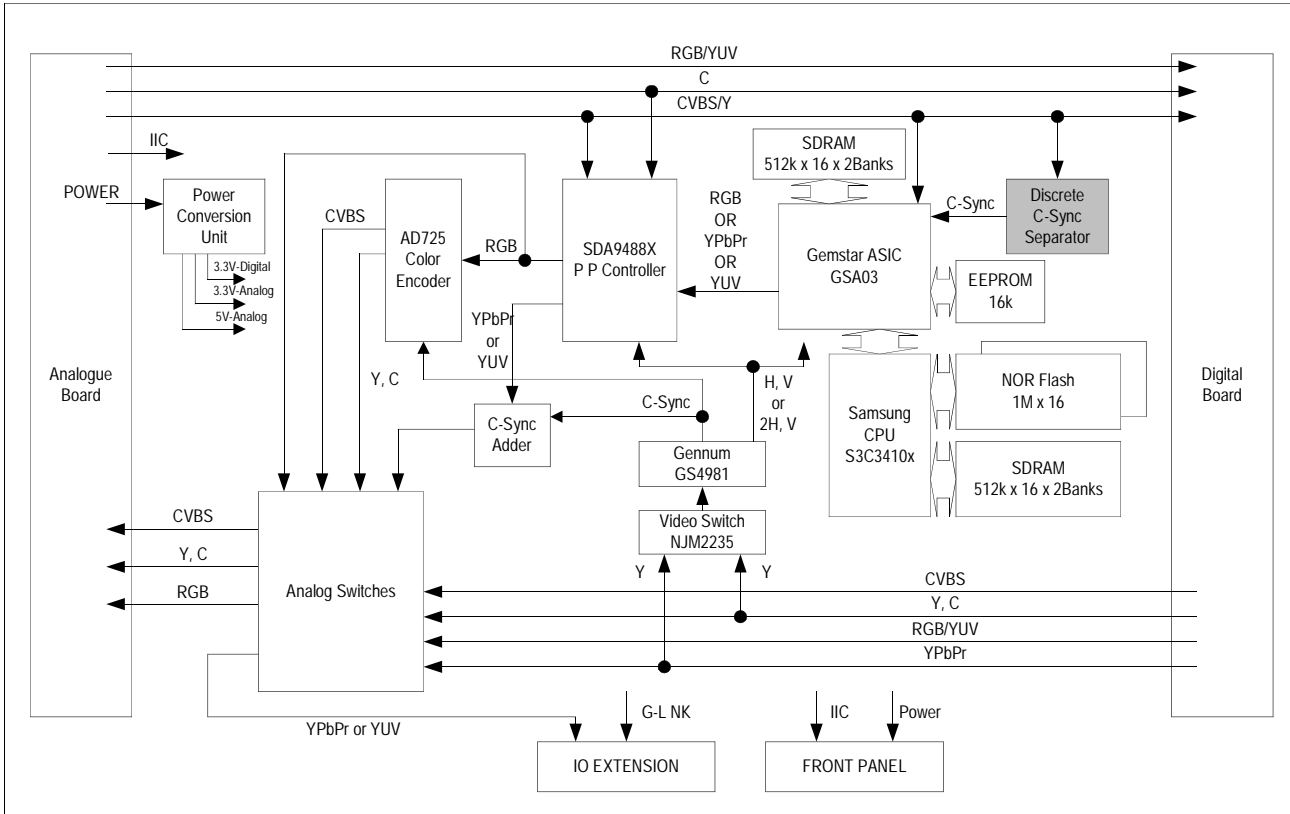


Figure 9-13

Either the board works in 'Loop Trough' mode, or (for EPG) the output path is switched to the 'EPG RGB' video.

9.10.2 Loop Trough

For 'Loop Trough', the input video signals (CVBS, YC, RGB, YUV-interlaced, and YUV-progressive) from the digital board are passing three video switches before going to the Analogue board.

- Item U15 for CVBS and Y/C selection between EPG and Loop trough.
- Items U16, U18, and U19 (and periphery) for RGB selection between EPG and Loop trough.
- Items U42 and U17 for YUV-interlaced and YUV-progressive selection between EPG and Loop trough. These signals are amplified (items U13B, C, and D) for driving a 75-Ohm output.

Note: RGB and YUV-interlaced (VR_DVD, UB_DVD, YG_DVD) are the same signals. It depends on the software, which signal is chosen.

9.10.3 EPG RGB

A V-sync and H-sync (for progressive = 2H-sync) are necessary for outputting an EPG video. A sync separator (item U10) generates these syncs. Input for the sync separator is either the 1fh or the 2fh luminance signal from the Digital board. A video switch (item U50) makes the selection.

The EPG signal goes via a PIP-inserter IC (item U11 and peripherals) that inserts a PIP (Picture In Picture) into the EPG OSD. Source for this PIP is the CVBS signal from the digital board.

When the PIP output is a YUV signal, the Y signal is without a sync. Therefore, this sync must be added with item U13A.

For RGB-to-CVBS, Y/C conversion is realized by a PAL conversion IC (item U14). The oscillator (item Y5) is necessary for generating the chroma carrier.

For scanning EPG data, the A_YCVBS signal from the Analog board is used. This signal is fed to pin 189 of item U2. There is also a sync from the Analog board necessary. A discrete circuit (items Q18-Q23 and periphery) generates it.

9.10.4 Power supply

The supply for the video stages and the EPG digital part are generated via DC-DC converters and linear regulators (items U28, U40, and U41) out of the 12VSTBY.

9.11 I/O Extension Board

This board feeds the internal S/PDIF signal from the Digital board to an optical and/or digital out connector. For European players, also an YUV output is present on this board.

9.12 IC Descriptions

9.12.1 Display Board

IC 7103 TMP87CH74F Display Board, Front Microprocessor

Block Diagram

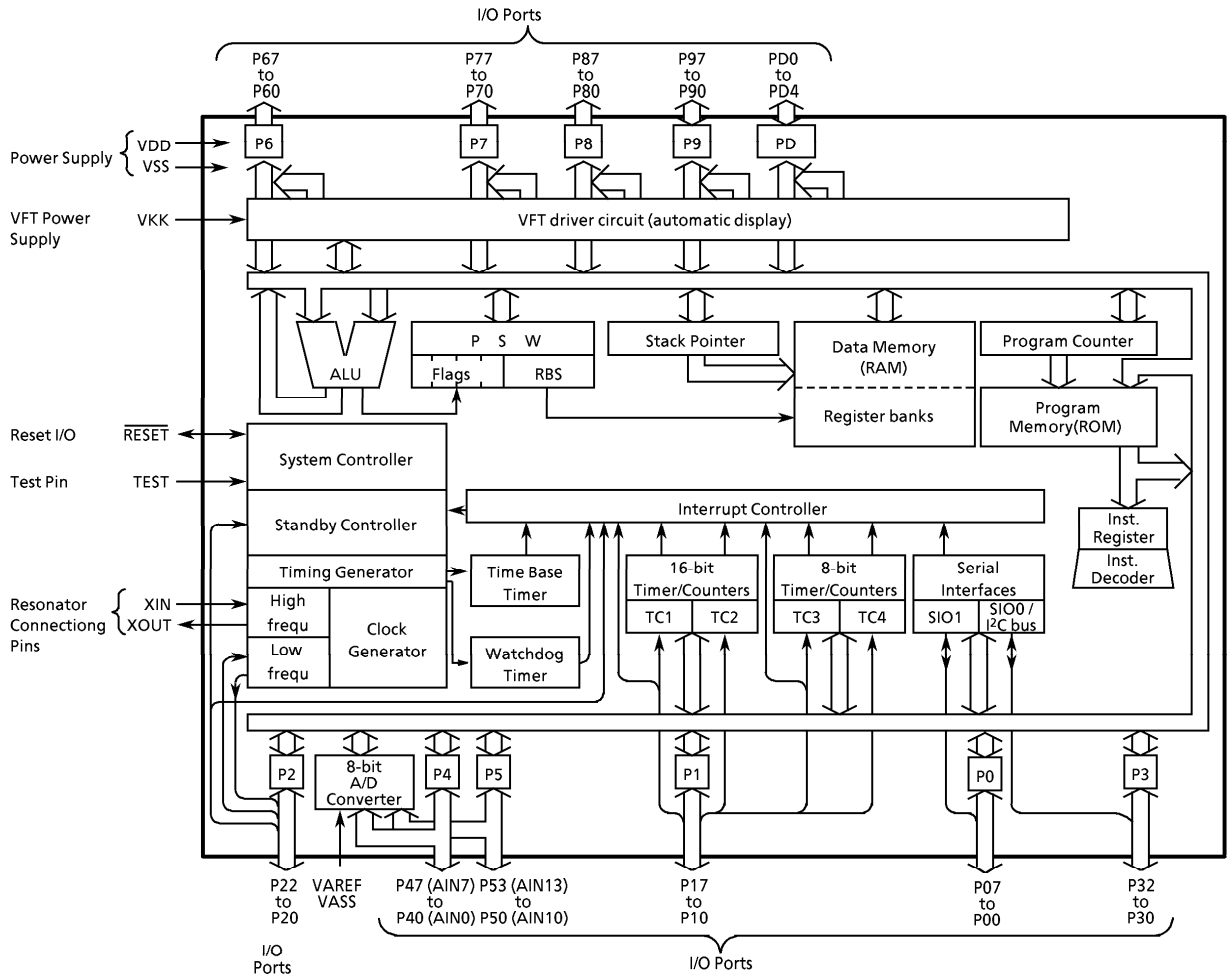


Figure 9-14

Pin Function

Pin Name	Input / Output	Function	
P07 to P03	I/O	Two 8-bit programmable input/output ports (tri-state).	
P02 (SO1)	I/O (Output)	Each bit of these ports can be individually configured as an input or an output under software control. When used as a SIO input/output, an External interrupt input, a timer/counter input, the latch must be set to "0". When used as a PPG output or divider output, the latch must be set to "1".	SIO1 serial data Output
P01 (SI1)	I/O (Input)		SIO1 serial data Input
P00 (SCK1)	I/O (I/O)		SIO1 serial clock input/output
P17 (INT4/TC3)	I/O (Input)		External interrupt input 4 or Timer/Counter 3 input
P16 (INT2)			External interrupt input 2
P15 (INT3/TC1)			External interrupt input 3 or Timer/Counter 1 input
P14 (TC4/PDO/PWM)			Timer counter 4 input or 8-bit programmable divider output or 8-bit PWM output
P13 (DVO)			Divider output
P12 (TC2/PPG)			Timer counter 2 input or Programmable pulse generator output
P11 (INT1)			External interrupt input 1
P10 (INT0)		External interrupt input 0	
P22 (XTOUT)		I/O (Output)	3-bit input/output port with latch. When used as input port, or external interrupt input, STOP mode release signal input, the latch must be set to "1".
P21 (XTIN)	I/O (Input)	External interrupt input 5 or STOP mode release signal input	
P20 (INT5/STOP)	I/O (Input)		
P32 (SCK0)	I/O (I/O)	3-bit programmable input/output ports (Sink open drain).	SIO0 serial clock input/output
P31 (SDA/SO0)	I/O (I/O/Output)	Each bit of these ports can be individually configured as an input or an output under software control. When used as a I ² C input/output, the latch must be set to "1".	I ² Cbus serial data input/output or SIO0 serial data output
P30 (SCL/SI0)	I/O (I/O/Input)		I ² Cbus serial clock input/output or SIO0 serial data Input
P47 (AIN7) to P40 (AIN0)	I/O (Input)	8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as an analog input, the P4CR must be set to "0".	A/D converter analog inputs
P53 (AIN13) to P50 (AIN10)	I/O (Input)	4-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. When used as an analog input, the P5CR must be set to "0".	A/D converter analog inputs
P67 (V7) to P60 (V0)	I/O (Output)	Four 8-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	VFT driver outputs
P77 (V15) to P70 (V8)			
P87 (V23) to P80 (V16)			
P97 (V31) to P90 (V24)			
PD4 (V36) to PD0 (V32)	I/O (Output)	5-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	

Figure 9-15

Pin Name	Input / Output	Function
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.
RESET	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset outputted.
TEST	Input	Test pin for out-going test. Be tied to low.
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)
VKK		VFT driver power supply
VAREF, VASS		Analog reference voltage inputs (High, Low)

Figure 9-16

9.12.2IC's Analog Board

IC7408: STV6618 Analog Board, Video Switch Matrix

1.2 Pin Description

Pin No.	Symbol	Description
1	Y/CVBSIN_TUN	Y/CVBS Input from Tuner
2	DIGOUT3	Digital Output Pin 3
3	GND1	Ground Supply 1 for Video Inputs
4	CVBSIN_ENC	CVBS Input from Encoder
5	DECV	Video decoupling capacitor
6	CIN_ENC	Chroma Input from Encoder
7	YIN_ENC	Y Input from Encoder
8	V _{CC}	+5 V Power Supply for Video Inputs
9	R/PR/CIN_ENC	Red or Pr or Chroma Input from Encoder
10	G/YIN_ENC	Green or Y Input from Encoder
11	B/PBIN_ENC	Blue or Pb Input from Encoder
12	GND2	Ground Supply 2 for Video Inputs
13	B/PBIN_AUX	Blue or Pb Input from Auxiliary (SCART2 or external Cinch)
14	DIGOUT4	Digital Output Pin 4
15	G/YIN_AUX	Green or Y Input from Auxiliary (SCART2 or external Cinch)
16	DIGOUT5	Digital Output Pin 5
17	R/PR/CIN_AUX	Red or Pr or Chroma input from Auxiliary (SCART2 or external Cinch)
18	DIGOUT6	Digital Output Pin 6
19	Y/CVBSIN_AUX	Y/CVBS Input from Auxiliary (SCART2 or external Cinch)
20	VCCB_REC	Video Output Recorder Buffer Supply Pin
21	Y/CVBSOUT_REC	Y/CVBS Output to Recorder
22	GNDB_REC	Ground Supply for Recorder Buffer
23	COUT_AUX	Chroma Output to Auxiliary (SCART2 or external Cinch)
24	VCCB1	Video Output Buffer Supply Pin
25	Y/CVBSOUT_AUX	Y/CVBS Output to Auxiliary (SCART2 or external Cinch)
26	GNDB	Ground Supply for Video Buffer
27	B/PBOUT_TV	Blue or Pb Output to TV (SCART1 or external Cinch)
28	C_GATE	External Transistor Command for Bidirectinnal B/C SCART I/O
29	G/YOUT_TV	Green or Y Output to TV (SCART1 or external Cinch)
30	VCCB2	Video Buffer
31	R/PR/COUT_TV	Red or Pr or Chroma Output to TV (SCART1 or external Cinch)
32	VCCB3	Video Output Buffer Supply Pin
33	Y/CVBSOUT_TV	Y/CVBS Output to TV (SCART1 or external Cinch)
34	FBOUT_TV	Fast Blanking Output to TV (SCART1)
35	FBIN_AUX	Fast Blanking Input from Auxiliary (SCART2)

Pin No.	Symbol	Description
36	VDD	+5 V Digital Power Supply
37	SCL	I ² C Bus Clock
38	SDA	I ² C Bus Data
39	GNDD	Digital Ground Supply
40	CIN_TV	Chroma Input from TV (SCART1 or external Cinch)
41	Y/CVBSIN_TV	Y/CVBS Input from TV (SCART1 or external Cinch)
42	DIGOUT1	Digital Output Pin 1
43	CIN_TUN	Chroma Input from Tuner
44	DIGOUT2	Digital Output Pin 2

Figure 2: STV6618 Input/Output Diagram

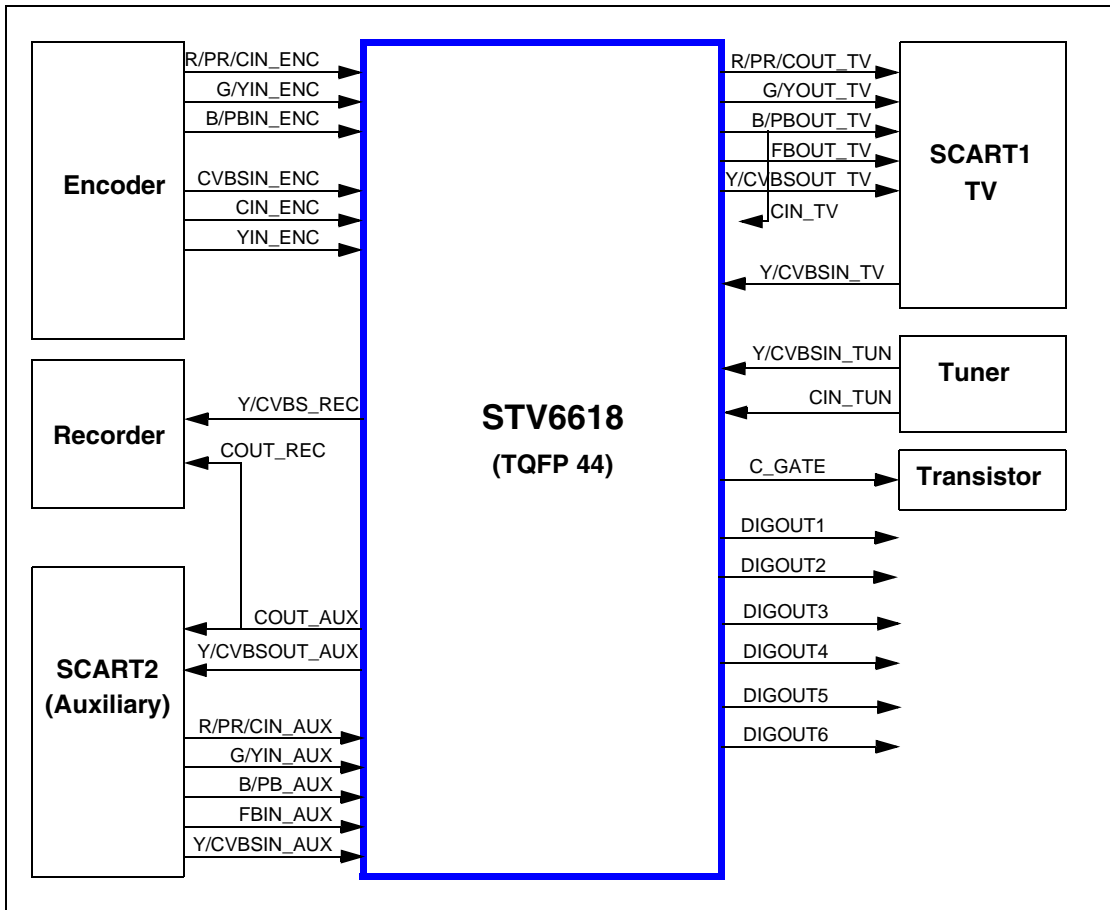
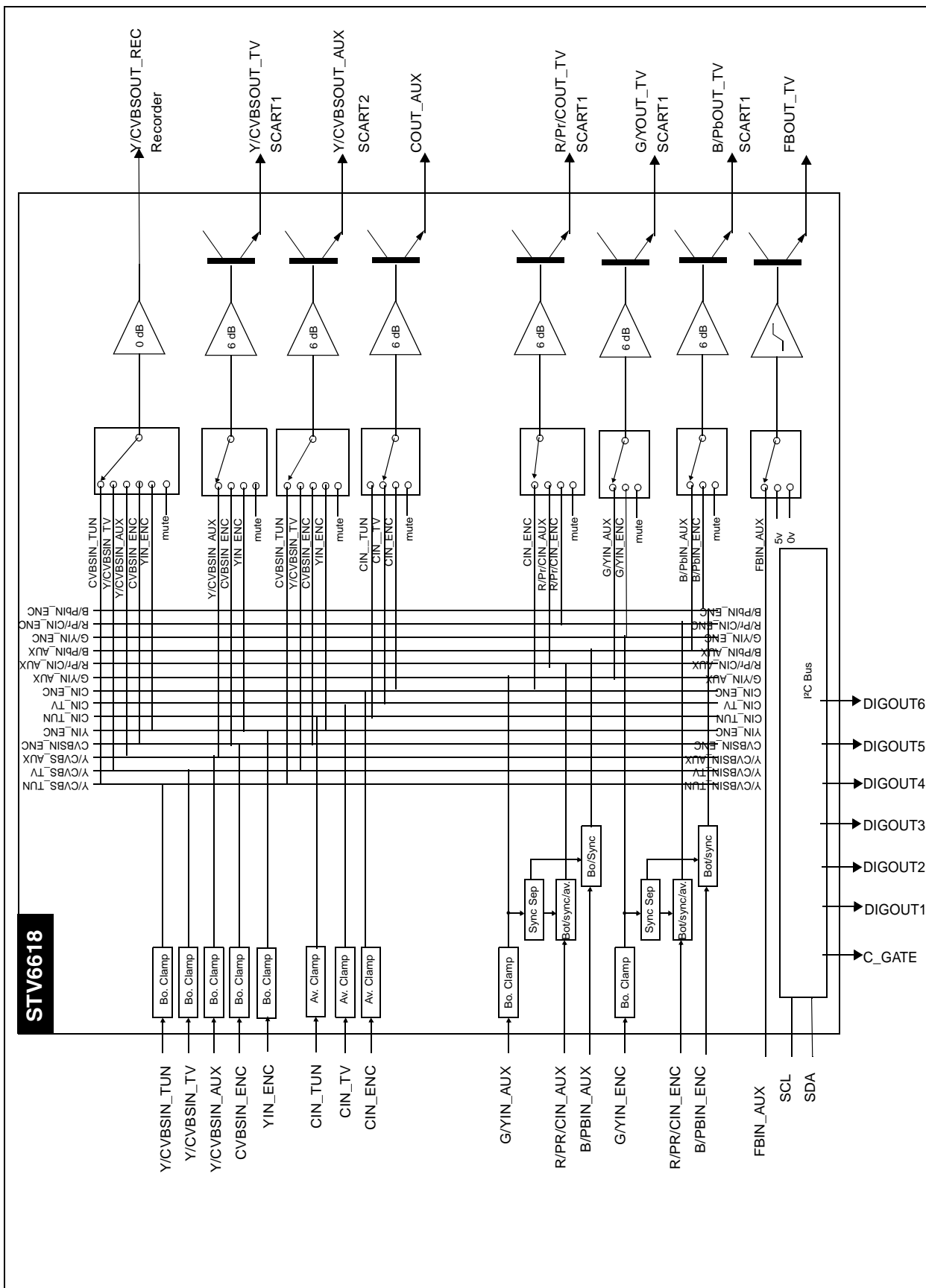
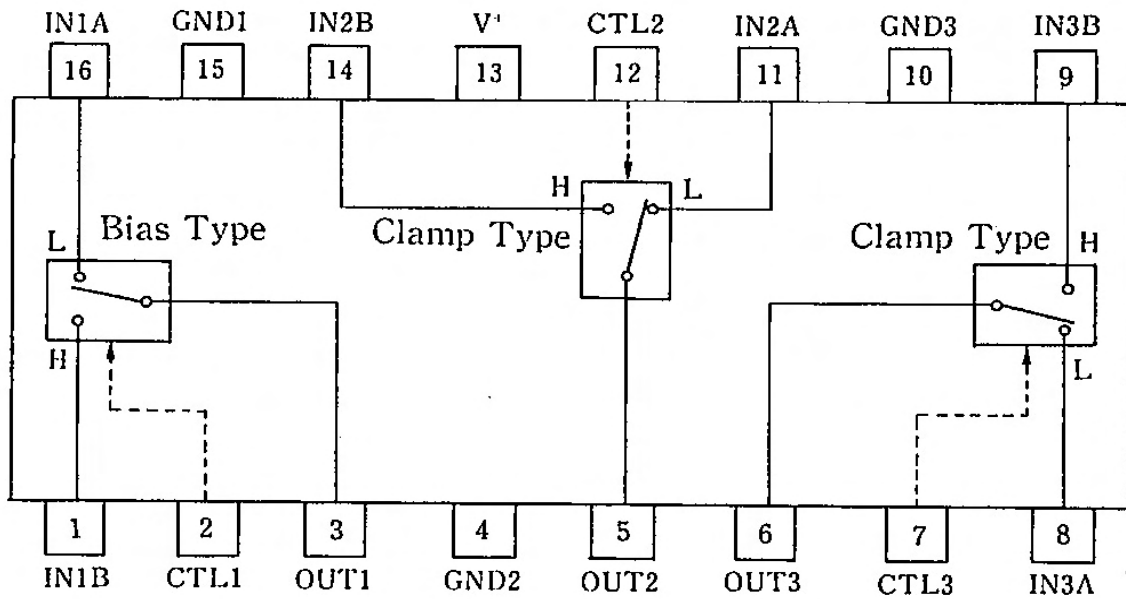


Figure 3: STV6618 Block Diagram



IC7411: NJM2285 Analog Board, Video Switch



NJM2285D
NJM2285M
NJM2285V

IC7313 TEA 1507 Analog Board, Power Supply Control

BLOCK DIAGRAM

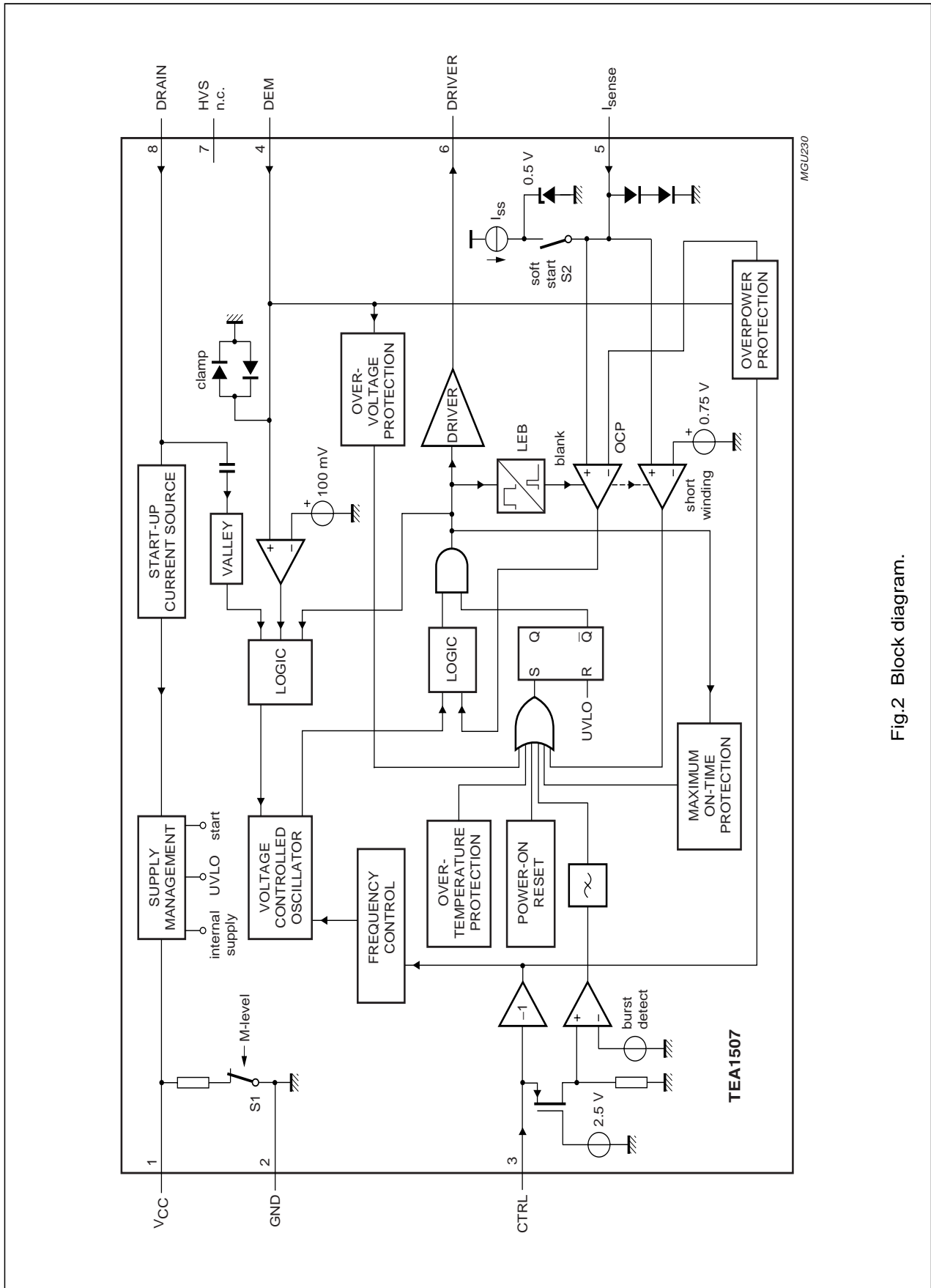
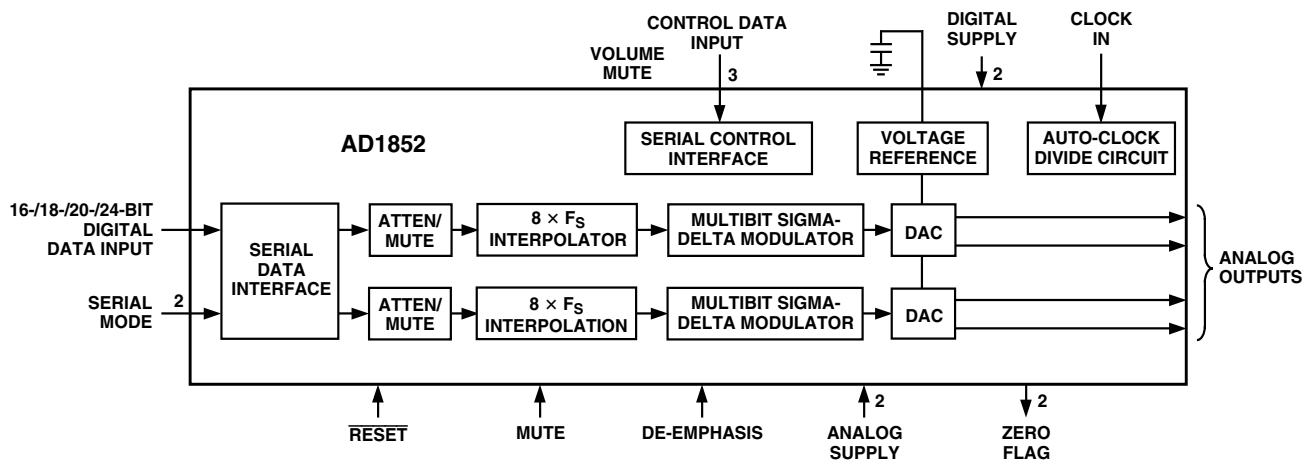


Fig.2 Block diagram.

IC7404: AD1582 Analog Board, Digital/Analogue Converter

FUNCTIONAL BLOCK DIAGRAM



AD1852

PIN FUNCTION DESCRIPTIONS

Pin	Input/Output	Pin Name	Description
1	I	DGND	Digital Ground.
2	I	MCLK	Master Clock Input. Connect to an external clock source at either 256 F _S , 384 F _S , 512 F _S , 768 F _S , or 1024 F _S .
3	I	CLATCH	Latch Input for Control Data. This input is rising-edge sensitive.
4	I	CCLK	Control Clock Input for Control Data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.
5	I	CDATA	Serial Control Input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel-specific attenuation and mute.
6		NC	No Connect.
7	I	192/48	Selects 48 kHz (LO) or 192 kHz Sample Frequency.
8	O	ZEROR	Right Channel Zero Flag Output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.
9	I	DEEMP	De-Emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50 μs/15 μs response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate. Curves for 32 kHz and 48 kHz sample rates may be selected via SPI control register.
10	I	96/48	Selects 48 kHz (LO) or 96 kHz Sample Frequency.
11, 15	I	AGND	Analog Ground.
12	O	OUTR+	Right Channel Positive Line Level Analog Output.
13	O	OUTR-	Right Channel Negative Line Level Analog Output.
14	O	FILTR	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 μF and 0.1 μF capacitors to the AGND.
16	O	OUTL-	Left Channel Negative Line Level Analog Output.
17	O	OUTL+	Left Channel Positive Line Level Analog Output.
18	I	AVDD	Analog Power Supply. Connect to Analog 5 V Supply.
19		FILTB	Filter Capacitor Connection. Connect 10 μF capacitor to AGND (Pin 15).
20	I	IDPM1	Input Serial Data Port Mode Control One. With IDPM0, defines 1 of 4 serial modes.
21	I	IDPM0	Input Serial Data Port Mode Control Zero. With IDPM1, defines 1 of 4 serial modes.
22	O	ZEROL	Left Channel Zero Flag Output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
23	I	MUTE	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
24	I	RESET	Reset. The AD1852 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
25	I	L \overline{R} CLK	Left/Right Clock Input for Input Data. Must run continuously.
26	I	BCLK	Bit Clock Input for Input Data. Need not run continuously; may be gated or used in a burst fashion.
27	I	SDATA	Serial Input, MSB first, containing two channels of 16, 18, 20, and 24 bits of twos complement data per channel.
28	I	DVDD	Digital Power Supply Connect to digital 5 V supply.

Table I. Serial Data Input Mode

IDPM1 (Pin 20)	IDPM0 (Pin 21)	Serial Data Input Format
0	0	Right-Justified
0	1	I ² S-Compatible
1	0	Left-Justified
1	1	DSP

9.12.3 IC's Digital Board 1.5

IC7100: VSM Digital Board 1.5, Versatile Stream Manager

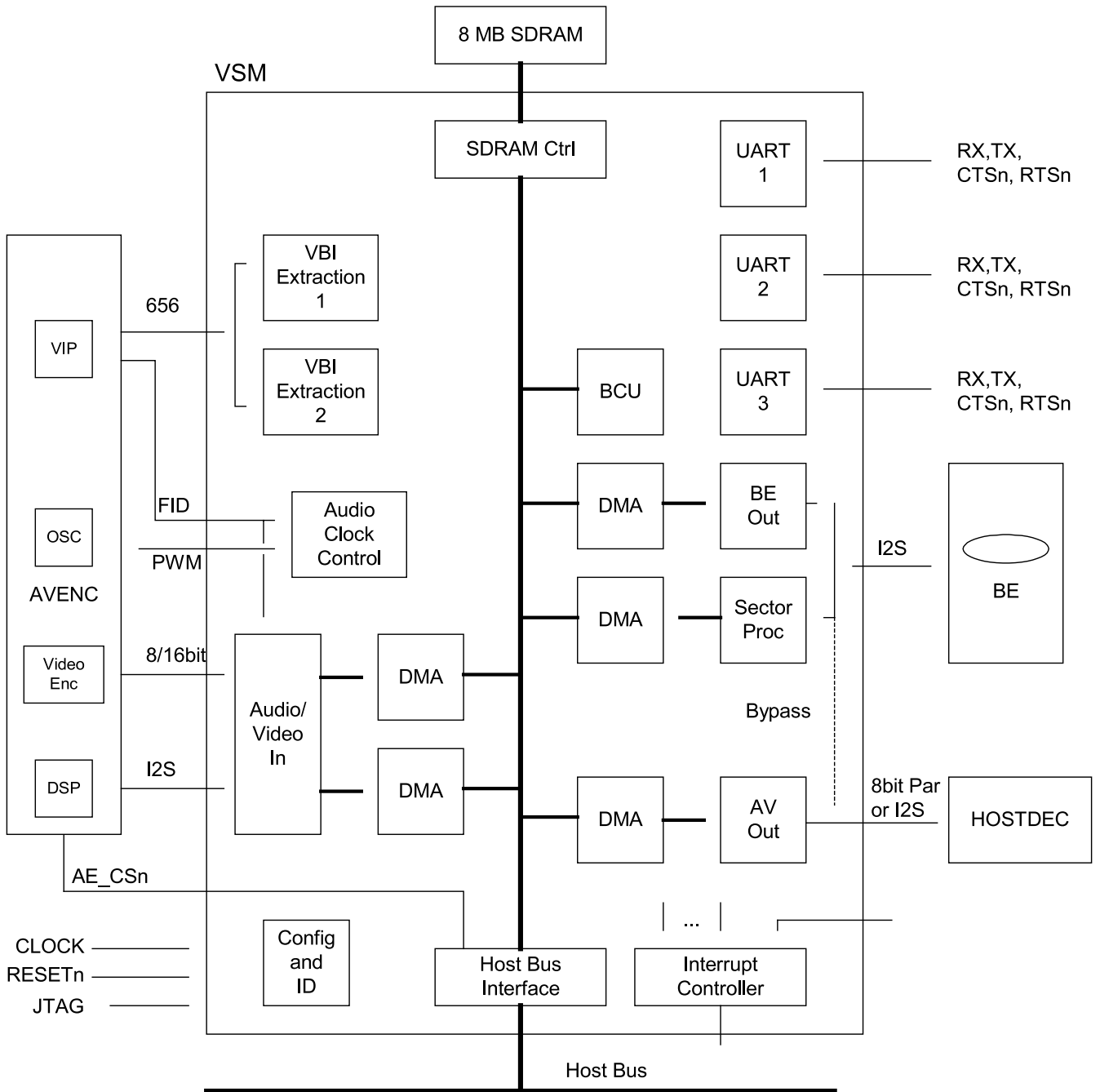


Figure 2.1: VSM Overview

PINNING

OVERVIEW

Name	Pins	Type	Function
System			
RESETn	1	In	
SYSCLK (27MHz)	1	In	
Host Interface			
HO_A(21:1)	21	In	
HO_D(15:0)	16	In/Out	
HO_BEn(1:0)	2	In	
HO_RWn	1	In	
HO_CSIn	1	In	
HO_CSHn	1	In	
HO_A22	1	In	
HO_WAIT	1	Out	
HO_PROCCLK	1	In	
Memory Interface			
M_A(13:0)	14	Out	
M_DQ(15:0)	16	In/Out	
M_RASn	1	Out	
M_CASn	1	Out	
M_WEn	1	Out	
M_LDQM	1	Out	
M_UDQM	1	Out	
M_CLKOUT	1	Out	
M_CLKEN	1	Out	
Basic Engine Interface			
BE_BCLK	1	In	
BE_DATI	1	In	
BE_WCLK	1	In	
BE_SYNC	1	In/Out	
BE_FLAG	1	In	
BE_V4	1	In	
BE_DATO	1	Out	
Video Encoder Interface			
VE_D(15:0)	16	In	
VE_DS _n	1	Out	
VE_DTACK _n	1	In	
VE_VIP_ERROR	1	In	Signal coming from SAA7114
Audio Encoder Interface			
AE_CS _n	1	Out	
AE_BCLK	1	In/Out	(CR151,CR157)
AE_WCLK	1	In/Out	(CR151,CR157)
AE_DATA	1	In	(CR157)

Decoder Interface

D_PAR_D(7:0)	8	Out	
D_PAR_DVALID	1	Out	
D_PAR_STR	1	Out	
D_PAR_REQ	1	In	
D_PAR_SYNC	1	Out	
D_WCLK	1	Out	
D_V4	1	Out	

Audio Clock Control

ACC_FID	1	In	(CR200)
ACC_PWM	1	Out	
ACC_ACLK_OSC	1	In	
ACC_ACLK_DAI	1	In	
ACC_ACLK_PLL	1	In	
ACC_ACLK_DEC	1	Out	

VBI Extractor

VBI_IPD(7:0)	8	In	
VBI_ICLK	1	In	

UART 1

UART1_RX	1	In	
UART1_TX	1	Out (OC)	
UART1_CTSn	1	In	
UART1_RTSn	1	Out (OC)	

UART 2

UART2_RX	1	In	
UART2_TX	1	Out (OC)	
UART2_CTSn	1	In	
UART2_RTSn	1	Out (OC)	

UART 3 (VSM1B)

UART3_RX	1	In	
UART3_TX	1	Out	
UART3_CTSn	1	In	
UART3_RTSn	1	Out	

Interrupt Controller

EXTINT(3:0)	4	In	From: VEnc, AEnc, BE, VSync (STi5505)
CPUINT(1:0)	2	Out (OC)	

JTAG

TCK	1	In	Boundary Scan
TDI	1	In	
TDO	1	Out/Z	
TMS	1	In	
TRSTn	1	In	

Test

TEST0	1	In	Amsal Test
TEST1	1	In	

Power Supply

VDD	20	Power	10% of total pins package
VSS	20	Power	10% of total pins package

Total Pins	208		
------------	-----	--	--

IC7403: SAA6752H (EMPRESS), Digital Board 1.5, MPEG-2 Encoder

5 BLOCK DIAGRAM

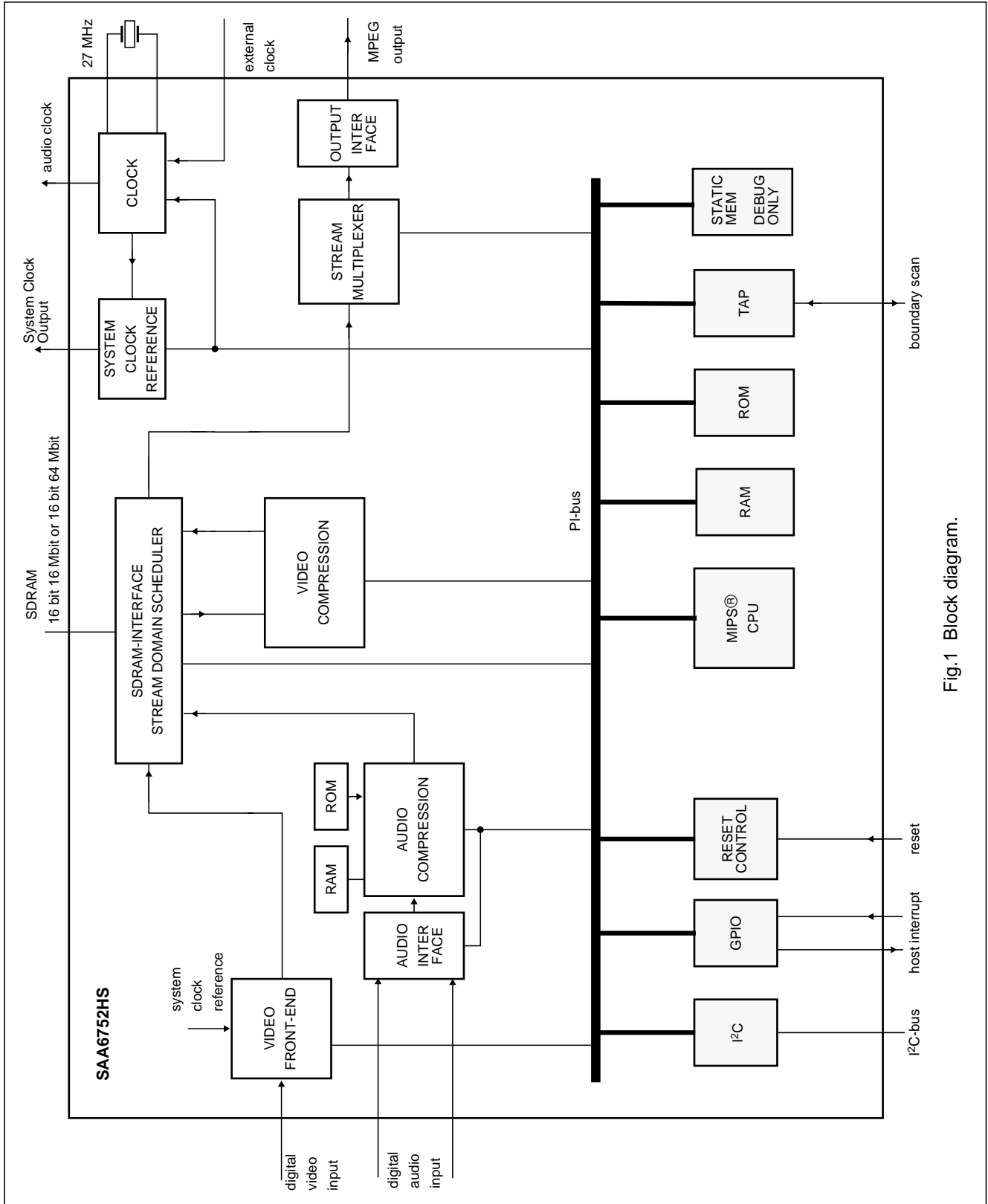


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSP}	1	ground	–	pad ground
SDATA1	2	input	–	I ² S-bus serial data input port 1 with internal pull-down resistor
SCLK1	3	input/output	4	I ² S-bus serial clock port 1 with internal pull-down resistor
SWS1	4	input/output	4	I ² S-bus word select port 1 with internal pull-down resistor
V _{DDP}	5	supply	–	pad ring supply voltage (3.3 V)
SDATA2	6	input/output	4	I ² S-bus serial data port 2 with internal pull-down resistor
SCLK2	7	input/output	4	I ² S-bus serial clock port 2 with internal pull-down resistor
SWS2	8	input/output	4	I ² S-bus word select port 2 with internal pull-down resistor
ACLK	9	output	4	audio clock output ($256 \times f_s$ or $384 \times f_s$)
V _{SSP}	10	ground	–	pad ground
IDQ	11	input	–	reserved (recommended connect to pin V _{SSP}) with internal pull-down resistor
YUV0	12	input	–	video input signal bit 0 (LSB)
YUV1	13	input	–	video input signal bit 1
YUV2	14	input	–	video input signal bit 2
YUV3	15	input	–	video input signal bit 3
YUV4	16	input	–	video input signal bit 4
YUV5	17	input	–	video input signal bit 5
YUV6	18	input	–	video input signal bit 6
YUV7	19	input	–	video input signal bit 7 (MSB)
V _{SSP}	20	ground	–	pad ground
HSYNC	21	input	–	horizontal sync input (video) with internal pull-down resistor
VSYNC	22	input	–	vertical sync input (video) with internal pull-down resistor
FID	23	input	–	video field identification input (odd/even field) with internal pull-down resistor
VCLK1	24	input	–	video clock input 1 (27 MHz) with internal pull-down resistor
V _{SSCO}	25	ground	–	core ground
V _{SSCO}	26	ground	–	core ground
V _{DDCO}	27	supply	–	core supply voltage (2.5 V)
V _{DDCO}	28	supply	–	core supply voltage (2.5 V)
V _{DDP}	29	supply	–	pad ring supply voltage (3.3 V)
VCLK2	30	input	–	video clock input 2 (27 MHz) with internal pull-down resistor
PDOAV	31	3-state output	4	parallel stream data output for audio/video identifier
PDIDS	32	input	–	parallel stream data input for data strobe (request for packet in Data Expansion Bus Interface (DEBI) slave mode) with internal pull-up resistor
PDOSYNC	33	3-state output	4	parallel stream data output for packet sync
V _{SSP}	34	ground	–	pad ground
PDOVAL	35	3-state output	4	parallel stream data valid output with internal pull-up resistor
PDO0	36	3-state output	4	parallel stream data output bit 0 (LSB)

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
PDO1	37	3-state output	4	parallel stream data output bit 1
PDO2	38	3-state output	4	parallel stream data output bit 2
V _{DDP}	39	supply	–	pad ring supply voltage (3.3 V)
PDO3	40	3-state output	4	parallel stream data output bit 3
PDO4	41	3-state output	4	parallel stream data output bit 4
PDO5	42	3-state output	4	parallel stream data output bit 5
PDO6	43	3-state output	4	parallel stream data output bit 6
V _{SSP}	44	ground	–	pad ground
PDO7	45	3-state output	4	parallel stream data output bit 7 (MSB)
PDI0CLK	46	input/output	4	parallel stream clock input/output
I2CADDRSEL	47	input	–	I ² C-bus address select input with internal pull-up resistor
SD_DQ15	48	input/output	8	SDRAM data input/output bit 15 (MSB)
V _{DDP}	49	supply	–	pad ring supply voltage (3.3 V)
SD_DQ0	50	input/output	8	SDRAM data input/output bit 0 (LSB)
SD_DQ14	51	input/output	8	SDRAM data input/output bit 14
SD_DQ1	52	input/output	8	SDRAM data input/output bit 1
V _{SSP}	53	ground	–	pad ground
SD_DQ13	54	input/output	8	SDRAM data input/output bit 13
SD_DQ2	55	input/output	8	SDRAM data input/output bit 2
SD_DQ12	56	input/output	8	SDRAM data input/output bit 12
V _{DDP}	57	supply	–	pad ring supply voltage (3.3 V)
SD_DQ3	58	input/output	8	SDRAM data input/output bit 3
SD_DQ11	59	input/output	8	SDRAM data input/output bit 11
SD_DQ4	60	input/output	8	SDRAM data input/output bit 4
SD_DQ10	61	input/output	8	SDRAM data input/output bit 10
V _{SSP}	62	ground	–	pad ground
SD_DQ5	63	input/output	8	SDRAM data input/output bit 5
SD_DQ9	64	input/output	8	SDRAM data input/output bit 9
SD_DQ6	65	input/output	8	SDRAM data input/output bit 6
SD_DQ8	66	input/output	8	SDRAM data input/output bit 8
V _{DDP}	67	supply	–	pad ring supply voltage (3.3 V)
SD_DQ7	68	input/output	8	SDRAM data input/output bit 7
SD_DQM1	69	output	8	SDRAM data mask enable output bit 1
SD_DQM0	70	output	8	SDRAM data mask enable output bit 0 (LSB)
SD_WE	71	output	8	SDRAM write enable output (active LOW)
V _{SSP}	72	ground	–	pad ground
SD_CAS	73	output	8	SDRAM column address strobe output (active LOW)
SD_CLK	74	output	8	SDRAM clock output
SD_RAS	75	output	8	SDRAM row address strobe output (active LOW)
SD_CKE	76	output	8	SDRAM clock enable output

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSCO}	77	ground	–	core ground
V _{SSCO}	78	ground	–	core and substrate ground
V _{DDCO}	79	supply	–	core supply voltage (2.5 V)
V _{DDCO}	80	supply	–	core supply voltage (2.5 V)
V _{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
SD_CS	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V _{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V _{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V _{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V _{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V _{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V _{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V _{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSCO}	77	ground	–	core ground
V _{SSCO}	78	ground	–	core and substrate ground
V _{DDCO}	79	supply	–	core supply voltage (2.5 V)
V _{DDCO}	80	supply	–	core supply voltage (2.5 V)
V _{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
SD_CS	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V _{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V _{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V _{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V _{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V _{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V _{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V _{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

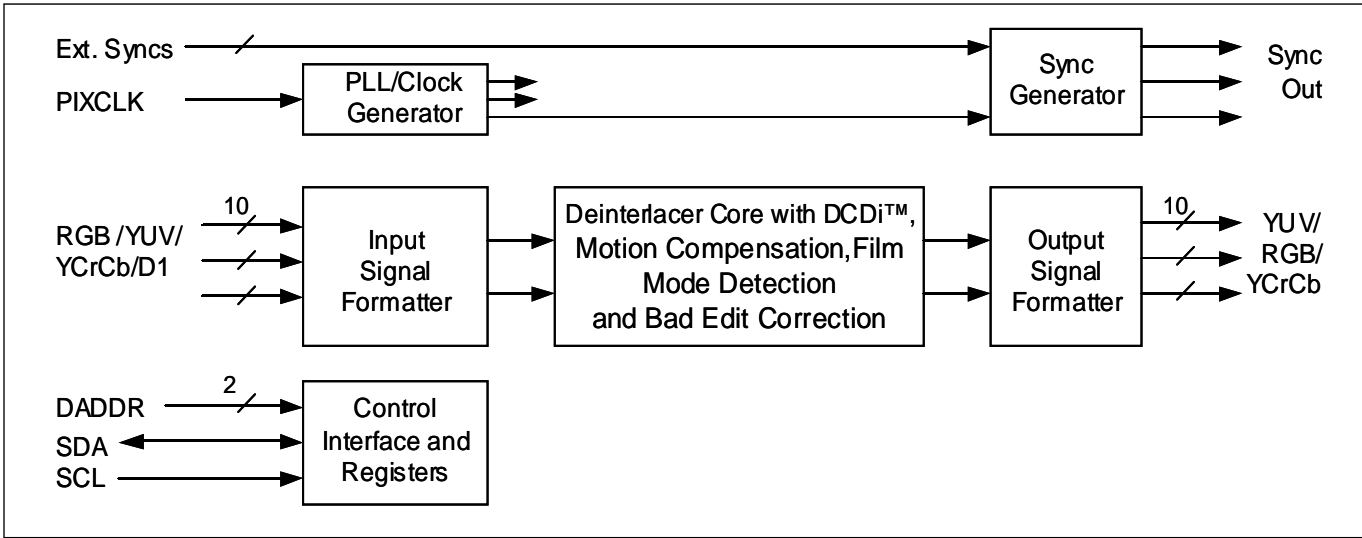
SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SD_DQ21	117	input/output	8	reserved (do not connect)
SD_DQ25	118	input/output	8	reserved (do not connect)
V _{DDP}	119	supply	–	pad ring supply voltage (3.3 V)
SD_DQ22	120	input/output	8	reserved (do not connect)
SD_DQ24	121	input/output	8	reserved (do not connect)
SD_DQ23	122	input/output	8	reserved (do not connect)
EXTCLK	123	input	–	27 MHz external clock input with internal pull-up resistor
V _{SSP}	124	ground	–	pad ground
V _{SSA}	125	ground	–	oscillator analog ground
XTALI	126	analog input	–	crystal oscillator input (27 MHz); note 2
XTALO	127	analog output	–	crystal oscillator output (27 MHz)
V _{DDA}	128	supply	–	oscillator analog supply voltage (2.5 V)
V _{SSCO}	129	ground	–	core ground
V _{SSCO}	130	ground	–	core ground
V _{DDCO}	131	supply	–	core supply voltage (2.5 V)
V _{DDCO}	132	supply	–	core supply voltage (2.5 V)
V _{DDP}	133	supply	–	pad ring supply voltage (3.3 V)
TDI	134	input	–	boundary scan test data input; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TMS	135	input	–	boundary scan test mode select; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TCK	136	input	–	boundary scan test clock; pin must be set to LOW during normal operating; with internal pull-up resistor; note 3
TDO	137	3-state output	4	boundary scan test data output; pin not active during normal operating; with 3-state output; note 3
V _{SSP}	138	ground	–	pad ground
$\overline{\text{TRST}}$	139	input	–	test reset input (active LOW), for boundary scan test (with internal pull-up); notes 3 and 4
CLKOUT	140	output	4	27 MHz system clock output
TEST0	141	input/output	4	reserved (do not connect)
TEST1	142	input/output	4	reserved (do not connect)
V _{DDP}	143	supply	–	pad ring supply voltage (3.3 V)
TEST2	144	input/output	4	reserved (do not connect)
SDA	145	input/open-drain output	–	serial data input/output (I ² C-bus)
SCL	146	input/open-drain output	–	serial clock input/output (I ² C-bus)
$\overline{\text{RESET}}$	147	input	–	reset input (active LOW); with internal pull-up resistor
V _{SSP}	148	ground	–	pad ground
$\overline{\text{RTS}}$	149	output	4	reserved (do not connect); Universal Asynchronous Receiver/Transmitter (UART) request to send output (active LOW)

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
CTS	150	input	–	reserved (recommended connect to pin V _{DDP}); UART clear to send input; external static memory select input (active LOW); with internal pull-up resistor
RXD	151	input	–	reserved (recommended connect to pin V _{DDP}); UART receive data; internal boot select input; with internal pull-up resistor
TXD	152	output	4	reserved (do not connect); UART transmit data
V _{DDP}	153	supply	–	pad ring supply voltage (3.3 V)
SM_LB	154	input/output	4	reserved (do not connect)
SM_UB	155	input/output	4	reserved (do not connect)
H_IRF	156	3-state output	4	host interrupt ?ag output; with internal pull-up resistor
V _{SSP}	157	ground	–	pad ground
SM_OE	158	output	4	reserved (do not connect), static memory output enable output (active LOW)
SM_A9	159	output	4	reserved (do not connect), static memory address output bit 9
SM_A10	160	output	4	reserved (do not connect), static memory address output bit 10
V _{DDP}	161	supply	–	pad ring supply voltage (3.3 V)
SM_A8	162	output	4	reserved (do not connect), static memory address output bit 8
SM_A11	163	output	4	reserved (do not connect), static memory address output bit 11
SM_A7	164	output	4	reserved (do not connect), static memory address output bit 7
SM_A12	165	output	4	reserved (do not connect), static memory address output bit 12
V _{SSP}	166	ground	–	pad ground
SM_A6	167	output	4	reserved (do not connect), static memory address output bit 6
SM_A13	168	output	4	reserved (do not connect), static memory address output bit 13
SM_A5	169	output	4	reserved (do not connect), static memory address output bit 5
SM_A14	170	output	4	reserved (do not connect), static memory address output bit 14
V _{DDP}	171	supply	–	pad ring supply voltage (3.3 V)
SM_WE	172	output	4	reserved (do not connect), static memory write enable output (active LOW)
SM_D7	173	input/output	4	reserved (do not connect), static memory data input/output bit 7 with internal pull-down resistor
SM_D8	174	input/output	4	reserved (do not connect), static memory data input/output bit 8 with internal pull-down resistor
SM_D6	175	input/output	4	reserved (do not connect), static memory data input/output bit 6 with internal pull-down resistor
V _{SSP}	176	ground	–	pad ground
SM_D9	177	input/output	4	reserved (do not connect), static memory data input/output bit 9 with internal pull-down resistor
SM_D5	178	input/output	4	reserved (do not connect), static memory data input/output bit 5 with internal pull-down resistor
SM_D10	179	input/output	4	reserved (do not connect), static memory data input/output bit 10 with internal pull-down resistor

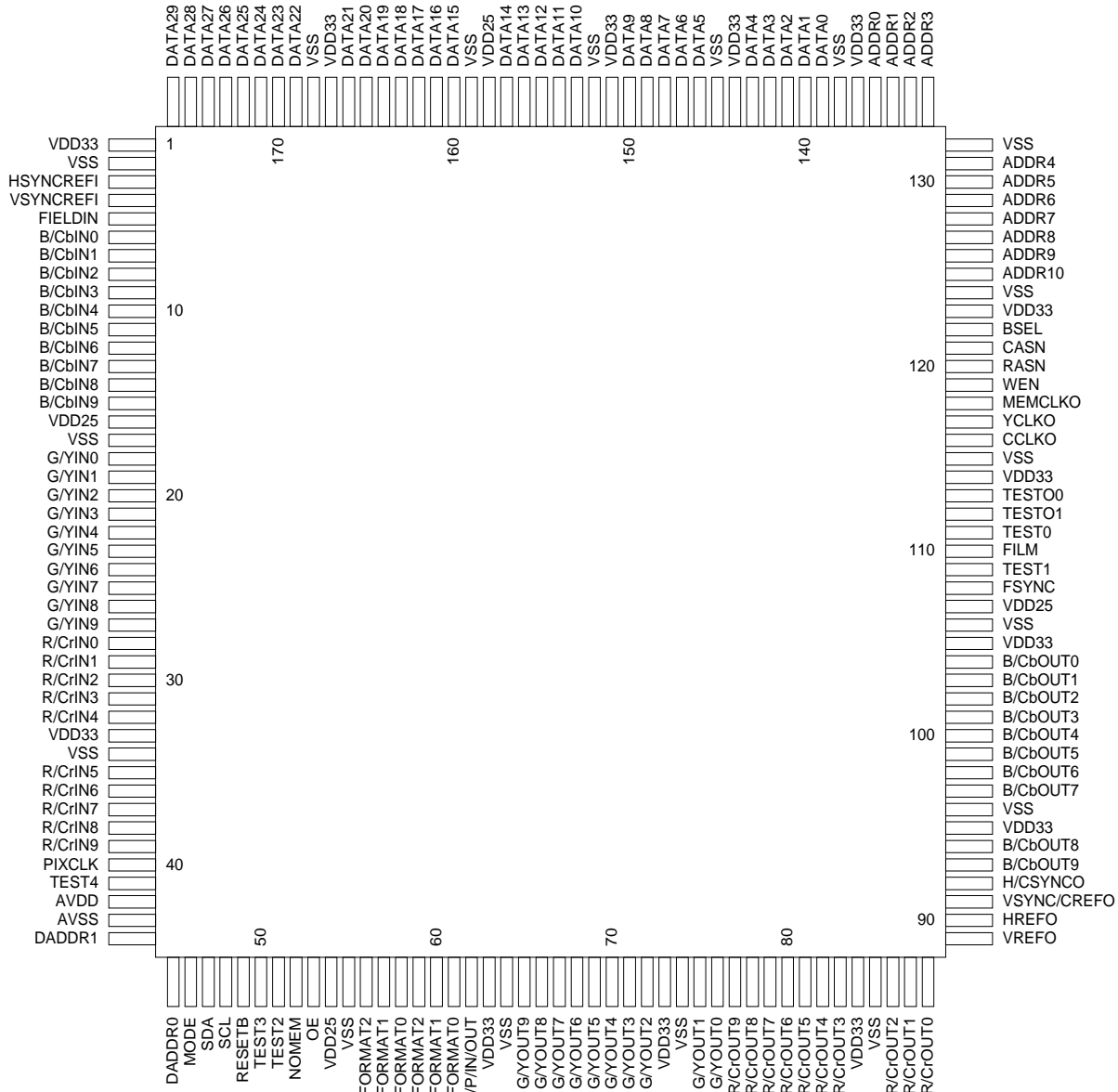
SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SM_D4	180	input/output	4	reserved (do not connect), static memory data input/output bit 4 with internal pull-down resistor
V _{SSCO}	181	ground	–	internal pre-driver and substrate ground
V _{SSCO}	182	ground	–	core ground
V _{DDCO}	183	supply	–	core supply voltage (2.5 V)
V _{DDCO}	184	supply	–	internal pre-driver supply voltage (2.5 V)
V _{DDP}	185	supply	–	pad ring supply voltage (3.3 V)
SM_D11	186	input/output	4	reserved (do not connect), static memory data input/output bit 11 with internal pull-down resistor
SM_D3	187	input/output	4	reserved (do not connect), static memory data input/output bit 3 with internal pull-down resistor
SM_D12	188	input/output	4	reserved (do not connect), static memory data input/output bit 12 with internal pull-down resistor
SM_D2	189	input/output	4	reserved (do not connect), static memory data input/output bit 2 with internal pull-down resistor
V _{SSP}	190	ground	–	pad ground
SM_D13	191	input/output	4	reserved (do not connect), static memory data input/output bit 13 with internal pull-down resistor
SM_D1	192	input/output	4	reserved (do not connect), static memory data input/output bit 1 with internal pull-down resistor
SM_D14	193	input/output	4	reserved (do not connect), static memory data input/output bit 14 with internal pull-down resistor
SM_D0	194	input/output	4	reserved (do not connect), static memory data input/output bit 0 (LSB) with internal pull-down resistor
V _{DDP}	195	supply	–	pad ring supply voltage (3.3 V)
SM_D15	196	input/output	4	reserved (do not connect), static memory data input/output bit 15 (MSB) with internal pull-down resistor
SM_CS ³	197	output	4	reserved (do not connect), static memory chip select output for external ROM or RAM (active LOW)
SM_A4	198	output	4	reserved (do not connect), static memory address output bit 4
SM_A3	199	output	4	reserved (do not connect), static memory address output bit 3
V _{SSP}	200	ground	–	pad ground
SM_A2	201	output	4	reserved (do not connect), static memory address output bit 2
SM_A15	202	output	4	reserved (do not connect), static memory address output bit 15
SM_A1	203	output	4	reserved (do not connect), static memory address output bit 1
SM_A16	204	output	4	reserved (do not connect), static memory address output bit 16
V _{DDP}	205	supply	–	pad ring supply voltage (3.3 V)
SM_A0	206	output	4	reserved (do not connect), static memory address output bit 0 (LSB)
SM_A17	207	output	4	reserved (do not connect), static memory address output bit 17 (MSB)
SM_CS ⁰	208	output	4	reserved (do not connect)

IC7700: FLI2200, Digital Board 1.5, Deinterlacer

Simplified Block Diagram



Pin description



Pin #	Name	Description
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence. This can be overridden by the NMOvr bit, bit 1 in register 05 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 05 _H for details.
27-18	G/YIN _{9,0}	10-bit green or luminance signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN _{9,0}	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN _{9,0}	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00 _H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00 _H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00 _H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

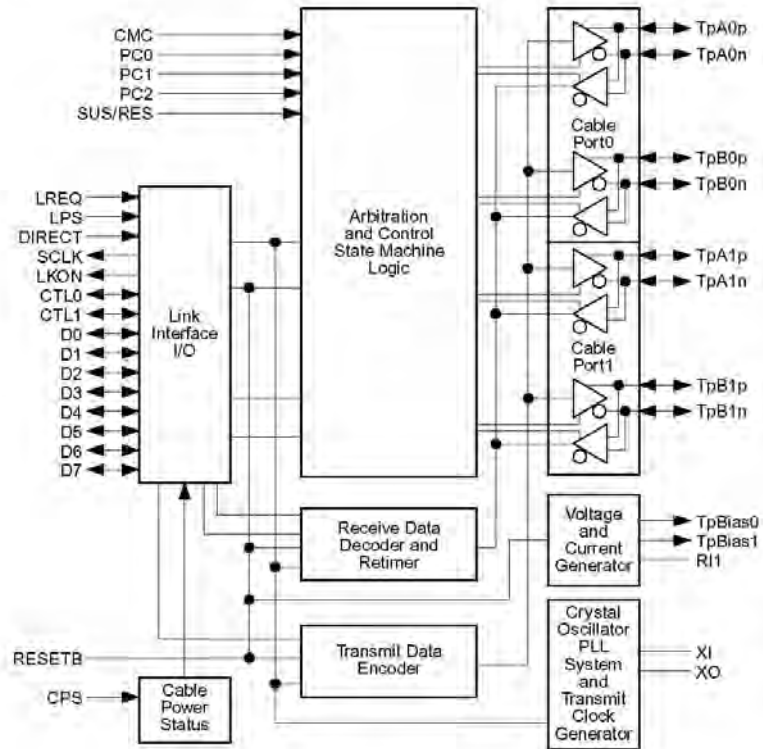
Pin Connections and Functions

Pin #	Name	Description
See list	V _{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V _{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V _{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV _{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV _{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV _{SS} pin..
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	IFORMAT ₂₋₀	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details.
59-61	OFORMAT ₂₋₀	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details.
44-45	DADDR ₁₋₀	The settings of DADDR ₁₋₀ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. DADDR ₁₋₀ allow the device address to be set to any of the following values: C0/C1 _H , C2/C3 _H , E0/E1 _H , E2/E3 _H . Please refer to the section “Control Bus Operation and Protocol” for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to be programmed from an external controller. When it is set high the FLI2200 will self-program from an external I ² C memory connected to the bus. Please refer to the “Control Bus Operation and Control Protocol” section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the NPOP ₁₋₀ bits, bits 5-4 in register 03 _H , are set to 00 _H , overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
65-72 75-76	G/YOUT ₉₋₀	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT ₉₋₀	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT ₉₋₀	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
108	FSYNC	Film mode sync output. When film mode is detected this pin will toggle in sync with the 3:2 (NTSC) or 2:2 (PAL and 30 Hz film in NTSC) pulldown sequence detected in the source.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
125-131 133-136	ADDR ₁₀₋₀	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A ₁₀₋₀ bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	DATA ₂₉₋₀	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ ₂₉₋₀ bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k Ω resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock..
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A ₁₁) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A ₁₁) pin on the SDRAM and BA1/BS1 (also called BA when BA0 is referred to as A ₁₁) should be tied low.
41, 50, 51, 109, 111	TEST ₄₋₀	These pins are used for test purposes only and should always be tied low for normal operation.
112, 113	TESTO ₁₋₀	These pins are test outputs and should be left unconnected in normal operation.

9.12.4 IC's Divio 1.8

IC7400: uPD72852, DVIO Board, IEEE1394 Physical Layer Chip**BLOCK DIAGRAM**

1.1 Cable Interface Pins

Name	Pin No.	I/O	Function
TpA0p	39	I/O	Port 0 twisted pair cable A positive phase I/O
TpA0n	38	I/O	Port 0 twisted pair cable A negative phase I/O
TpB0p	37	I/O	Port 0 twisted pair cable B positive phase I/O
TpB0n	36	I/O	Port 0 twisted pair cable B negative phase I/O
TpA1p	46	I/O	Port 1 twisted pair cable A positive phase I/O
TpA1n	45	I/O	Port 1 twisted pair cable A negative phase I/O
TpB1p	44	I/O	Port 1 twisted pair cable B positive phase I/O
TpB1n	43	I/O	Port 1 twisted pair cable B negative phase I/O
SUS/RES	19	I	Suspend/Resume function select 1: Suspend/Resume on (IEEE1394a-2000 compliant) 0: Suspend/Resume off (P1394a draft 1.3 compliant)
CPS	32	I	Cable power status Connect to the cable through a 390 k Ω resistor and to GND through a 100 k Ω resistor. 0: Cable power fail 1: Cable power on

1.2 Link Interface Pins

Name	Pin No.	I/O	Function
D0	8	I/O	Data input/output (bit 0)
D1	9	I/O	Data input/output (bit 1)
D2	11	I/O	Data input/output (bit 2)
D3	12	I/O	Data input/output (bit 3)
D4	14	I/O	Data input/output (bit 4)
D5	15	I/O	Data input/output (bit 5)
D6	17	I/O	Data input/output (bit 6)
D7	18	I/O	Data input/output (bit 7)
CTL0	5	I/O	Link interface control (bit 0)
CTL1	6	I/O	Link interface control (bit 1)
LREQ	63	I	Link request input
SCLK	2	O	Link control output clock LPS 1: 49.152 MHz output LPS 0: Clamp to 0 (The clock signal will be output within 25 μ sec after change to "0")
LPS	59	I	Link power status input 0: Link power off 1: Link power on (PHY/Link direct connection)
LKON	58	O	Link-on signal output Link-on signal is 6.144 MHz clock output. Please refer to 4.2 Link-on Indication .
DIRECT	50	I	PHY/Link isolation barrier control input 0: Isolation barrier 1: PHY/Link direct connection

1.3 Control Pins

Name	Pin No.	I/O	Function
PC0	26	I	Power class set input
PC1	27	I	This pin status will be loaded to Pwr_class bit which allocated to PHY register 4H. IEEE1394a-2000 chapter [4.3.4.1]
PC2	28	I	
CMC	30	I	Configuration manager capable setting This pin status will be loaded to Contender bit which allocated to PHY register 4H. 0: Non contender 1: Contender
RESETB	55	I	Power-on reset input Connect to GND through a 0.1 μ F capacitor. 0: Reset 1: Normal
SPD	61	I	Speed select 0: MAX. S200 1: MAX. S400

1.4 IC

Name	Pin No.	I/O	Function
IC(AL)	29, 51	-	Internally Connected (Low Clamped) Connect to GND.
IC(DL)	3	-	Internally Connected (Low Clamped) Connect to GND.

1.5 Power Supply Pins

Name	Pin No.	I/O	Function
AV _{DD}	25, 31, 40, 47, 54	-	Analog power
AGND	24, 33, 35, 42, 49, 52, 53	-	Analog GND
DV _{DD}	4, 10, 20, 56, 60	-	Digital V _{DD}
DGND	1, 7, 13, 16, 21, 57, 64	-	Digital GND

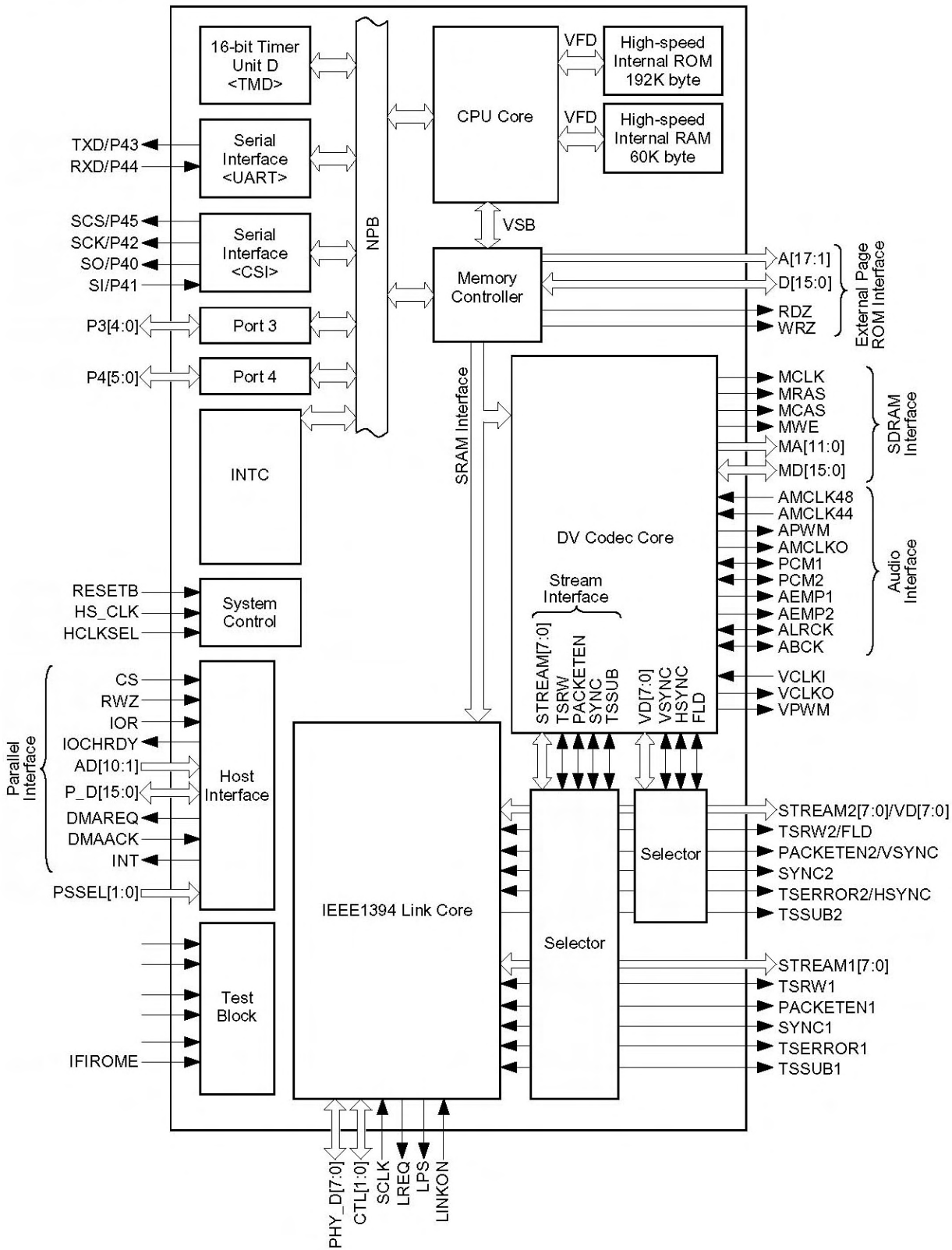
1.6 Other Pins

Name	Pin No.	I/O	Function
TpBias0	41	O	Port 0 twisted pair output
TpBias1	48	O	Port 1 twisted pair output
RI1	34	-	Resistor connection pin1 for reference current generator Connect to GND through a 9.1 k Ω resistor.
XI	23	-	Crystal oscillator connection XI
XO	22	-	Crystal oscillator connection XO
TEST	62	-	Test pin Internally connected (Low clamped). Connect to GND.

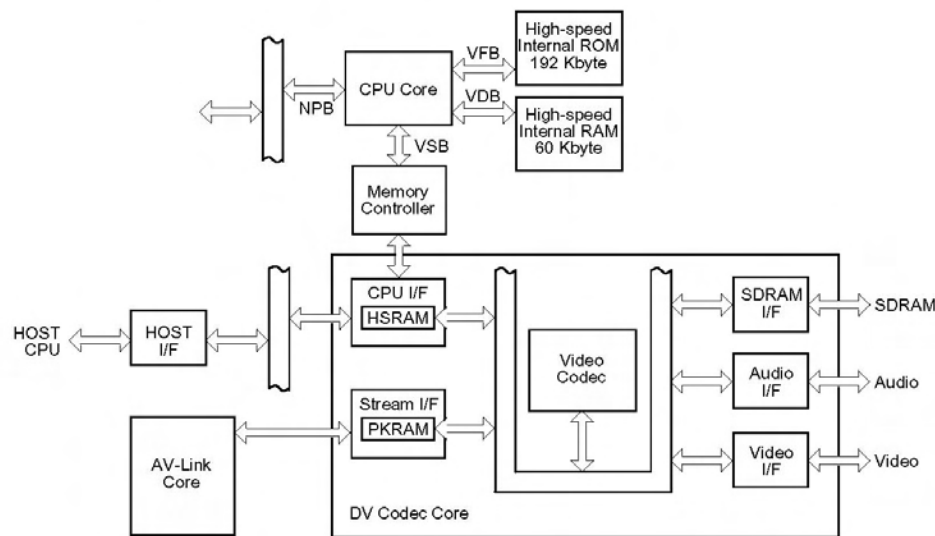
IC7431: uPD72893, DVIO Board, IEEE1394 Link Layer Chip and DV Decoder

BLOCK DIAGRAM

μPD72893 Block Diagram



DV Codec Unit Block Diagram



1. PIN FUNCTIONS

(1) Link-related pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
LINKON	18	I	Link-on signal input. Clock input. Inputs 0 if LPS is active.	—	I	—
LPS	17	O	Link power status output Link power OFF : 0 Link power ON : 2.7 MHz pulse output (54 MHz host clock divided by 20)	—	O	—
LREQ	16	O	Link request output	—	O	—
SCLK	15	I	Clock input for Link control When LPS is active : 49.152 MHz input LPS = 0 : Fixed to 0	—	I	—
CTL[1:0]	12, 13	I/O	PHY/Link control signal I/O	—	I	—
PHY_D[7:0]	2 to 4, 6 to 8, 10, 11	I/O	Data I/O between PHY and Link	—	I	—
STREAM1[7:0]	26 to 19	I/O	ISO data bus of stream interface 1 ^{Note}	—	I	—
PACKETEN1	27	I/O	Packet enable signal I/O to/from stream interface 1 ^{Note}	H/L	I	—
TSERROR1	28	I/O	Packet error signal I/O to/from stream interface 1 ^{Note}	H/L	I	—
TSRW1	29	I/O	Data read/write enable signal I/O to/from stream interface 1 ^{Note}	—	I	—
SYNC1	30	I/O	Frame sync signal I/O to/from stream interface 1 ^{Note}	H/L	I	—
TSSUB1	32	I/O	I : Inputs the packet gap signal when the stream is input through the stream interface O : Not used. Connect this pin to V _{DD} or GND via a resistor.	H/L	I	—
STREAM2[7:0]	47 to 40	I/O	ISO data bus of stream interface 2 ^{Note}	—	I	VD[7:0]
PACKETEN2	33	I/O	Packet enable signal I/O to/from stream interface 2 ^{Note}	H/L	I	VSYNC
TSERROR2	34	I/O	Packet error signal I/O to/from stream interface 2 ^{Note}	H/L	I	HSYNC
TSRW2	36	I/O	Data read/write enable signal I/O to/from stream interface 2 ^{Note}	—	I	FLD
SYNC2	37	I/O	Frame sync signal I/O to/from stream interface 2. ^{Note}	H/L	I	—
TSSUB2	38	O	Not used. Leave open.	—	O	—

Note When this signal is switched for transmission or reception to/from IEEE1394, it must be controlled that output does not conflict.

To prevent a floating state, connect a pull-up or pull-down resistor to this pin.

(2) Video interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
VCLKI	50	I	Video clock input (27 MHz)	–	–	–
VCLKO	51	O	Video clock output (27 MHz)	–	–	–
VD[7:0]	47 to 40	I/O	Video data signal	–	–	STREAM2[7:0]
VSYNC	33	I/O	Vertical sync video signal ^{Note}	L	–	PACKETEN2
HSYNC	34	I/O	Horizontal sync video signal ^{Note}	L	–	TSERROR2
FLD	36	I/O	Field index signal ^{Note}	–	–	TSRW2
VPWM	53	O	PWM signal for video PLL	–	–	–

Note: When this signal is switched for transmission or reception to/from IEEE1394, it must be controlled that output does not conflict.

(3) Audio interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
AMCLK48	104	I	Audio master clock input (for 48 kHz sampling frequency)	–	–	–
AMCLK44	103	I	Audio master clock input (for 44.1 kHz sampling frequency)	–	–	–
AMCLKO	101	O	Audio master clock output	–	–	–
PCM1	96	I/O	Audio PCM serial data ^{Note} With 2 channels: CH1 With 4 channels: CH1 or CH1 and CH2 mixed	–	–	–
PCM2	97	I/O	Audio PCM serial data ^{Note} With 2 channels: Mute With 4 channels: CH2	–	–	–
AEMP1	98	O	PCM1 emphasis ON/OFF for PCM1 output	H	–	–
AEMP2	100	O	PCM2 emphasis ON/OFF for PCM2 output	H	–	–
ALRCK	93	I/O	Audio LR clock ^{Note} L-ch: High R-ch: Low	–	–	–
ABCK	94	I/O	Audio bit clock ^{Note}	–	–	–
AFS[1:2]	48, 49	O	Audio sampling frequency AFS2 AFS1 44.1 kHz 0 1 48 kHz 0 0 32 kHz 1 0	–	–	–
APWM	102	O	PWM signal for audio PLL	–	–	–

Note: The input changes according to the switching of the encode/decode mode. It must be controlled so that the output does not conflict when the mode is switched.

To prevent a floating state, connect a pull-up or pull-down resistor to this pin.

(4) SDRAM interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
MCLK	77	O	CLK pin connection for SDRAM	–	–	–
MRAS	76	O	RAS pin connection for SDRAM	–	–	–
MCAS	75	O	CAS pin connection for SDRAM	–	–	–
MWE	74	O	WE pin connection for SDRAM	–	–	–
MA[11:0]	92, 90 to 83, 81 to 79	O	Address pin connection for SDRAM	–	–	–
MD[15:0]	73 to 69, 66 to 64, 62 to 57, 55, 54	I/O	Data pin connection for SDRAM These pins must be pulled up or down and then must be directly connected to the SDRAM pins.	–	–	–

(5) Host interface pins

(a) Parallel interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
CS	117	I	Parallel interface chip select input	L	I	–
RWZ	119	I	Parallel interface read/write control input ISA bus, SH-1 bus : Write strobe 68000 bus : Read/write select signal	L	I	–
IOR	120	I	Parallel interface IO read control input ISA bus, SH-1 bus : Read strobe 68000 bus : Data strobe (DS)	L	I	–
IOCHRDY	123	O	Parallel interface ready output	L	O	–
AD[10:1]	116 to 107	I	Parallel interface address input	–	I	–
P_D[15:0]	143 to 141, 139 to 132, 130 to 128, 126, 125	I/O	Parallel interface data input/output	–	I	–
DMAREQ	122	O	DMA request output	L	O	SIO_CNTO
DMAACK	121	I	DMA acknowledge input for parallel interface	L	I	SIO_CNTI

(b) Serial interface pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
SO	145	O	Serial transmit data output for clocked serial interface (CSI)	–	O	P40
SI	146	I	Serial receive data input for clocked serial interface (CSI)	–	I	P41
SCK	147	O	Clock output for clocked serial interface (CSI)	–	O	P42
TXD	149	O	Serial transmit data output for asynchronous serial interface (UART)	–	O	P43
RXD	150	I	Serial transmit data input for asynchronous serial interface (UART)	–	I	P44
SCS	151	O	Chip select output for clocked serial interface (CSI)	–	O	P45
SIO_CNTI	121	I	Control input for asynchronous serial interface (UART). Externally input data is loaded in synchronization with the end of RXD of UART.	–	I	DMAACK
SIO_CNTO	122	O	Control output for asynchronous serial interface (UART)	–	O	DMAREQ

(c) Others

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
INT	124	O	Interrupt output to external device	H	O	–
PSSEL[1:0]	106, 105	I	Parallel/serial interface selection. These signals select a parallel or serial interface as the external interface. PSSEL[1:0] Selected Interface 00 Serial interface (UART) 01 Parallel interface (ISA bus) 10 Parallel interface (68000 bus) 11 Parallel interface (SH-1 bus)	–	I	–

(6) Port pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
P30	204	I/O	Port 3. This is a 4-bit I/O port that can be set in the input or output mode in 1-bit units. P30 : Connect this pin to GND via a resistor. P32 : This pin outputs an interrupt to the external device to read the DV status. It cannot be used as a port pin when DV is used.	-	I	-
P31	152					-
P32	153					-
P33	154					-
P34	155					-
P40	145	I/O	Port 4. This is a 6-bit I/O port that can be set in the input or output mode in 1-bit units. P40 to P45 are multiplexed with the pins described under the heading Alternate Function (they cannot be used as general-purpose port pins).	-	I	SO
P41	146					SI
P42	147					SCK
P43	149					TXD
P44	150					RXD
P45	151					SCS

(7) External ROM connection pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
D[15:0]	196, 194 to 189, 186 to 178	I/O	External ROM data bus. External ROM data bus used to access external ROM	-	I	-
A[17:1]	175, 174, 172, 171, 169 to 167, 165 to 156	O	External ROM address bus. External ROM address bus used to access external ROM. A space of 256 KB can be addressed.	-	O	-
RDZ	176	O	ROM read. This is a strobe signal that indicates a read cycle to the external ROM. It is inactive in the idle state.	L	O	-
WRZ	177	O	ROM write. This is a strobe signal that indicates a write cycle to the external ROM.	L	O	-

(8) Clock and reset pins

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function									
RESETB	1	I	<p>Reset.</p> <p>RESETB is asynchronous input. If a signal with a specified low-level width is input to this pin independently of the operating clock, a system reset is effected, taking precedence over all the other operations.</p> <p>This signal can also be used to clear the power-saving mode (HALT or software STOP), as well as for normal initialization and starting.</p> <p>Caution RESETB is active-low.</p>	L	I	—									
HS_CLK	202	I	<p>Host clock.</p> <p>This pin inputs the clock that is to be supplied to the GPU core and internal peripheral I/O. This clock is input to the internal clock generator. An internal clock is generated according to the value of HCLKSEL and is supplied to the CPU core and internal peripheral I/O. Usually, input a clock of 27 MHz to this pin.</p>	—	I	—									
HCLKSEL	197	I	<p>Host clock selection.</p> <p>This pin inputs the clock that is to be supplied to the CPU core and internal peripheral I/O. The relationship between the clock supplied by the HS_CLK pin (27 MHz) and the clock supplied to the CPU core and internal peripheral I/O is as follows:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>HCLKSEL</th> <th>Internal clock frequency</th> <th>PLL operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>54 MHz</td> <td>Multiplied by 2</td> </tr> <tr> <td>1</td> <td>Clock stops.</td> <td>PLL operation stops</td> </tr> </tbody> </table>	HCLKSEL	Internal clock frequency	PLL operation	0	54 MHz	Multiplied by 2	1	Clock stops.	PLL operation stops	—	I	—
HCLKSEL	Internal clock frequency	PLL operation													
0	54 MHz	Multiplied by 2													
1	Clock stops.	PLL operation stops													

(9) Power supply, ground, and others

Pin Name	Pin No.	I/O	Function	Active	After Reset	Alternate Function
3.3V _{DD}	5, 31, 52, 63, 78, 95, 127, 140, 166, 187	—	<p>3.3 V power supply.</p> <p>Supplies a positive voltage of 3.3 V to the I/O pins of the 3.3 V interface.</p>	—	—	—
2.5V _{DD}	14, 67, 118, 170	—	<p>2.5 V power supply.</p> <p>Supplies a positive voltage of 2.5 V to the respective internal blocks.</p>	—	—	—
2.5GND	30, 91, 144, 195	—	<p>Ground.</p> <p>These are ground pins.</p> <p>Connect all GND pins to a common ground.</p>	—	—	—
3.3GND	9, 35, 56, 68, 82, 99, 131, 148, 173, 188	—				
PLLAV _{DD}	199	—	<p>Analog power supply to multiplication circuit.</p> <p>Supplies a positive analog voltage to the PLL. Supply 2.5 V to this pin.</p>	—	—	—
PLLAGND	200	—	<p>Analog ground for multiplication circuit.</p> <p>Analog ground pin for PLL.</p>	—	—	—
PLLDV _{DD}	198	—	<p>Digital power supply to multiplication circuit.</p> <p>Supplies a positive digital voltage to the PLL. Supply 2.5 V to this pin.</p>	—	—	—
PLLDGND	201	—	<p>Digital ground for multiplication circuit.</p> <p>Digital ground pin for PLL.</p>	—	—	—
IC(L)	203, 205 to 207	—	<p>Internally connected pins</p> <p>Directly connect these pins to ground.</p>	—	—	—
IFIROME	208	I	<p>Internal ROM/external ROM select input</p> <p>0: External ROM mode</p> <p>1: Internal ROM mode</p>	—	I	—

1.2 Connection of Unused Pins

The following table shows how to connect unused pins.

Table 1-1. Connection of Unused Pins (1/2)

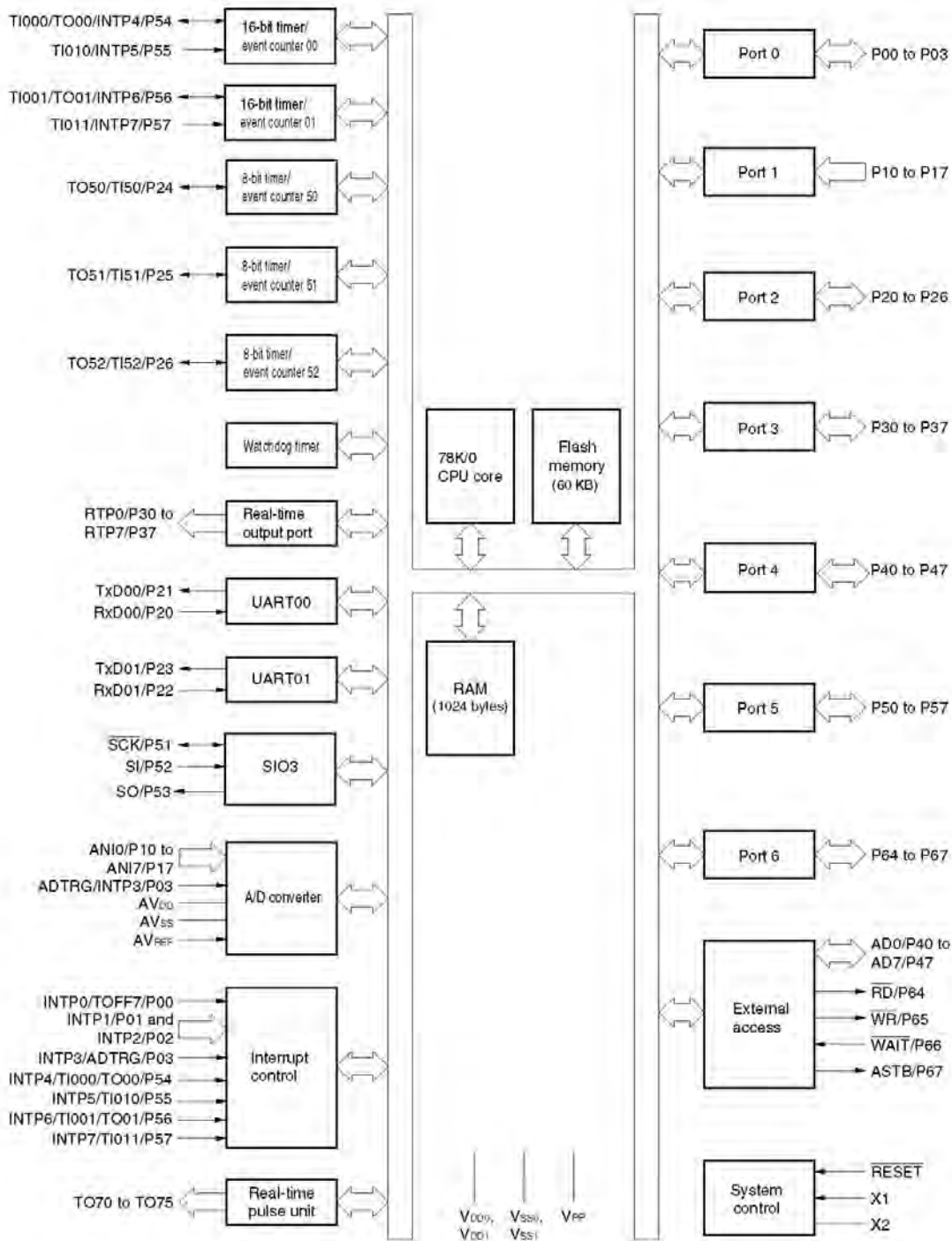
Pin Name	I/O	Interface	Recommended Connection of Unused Pin			
PHY_D[7:0]	I/O	I/O Buffer (LVTTTL) in 9 mA With Bus Holder	Connect these pins to V _{DD} or GND via a resistor.			
CTL[1:0]						
SCLK						
LREQ	O	3-state Output Buffer (LVTTTL) 9 mA	Leave open			
LPS	O	Output Buffer (LVTTTL) 9 mA				
LINKON	I	Input Buffer (LVTTTL)	Connect these pins to V _{DD} or GND via a resistor.			
STREAM1[7:0]	I/O	I/O Buffer (LVTTTL) 6 mA				
PACKETEN1						
TSERROR1						
TSRW1						
SYNC1						
STREAM2[7:0]						
PACKETEN2						
TSERROR2						
TSRW2						
SYNC2						
TSSUB1						
TSSUB2				O	Output Buffer (LVTTTL) 6 mA	Leave open
P3[4:0]				I/O	I/O Buffer (LVTTTL) Schmitt in 6 mA	Connect these pins to V _{DD} or GND via a resistor.
P40/SO						
P41/SI						
P42/SCK						
P43/TXD						
P44/RXD						
P45/SCS						
A[17:1]	O	I/O Buffer (LVTTTL) 6 mA				
RDZ	O	Output Buffer (LVTTTL) 6 mA	Leave open			
WRZ						
D[15:0]	I/O	I/O Buffer (LVTTTL) 6 mA	Connect these pins to V _{DD} or GND via a resistor.			
AD[10:1]	I	Input Buffer (LVTTTL)				
PSSSEL[1:0]						
CS						
RWZ						
IOR						
DMAACK/SIO_CNTI						

Table 1-1. Connection of Unused Pins (2/2)

Pin Name	I/O	Interface	Recommended Connection of Unused Pin
INT	O	Output Buffer (LVTTTL) 6 mA	Leave open
IOCHRDY			
DMAREQ/SIO_CNTO			
P_D[15:0]	I/O	I/O Buffer (LVTTTL) 9 mA	Connect these pins to V _{DD} or GND via a resistor.
IFIROME	I	Input Buffer (LVTTTL)	-
HS_CLK			
HCLKSEL			
RESETB	I	Output Buffer (LVTTTL) Schmitt	

IC7802: uPD78F0988A, DVIO Board, Control and Communication

BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 4-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	INTP0/TOFF7
P01				INTP1
P02				INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port	Input	ANI0 to ANI7
P20	I/O	Port 2 7-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RxD00
P21				TxD00
P22				RxD01
P23				TxD01
P24				T150/TO50
P25				T151/TO51
P26				T152/TO52
P30 to P37	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RTP0 to RTP7
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	AD0 to AD7
P50	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units. LEDs can be driven directly. Use of an on-chip pull-up resistor can be specified by software setting.	Input	—
P51				SCK
P52				SI
P53				SO
P54				INTP4/TI000/TO00
P55				INTP5/TI010
P56				INTP6/TI001/TO01
P57	INTP7/TI011			
P64	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting.	Input	RD
P65				WR
P66				WAIT
P67				ASTB

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function	
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00/TOFF7	
INTP1			Input	P01	
INTP2			Input	P02	
INTP3			Input	P03/ADTRG	
INTP4			Input	P54/TI000/TO00	
INTP5			Input	P55/TI010	
INTP6			Input	P56/TI001/TO01	
INTP7			Input	P57/TI011	
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P24/TO50	
TI51		External count clock input to 8-bit timer/event counter 51	Input	P25/TO51	
TI52		External count clock input to 8-bit timer/event counter 52	Input	P26/TO52	
TI000		External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000, CR010) of 16-bit timer/event counter 00	Input	P54/INTP4/TO00	
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00	Input	P55/INTP5	
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001, CR011) of 16-bit timer/event counter 01	Input	P56/INTP6/TO01	
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01	Input	P57/INTP7	
TO50		Output	8-bit timer/event counter 50 output	Input	P24/TI50
TO51			8-bit timer/event counter 51 output	Input	P25/TI51
TO52			8-bit timer/event counter 52 output	Input	P26/TI52
TO00			16-bit timer/event counter 00 output	Input	P54/INTP4/TI000
TO01	16-bit timer/event counter 01 output		Input	P56/INTP6/TI001	
RTP0 to RTP7	Output		Real-time output port that outputs pulses in synchronization with trigger signals outputs from the real-time pulse unit	Input	P30 to P37
TxD00	Output	Asynchronous serial interface serial data output	Input	P21	
TxD01			Input	P23	
RxD00	Input	Asynchronous serial interface serial data input	Input	P20	
RxD01			Input	P22	
SCK	I/O	Serial interface serial clock input/output	Input	P51	
SI	Input	Serial interface serial data input	Input	P52	
SO	Output	Serial interface serial data output	Input	P53	
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17	
ADTRG	Input	External trigger signal input to the A/D converter	Input	P03/INTP3	
TO70 to TO75	Output	Timer output for the 3-phase PWM inverter control	Hi-Z	-	
TOFF7	Input	Timer output (TO70 to TO75) stop external input	Input	P00/INTP0	
AD0 to AD7	I/O	Address/data bus for expanding memory externally	Input	P40 to P47	
RD	Output	Strobe signal output for reading from external memory	Input	P64	
WR		Strobe signal output for writing to external memory	Input	P65	
WAIT	Input	Wait insertion at external memory access	Input	P66	
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67	
AV _{REF}	Input	A/D converter reference voltage input	-	-	
AV _{DD}	-	A/D converter analog power supply	-	-	

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AV _{SS}	–	A/D converter ground potential	–	–
RESET	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2	–		–	–
V _{DD0}	–	Positive power supply for ports	–	–
V _{SS0}	–	Ground potential for ports	–	–
V _{DD1}	–	Positive power supply except for ports	–	–
V _{SS1}	–	Ground potential except for ports	–	–
V _{FP}	–	High-voltage application during program write/verify. In the normal operation mode, connect directly to V _{SS0} .	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

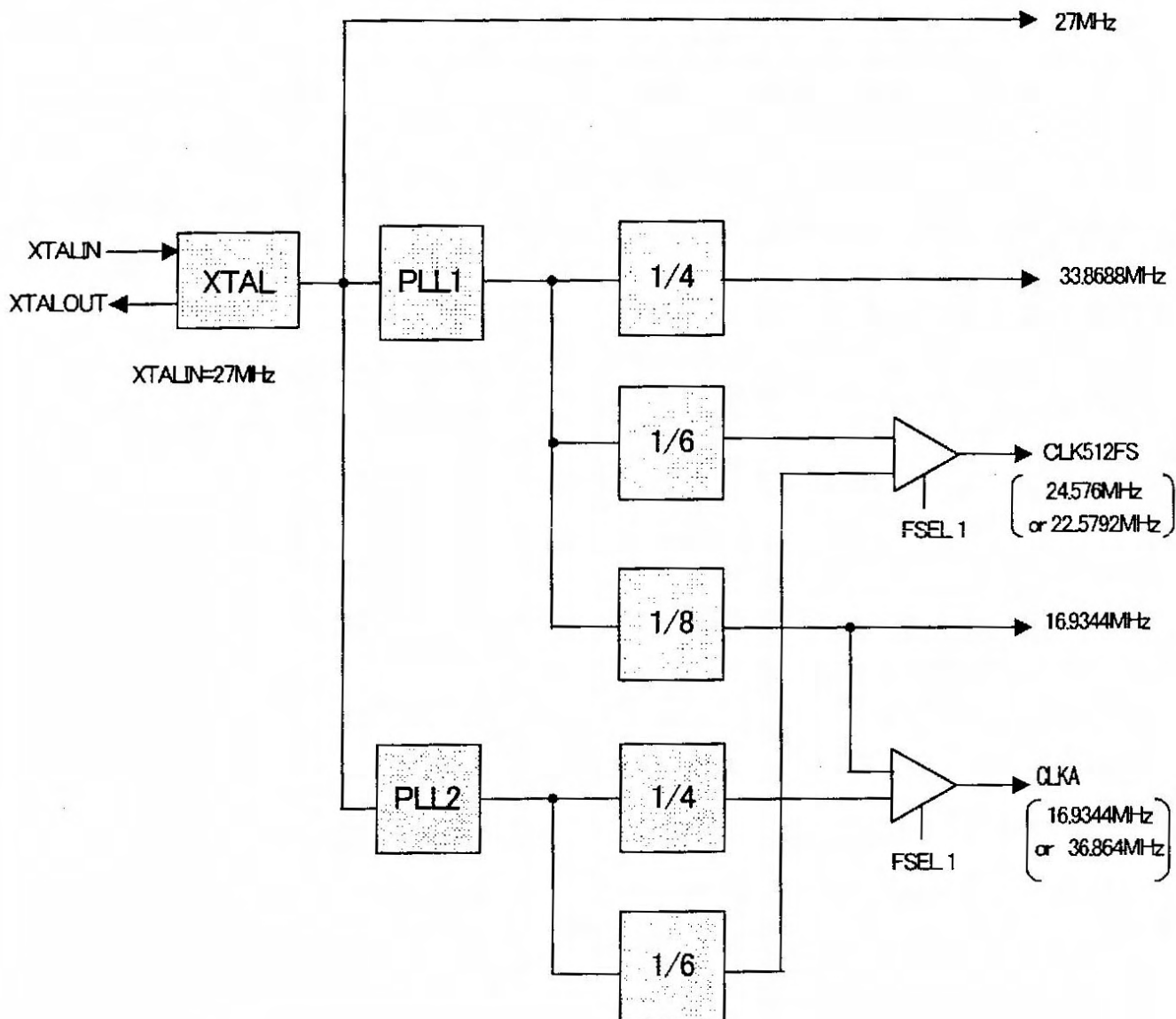
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins			
P00/INTP0/TOFF7	8-C	I/O	Input: Independently connect to V _{SS0} via a resistor. Output: Leave open.			
P01/INTP1						
P02/INTP2						
P03/INTP3/ADTRG						
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V _{DD0} or V _{SS0} via a resistor.			
P20/RxD00	8-C	I/O	Input: Independently connect to V _{DD0} or V _{SS0} via a resistor. Output: Leave open.			
P21/TxD00						
P22/RxD01						
P23/TxD01						
P24/TI50/TO50						
P25/TI51/TO51						
P26/TI52/TO52						
P30/RTP0 to P37/RTP7				5-H		
P40/AD0 to P47/AD7						
P50	8-C					
P51/SCK						
P52/SI						
P53/SO						
P54/INTP4/TI000/TO00						
P55/INTP5/TI010						
P56/INTP6/TI001/TO01						
P57/INTP7/TI011						
P64/RD						
P65/WR						
P66/WAIT						
P67/ASTB						
TO70 to TO75				4	Output	Leave open.
RESET				2	Input	–
AV _{DD}	–	–	Connect to V _{DD0} .			
AV _{REF}			Connect to V _{SS0} .			
AV _{SS}						
V _{FP}			Connect directly to V _{SS0} .			

IC7605: BU2288FV, DVIO Board, Clock Divider

Block Diagram

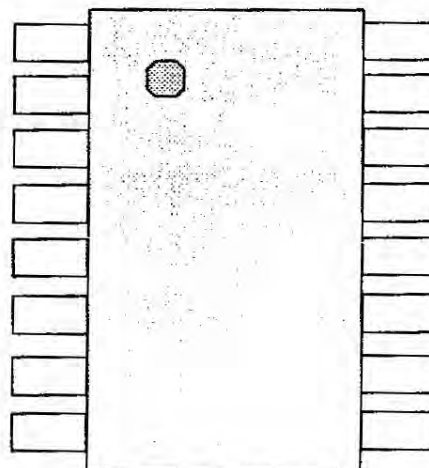


FSEL1	CLK512FS	CLKA
OPEN	22.5792MHz	16.9344MHz
L	24.576MHz	36.864MHz

Explanation for terminal function

PIN No.	PIN NAME	FUNCTION
1	VDD2	Digital VDD for 27MHz clock output
2	VSS2	Digital GND for 27MHz clock output
3	CLK27M	27MHz clock output
4	TEST	Output for test
5	AVDD	Analog VDD
6	AVSS	Analog GND
7	XTALOUT	Standard crystal output
8	XTALIN	Standard crystal input
9	CLKA	clock output (FSEL1=Open:16.9344MHz, FSEL1=L:36.864MHz)
10	CLK512FS	clock output (FSEL1=Open:22.5792MHz, FSEL1=L:24.576MHz)
11	DVSS	Digital GND
12	DVDD	Digital VDD
13	CLK16M	16.9344MHz clock output
14	FSEL1	Output select :with pull-up Open:16.9344MHz (9pin), 22.5792MHz (10pin) L :36.864MHz (9pin), 24.576MHz (10pin)
15	CLK33M	33.8688MHz clock output
16	OE	Output enable(open:enable, L:disable):with pull-up

1 : VDD2
2 : VSS2
3 : CLK27M
4 : TEST
5 : AVDD
6 : AVSS
7 : XTALOUT
8 : XTALIN



16 : OE
15 : CLK33M
14 : FSEL1
13 : CLK16M
12 : DVDD
11 : DVSS
10 : CLK512FS
9 : CLKA

IC7604: BA7082F, DVIO Board, PLL IC

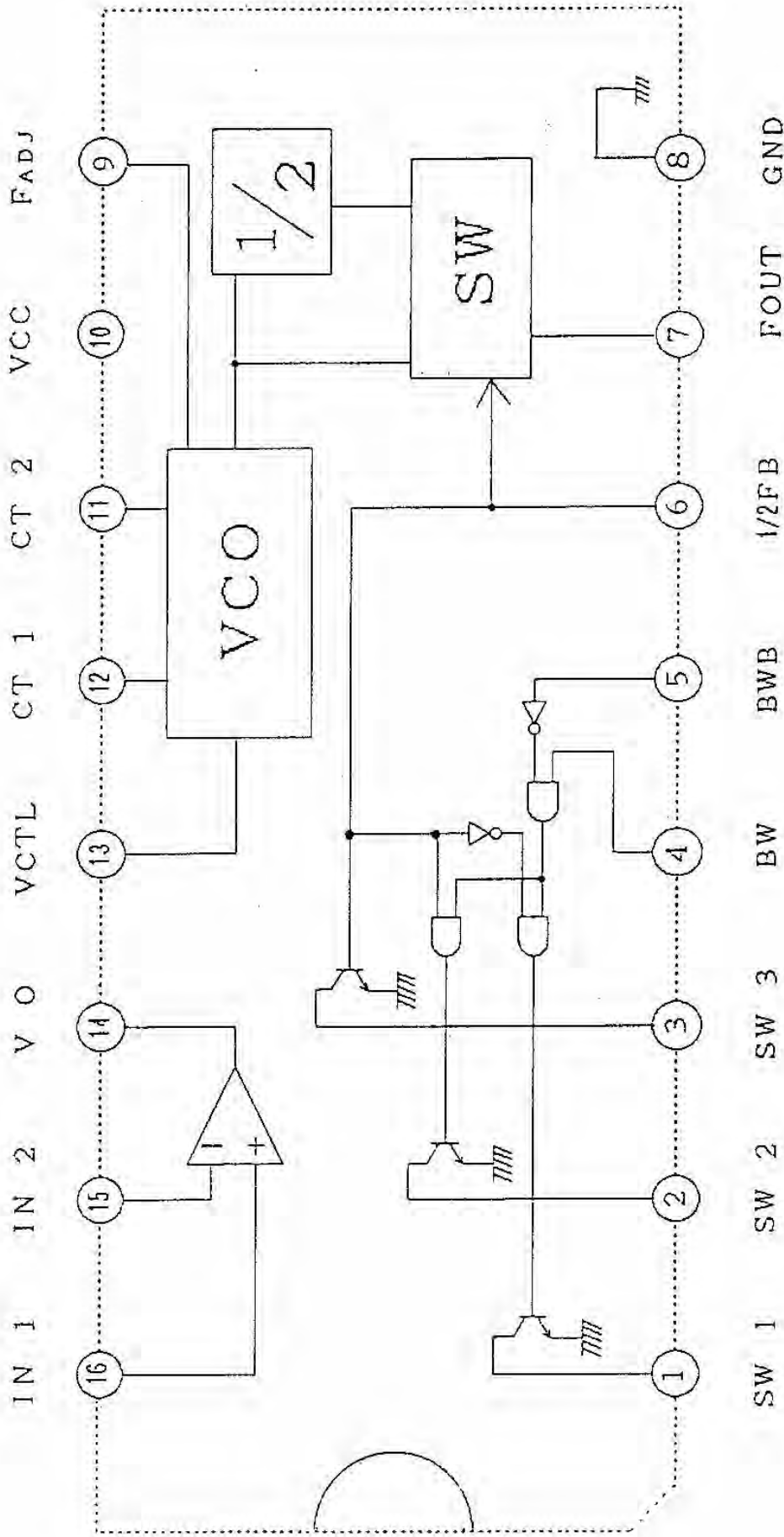
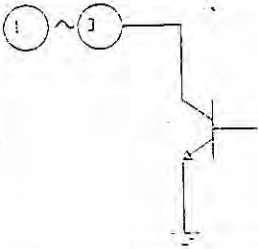
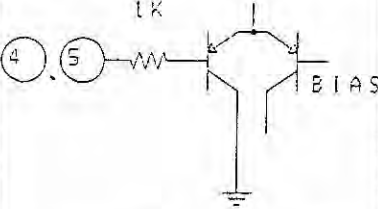
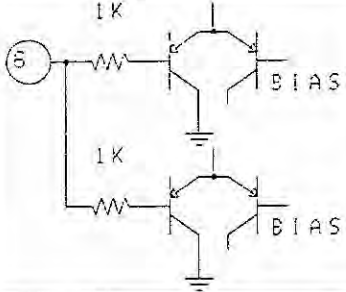
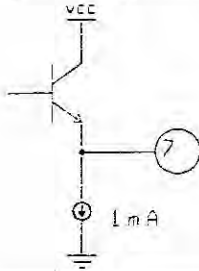
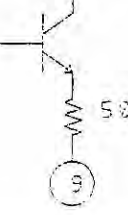
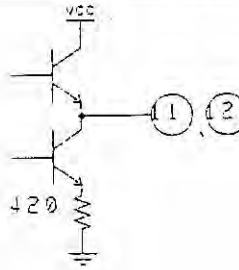
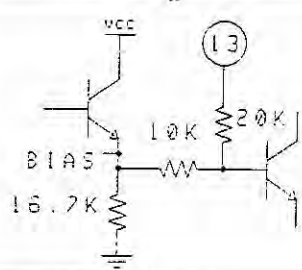
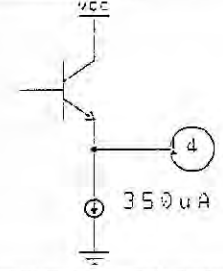
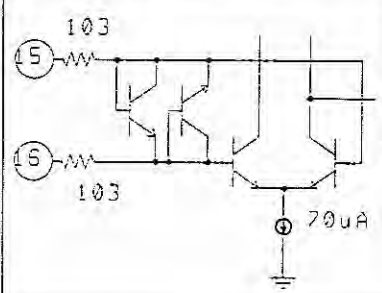


Fig-2 Block diagram

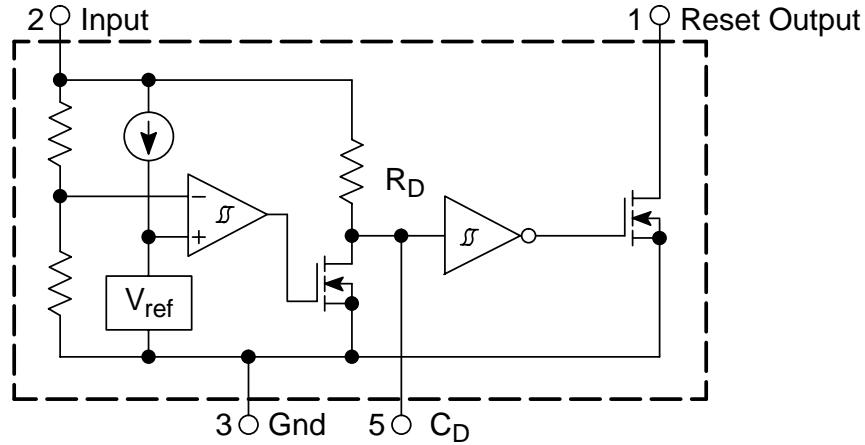
No.	Symbol	IN	OUT	normal DC Voltage	Internal pin configuration	Description
1	SW1			L 0.1V		Pin 1-3 are output pins at LOGIC parts for adjustment frequency sensitivity.
2	SW2		○	- OPEN 5V		These pins are open collector output.
3	SW3					
4	BW					Pin 4,5 are input pins at logic parts for adjustment frequency sensitivity.
5	BWB					
6	1/2FB	○		-		Pin 6 is input pin at LOGIC parts for adjustment frequency sensitivity and changing 1/2 Frequency demultiplier. "H" is through output. and "L" is 1/2 Frequency demultiplier output.
7	Fout		○	3.6V		VCO Output.
8	GND	-	-	0V	GND	GND
9	FADJ	-	-	2.5V		Pin9 is a pin to adjust f0. It is possible to adjust f0 by added resistor (RADJ). If Value of RADJ down, oscillation frequency up. (Use to RADJ > 22kΩ).

No.	Symbol	IN	OUT	normal DC Volt tag	Internal pin configuration	Description
10	VCC	—	—	5.0V	VCC	VCC
11	CT2	—	—	1.9V		<p>Pin 11,12 are added capacitor pins for oscillation. Use to added capacitor between CT1 and CT2. If value of capacitor down, oscillation frequency up.</p>
12	CT1					
13	VCTL	○		2.5V		<p>Pin13 is control pin for VCO. A regular this pin connect pin14(V0).</p>
14	V0		○	2.5V		<p>Pin14 is output pin at Amplifier for sencitivity adjustment. Adjustment amplifier GAIN by added resistor.</p>
15	IN2	○		2.5V		<p>Pin15,16 are input pins at amplifier for sencitivity adjustment. In1 ; normal input In2 ; inversion input</p>
16	IN1					

9.12.5 ICs Digital Board Chrysalis

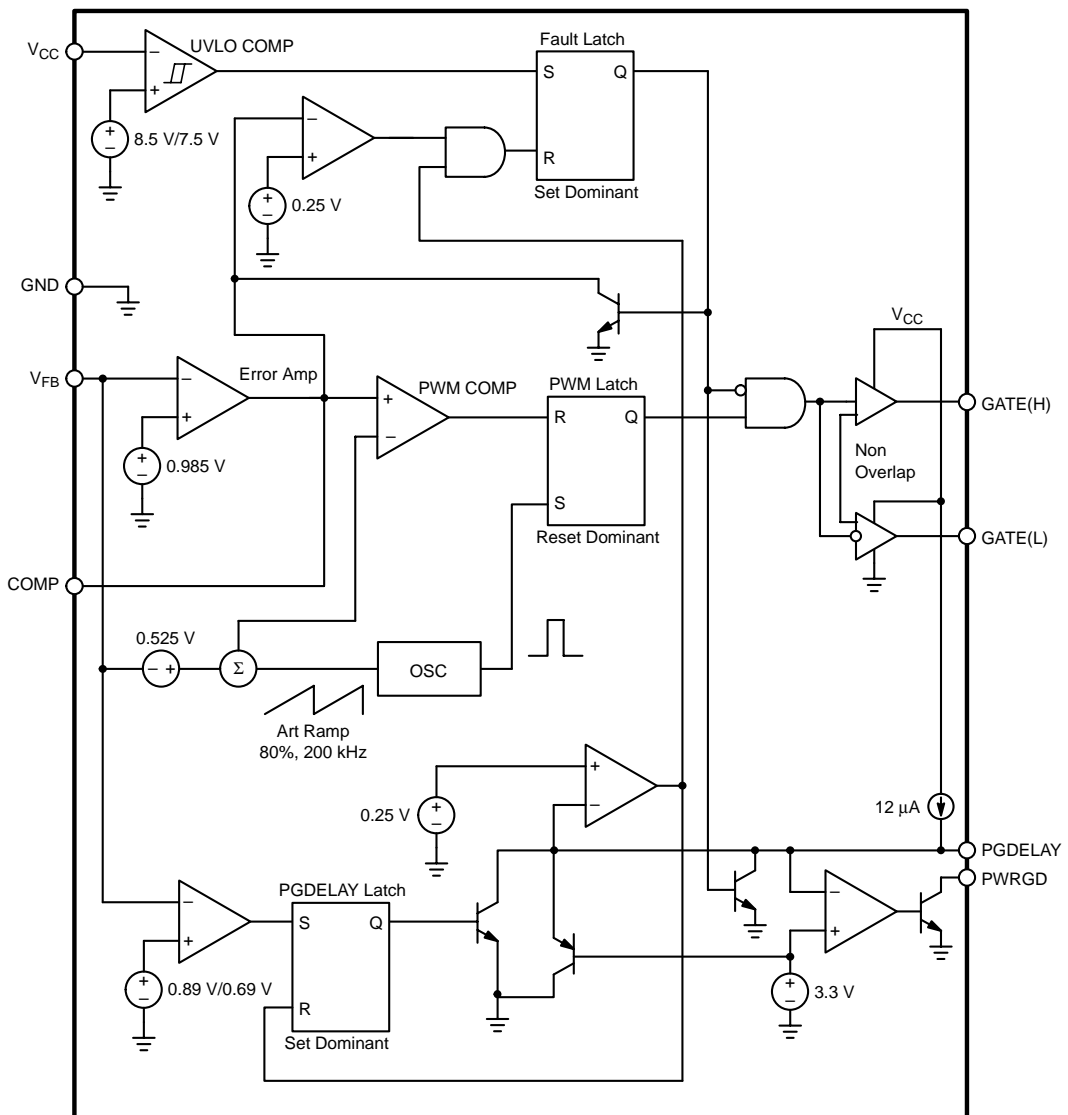
IC7106 NCP303LSN29, Digital Board 2.1 Chrysalis, Reset Circuit

NCP303LSNxxT1
Open Drain Output Configuration



IC7501 NCP1570D, Digital Board 2.1 Chrysalis, DC/DC Converter Control

NCP1570

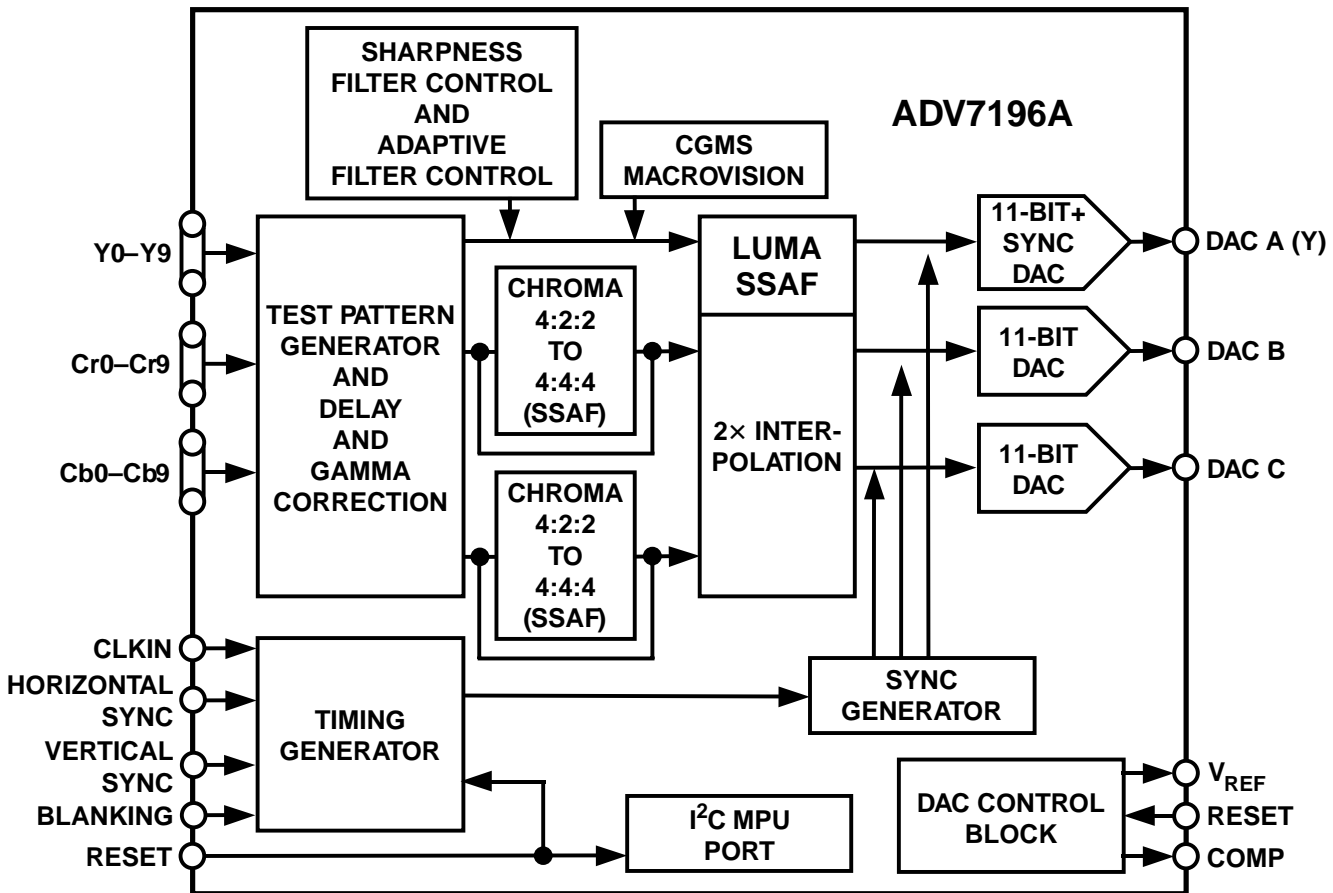


PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
SO-8		
1	V _{CC}	Power supply input.
2	PWRGD	Open collector output goes low when V _{FB} is out of regulation. User must externally limit current into this pin to less than 20 mA.
3	PGDELAY	External capacitor programs PWRGD low-to-high transition delay.
4	COMP	Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft Start. Pulling pin < 0.45 locks gate outputs to a zero percent duty cycle state.
5	GATE(H)	High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A.
6	GATE(L)	Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A.
7	V _{FB}	Error amplifier and PWM comparator input.
8	GND	Power supply return.

IC7703 ADV7196A, Digital Board 2.1 Chrysalis, Progressive Scan Video Encoder

FUNCTIONAL BLOCK DIAGRAM



ADV7196A

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Input/Output	Function
1, 12	V _{DD}	P	Digital Power Supply
2–11	Y0–Y9	I	10-Bit Progressive Scan/HDTV Input Port for Y Data. Input for G data when RGB data is input.
13, 52	GND	G	Digital Ground
14–23	Cr0–Cr9	I	10-Bit Progressive Scan/HDTV Input Port for Color Data in 4:4:4 Input Mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.
24, 35	V _{AA}	P	Analog Power Supply
25	CLKIN	I	Pixel Clock Input. Requires a 27 MHz reference clock for standard operation in Progressive Scan Mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode.
26, 33	AGND	G	Analog Ground
27	DV	I	Video Blanking Control Signal Input
28	$\overline{\text{VSYNC}}$ / TSYNC	I	$\overline{\text{VSYNC}}$, Vertical Sync Control Signal Input or TSYNC Input Control Signal in Async Timing Mode
29	$\overline{\text{HSYNC}}$ / SYNC	I	$\overline{\text{HSYNC}}$, Horizontal Sync Control Signal Input or $\overline{\text{SYNC}}$ Input Control Signal in Async Timing Mode
30	SCL	I	MPU Port Serial Interface Clock Input
31	SDA	I/O	MPU Port Serial Data Input/Output
32	DAC C	O	Color Component Analog Output of Input Data on Cb/Cr9–0 Input Pins
34	DAC A	O	Y Analog Output
36	DAC B	O	Color Component Analog Output of Input Data on Cr9–Cr0 Input Pins
37	COMP	O	Compensation Pin for DACs. Connect 0.1 μF capacitor from COMP pin to V _{AA} .
38	R _{SET}	I	A 2470 Ω resistor (for input ranges 64–940 and 64–960; output standards EIA-770.1–EIA-770.3) must be connected from this pin to ground and is used to control the amplitudes of the DAC outputs. For input ranges 0–1023 (output standards RS-170, RS-343A) the R _{SET} value must be 2820 Ω .
39	V _{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V)
40	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7196A into Default Register setting. Reset is an active low signal.
41	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high, the $\overset{\circ}{\text{I}}\text{C}$ filter is activated which reduces noise on the $\overset{\circ}{\text{I}}\text{C}$ interface. When this pin is tied low, the input bandwidth on the $\overset{\circ}{\text{I}}\text{C}$ interface is increased.
42–51	Cb/Cr9–0	I	10-Bit Progressive Scan/HDTV Input Port for Color Data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.

9.13 List of Abbreviations

Analog Board

+5VSTBY	Permanent Supply 5V
8SC2	Pin8 Scart2 (only for Europe)
A_DATA	Data from Analog- to Digital-Board (UART-Communication)
A_RDY	Analog-board ready (status information to digital-board)
A18 - A19	Parallel Address Bus (CC - Flash-ROM and S-RAM)
A8 - A17	Parallel Address Bus (CC - Flash-ROM and S-RAM)
AD0 - AD7	Parallel Address and Data Bus (CC - Flash-ROM and S-RAM)
AFC	Automatic Frequency Control
AFEL	Audio Frontend Left
AFER	Audio Frontend Right
AGC / WSRI	Automatic Gain Control (for Europe), Wide Screen Rear In (for NTSC)
AINFL	Audio In Front Left
AINFR	Audio In Front Right
AKILL	Audio Kill Signal
ALADC	Audio Left to ADC
ALDAC	Audio Left from DAC
ALE	Address Latch Enable

AM0	Address-mode 0
AM1	Address-mode 1
ARADC	Audio Right to ADC
ARDAC	Audio Right from DAC
ASCC1M	Audio Scart 1 Mute (System Clock Output for Real time Clock-Adjustment)
AVCC	Power Supply for A/D-converter
AVSS	GND-Pin for A/D-converter
CFIN	Chroma Front In
CS0	Chip Select 0 (CC - S-RAM)
CS2	Chip Select 2 (CC - Flash-ROM)
CVBSFIN	Video Front In
D_DATA	Data from Digital- to Analog-Board (UART-Communication)
D_RDY	Digital-board ready (status information from digital-board)
DAC_MUTE	Mute Signal for DAC
DAOUT	Digital Audio Out
DVAL	Audio from Digital Video In Left
DVAR	Audio from Digital Video In Right
DVCC1	Power Supply Pin
DVCC2	Power Supply Pin
DVCC3	Power Supply Pin
DVSS1	GND Pin
DVSS2	GND Pin
DVSS3	GND Pin
FAN_OFF	Fan for Basic engine

FBIN	Fast Blanking input	5508_ODD_EVEN	Odd - Even control from Host Decoder to Progressive Scan
FOME	FOLLOW ME Status line (matching signals yes/no; only for Europe)	-5V	-5V Power Supply
G1...10	DISPLAY GRID	-5V_BUFFER	-5V Power Supply for Video Filters
INT	Interrupt OUT for the CC	A_EMPRESS(13:0).....	EMPRESS address output to SDRAM
INT	Interrupt – line from Display Print	ACC_ACLK_OSC	Audio Clock PLL output sync with incoming video for record
ION	Inverse ON-Line	ACC_ACLK_PLL.....	Audio Clock PLL output for play back
IPFAIL	Inverse Power Fail Detection	ACLK_EMP	EMPRESS audio clock output
IPOR.....	Inverse Power On Reset	AD_ACLK.....	Audio Decoder Clock
IRESET	Inverse Reset Input	AD_BCLK.....	Audio Decoder I2S bit clock
IRR	Signal from IR-Receiver	AD_DATAO.....	Audio Decoder Output data (PCM)
K1	Key-Input-Line	AD_SPDIF33	Audio digital output to the analog board
K2	Key-Input-Line	AD_WCLK.....	Audio Decoder I2S word clock
KILL	Audio Mute	AE_ACLK.....	Audio Encoder Clock
P50 IN	P50 INput-line (only for Europe)	AE_ACLK_OEN	Audio Encoder Clock Output Enable
P50 OUT	P50 OUTput-line (only for Europe)	AE_BCLK.....	Audio Encoder I2S bit clock
POR_DC	Power On Reset for Display Control Print (Ext_DL)	AE_BCLK_DV.....	Audio Encoder I2S bit clock to DVIO
PSS	Pal/Secam-Select	AE_BCLK_VSM.....	Audio Encoder I2S bit clock to VSM
PWM_FIL	Control line for Filament Voltage Generation	AE_DATAI.....	Audio Encoder Input data (PCM)
PWONSW	Amplifier Switch Audio A/D Converter	AE_DATAI_DV.....	Audio Encoder Input data (PCM) from DVIO
RD	Output Enable Read (CC - Flash-ROM and S-RAM)	AE_DATAO.....	Audio Encoder Output data (PCM)
RECLED.....	Control Signal for REC-LED	AE_WCLK.....	Audio Encoder I2S word clock
RESET_DIG	Reset Line to Digital Board	AE_WCLK_DV	Audio Encoder I2S word clock to DVIO
RP_	Inverse Reset line to Flash-ROM	AE_WCLK_VSM.....	Audio Encoder I2S word clock to VSM
RSA1/2.....	Record Selector 1/2	ANA_WE.....	Analogue write enable
RY/BY.....	Ready/Busy – input line (from Flash-ROM)	ANA_WE_LV	Analogue write enable Low Voltage
SIF1.....	Sound intermediate frequency	B_IN_VIP	Video blue input to Video Input Processor
SB1.....	Secam Band 1 (PCB-Test entrance)	B_OUT	Video blue output from Host Decoder
SCL	I ² C-Bus	B_OUT_B.....	Filtered blue video output
SCLSW.....	Switched I ² C-Bus	BA	Bank Address
SDA	I ² C-Bus	BCLK_CTL_SERVICE	Bitclock control Service Interface
SDASW	Switched I ² C-Bus	BE_BCLK.....	Basic Engine I2S bit clock
SFS_TS.....	SAW Filter Select Trap Select	BE_BCLK_VSM.....	Basic Engine I2S bit clock to VSM
STBY	Standby-Line (Flash_Toshiba)	BE_CPR.....	Basic Engine Control Processor ready to accept data
SYNC	Video Sync input	BE_DATA_RD	Basic Engine Data read
TEMP_SENSE	Temperature Sense Line	BE_DATA_WR.....	Basic Engine Data write
VER	HW-version input	BE_FAN	Basic Engine FAN
VFV	Video from Frontend	BE_FLAG	Basic Engine error flag
VKK	VFT Driver Power Supply	BE_IRQN	Basic Engine interrupt request
VREFH.....	Pin for Reference-voltage input to A/D-converter	BE_LOADN.....	Basic Engine LOAD(LOW active)
VREFL.....	Pin for Reference-voltage input to A/D-converter	BE_RXD.....	Basic Engine S2B received data
VS1/2.....	View Selector 1/2	BE_SUR.....	Basic Engine servo unit ready to accept data (S2B)
WR_	Write Enable (CC - Flash-ROM and S-RAM)	BE_SYNC	Basic Engine sector/abs time sync
WSFI	Wide Screen Signalling Front In	BE_TXD	Basic Engine S2B transmitted data
WU	Wake Up	BE_V4.....	Basic Engine versatile input pin
X1	Oscillator Pin	BE_WCLK.....	Basic Engine I2S word clock
X2	Oscillator Pin	C_IN.....	Video Chrominance input
XIN	Oscillator Pin	C_IN_VIP	Chrominance input to Video Input Processor
XOUT	Oscillator Pin	C_OUT.....	Chrominance output from Host Decoder
XT1.....	Low Frequency Oscillator Pin	C_OUT_B	Filtered Chrominance output
XT2.....	Low Frequency Oscillator Pin	CAS.....	Column Address strobe
YFIN	Luminance Front In	CB_OUT(9:0).....	Chrominance Blue out
		CLK4.....	SDRAM clock
		CPUINT0.....	Control processor unit interrupt
		CPUINT1.....	Control processor unit interrupt
		CR_OUT(9:0).....	Chrominance Red out
		CTS1P	Clear to send (Service Interface)
		CVBS_OUT.....	Composite video output out of the Host Decoder
		CVBS_OUT_B	Filtered Composite video output
		CVBS_OUT_B_VIP	Composite video output to Video Input Processor(digital board video loop)
		CVBS_Y_IN	Composite video/Luminance input
		CVBS_Y_IN_A.....	Composite video/Luminance input to Video Input Processor
		CVBS_Y_IN_B.....	Composite video/Luminance input to Video Input Processor

Digital Board

+12V	+12V Power Supply
+2V5_FLI.....	+2V5 Power Supply for FLI
+2V5_PLL	+2V5 Power Supply for PLL
+3V3	+3V3 Power Supply
+3V3_ANA	+3V3 Power Supply Analogue
+3V3_DD.....	+3V3 Power Supply Digital
+3V3_FLI.....	+3V3 Power Supply for FLI
+5V	+5V Power Supply
+5V_BUFFER	+5V Power Supply for Video Filters
5508_HS	Horizontal Synchronisation from Host Decoder to Progressive Scan

CVBS_Y_IN_C.....	Composite video/Luminance input to Video Input Processor	JTAG3_TRSTN.....	JTAG Test part ResetN
D_ADDR(10:0).....	Address bus	LOAD_DVN.....	LOAD Digital Video(LOW active)
D_DATA(29:0).....	Data bus	MUTEN.....	Mute enable
D_EMPRESS(15:0).....	SDRAM data input/output of EMPRESS	MUTEN_LV.....	Mute enable Low Voltage
D_PAR_D(7:0).....	Front-end parallel interface data (record)	P_SCAN_YUV(7:0).....	Progressive Scan digital video bus
D_PAR_DVALID.....	Front-end parallel interface data valid	R_IN_VIP.....	Video Red input to Video Input Processor
D_PAR_REQ.....	Front-end parallel interface request	R_OUT.....	Video Red output from Host Decoder
D_PAR_STR.....	Front-end parallel interface strobe	R_OUT_B.....	Filtered Red Video output from Host Decoder
D_PAR_SYNC.....	Front-end parallel interface sync	RAS.....	Row Address Strobe
DV_IN_CLK.....	Digital Video in clock from DVIO board	RESETN.....	Reset Host Decoder
DV_IN_DATA(7:0).....	Digital Video in data bus from DVIO board	RESETN_BE.....	System reset basic engine (buffered)
DV_IN_HS.....	Digital Video in horizontal synchronisation from DVIO board	RESETN_DVIO.....	System reset Digital Video Input Output (buffered)
DV_IN_VS.....	Digital Video in vertical synchronisation from DVIO board	RESETN_VE.....	System reset Video Encoder
EMI_A(21:1).....	External Memory Interface Address Bus(Host Decoder)	ROMH_CEN.....	Flash 2 chip enable
EMI_BE0N.....	External Memory Interface Lower byte enable(Host Decoder)	ROML_CEN.....	Flash 1 chip enable
EMI_BE1N.....	External Memory Interface Upper byte enable(Host Decoder)	RSTN_BE.....	Reset control of basic engine
EMI_CAS0N.....	External Memory Interface SDRAM column address strobe(Host Decoder)	RSTN_DVIO.....	Reset control of DVIO
EMI_CE1N.....	External Memory Interface VSM Lower bank enable	RTS1P.....	Ready To Send data to service serial interface
EMI_CE2N.....	External Memory Interface VSM Higher bank enable	RX1P.....	Receive data from service serial interface
EMI_CE3N.....	External Memory Interface flash IC's enable	SCL.....	I2C bus clock
EMI_D(15:0).....	External Memory Interface Data Bus(Host Decoder)	SD_CASN.....	SDRAMColumn Address strobe output (active LOW)
EMI_PROCCLK.....	External Memory Interface Processor Clock(Host Decoder)	SD_CLK.....	SDRAMclock output
EMI_RWN.....	External Memory Interface Read/Write control signal(Host Decoder)	SD_CLKE.....	SDRAMclock enable output
EMI_WAIT.....	External Memory Interface Wait state request(Host Decoder)	SD_CSN.....	SDRAM
EMPRESS_BOOT.....	EMPRESS BOOT select input	SD_DQM(1:0).....	SDRAMdata mask enable output
EMPRESS_IRQN.....	EMPRESS Interrupt request output	SD_RASN.....	SDRAMrow address strobe output
FLASH_OEN.....	FLASH output enable control signal	SD_WEN.....	SDRAMwrite enable output
G_IN_VIP.....	Video green input to Video Input Processor	SDA.....	I2C bus dataSEL_ACLK1Select audio clock(playback)
G_OUT.....	Video green output from Host Decoder	SM_CS3N.....	SRAMchip select
G_OUT_B.....	Filtered green video output from Host Decoder	SM_LBN.....	SRAMlower bank
GNDD.....	Digital Ground	SM_OEN.....	SRAMoutput enable
HD_M_AD(13:0).....	Host Decoder SDRAM address bus	SM_UBN.....	SRAMupper bank
HD_M_CASN.....	Host Decoder SDRAM column address strobe	SM_WEN.....	SRAMwrite enable
HD_M_CLK.....	Host Decoder SDRAM clock	SMA(17:0).....	SRAMaddress output
HD_M_CSON.....	Host Decoder SDRAM chip select	SMD(15:0)SRAM.....	data input/output
HD_M_DQ(15:0).....	Host Decoder SDRAM data bus	SYCLK_EMPRESS...	System clock EMPRESS
HD_M_DQML.....	Host Decoder SDRAM data mask enable(Lower)	SYCLK_PROGSCAN	System clock Progressive Scan
HD_M_DQMU.....	Host Decoder SDRAM data mask enable(Upper)	SYCLK_VSM_5508...	System clock VSM and Host decoder
HD_M_RASN.....	Host Decoder SDRAM row address strobe	TX1P.....	Transmit data to service serial interface
HD_M_WEN.....	Host Decoder SDRAM write enable	U_IN.....	Video U input
HSOUT.....	Horizontal synchronisation OUT	U_IN_VIP.....	Video U input to Video Input Processor
ION.....	Inverted ON: Enable the power supply for the digital board when LOW	V_IN.....	Video V input
IRESET_DIG.....	Initialisation of the digital board, HIGH when power ON	V_IN_VIP.....	Video V input to Video Input Processor
JTAG3_TCK.....	JTAG Test Clock	VCC3_CLK_BUF.....	Power supply 3V3 clock buffer
JTAG3_TD_VIP_TO_VE	JTAG Transmitted Data Video Input Processor to Video Encoder	VCC3_VSM.....	Power supply 3V3 Versatile Stream Manager
JTAG3_TD_VSM_TO_VIP	JTAG Transmitted Data Versatile Stream Manager to Video Input Processor	VCC3_VSM_MEM.....	Power supply 3V3 Versatile Stream Manager Memory
JTAG3_TMS.....	JTAG Test Mode Select	VCC5_4046.....	Power supply 5V to PLL IC
		VDD_125.....	Power supply 5V to buffer 7202
		VDD_CORE.....	Sti5508 Core supply voltage 2.5V
		VDD_EMP.....	Empress supply voltage 3.3V
		VDD_EMP_CORE.....	Empress Core supply voltage 2.5V
		VDD_FLASH_H.....	Flash 7301 supply voltage
		VDD_FLASH_L.....	Flash 7302 supply voltage
		VDD_LVC32.....	Power supply LVC32
		VDD_PCM.....	Power supply Audio decoder of Sti5508
		VDD_PLL.....	Power supply PLL audio decoder of Sti5508
		VDD_RGB.....	Power supply video encoder of Sti5508
		VDD_STI.....	Power supply of Sti5508
		VDD_YCC.....	Power supply video encoder of Sti5508
		VDD5_MK2703.....	Power supply MK2703
		VDD5_OSC.....	Power supply Oscillator

VDDA1A_7118	Power supply for analog input of VIP
VDDA2A_7118	Power supply for analog input of VIP
VDDA3A_7118	Power supply for analog input of VIP
VDDA4A_7118	Power supply for analog input of VIP
VDDE_7118	Power supply digital for peripheral cells of VIP
VDDI_7118	Power supply digital for core of VIP
VDDX_7118	Power supply for crystal oscillator of VIP
VE_DATA(7:0)	Video Encoder data Bus
VE_DSN	Video Encoder Data Strobe
VE_DTACKN	Video Encoder Data Transfer acknowledge
VIP_ERROR	Video Input Processor error
VIP_FB	Video Input Processor Fast Blanking
VIP_FID_FF	Video Input Processor field identifier to Flip Flop
VIP_HS	Video Input Processor horizontal synchronisation
VIP_ICLK	Video Input Processor input Clock
VIP_IDQ	Video Input Processor output data qualifier
VIP_IGP1	Video Input Processor input general purpose 1
VIP_INT	Video Input Processor interrupt
VIP_RTS1	Video Input Processor ready to send
VIP_VS	Video Input Processor vertical synchronisation
VIP_YUV(7:0)	Video Input Processor digital video(CCIR 656)
VS_IN	Vertical synchronisation IN
VSM_M_A(13:0)	Versatile Stream Manager SDRAM address bus
VSM_M_CASN	Versatile Stream Manager SDRAM column address strobe
VSM_M_CLKEN	Versatile Stream Manager SDRAM clock enable
VSM_M_CLKOUT	Versatile Stream Manager SDRAM clock out
VSM_M_D(15:0)	Versatile Stream Manager SDRAM data bus
VSM_M_LDQM	Versatile Stream Manager SDRAM lower data mask enable
VSM_M_RASN	Versatile Stream Manager SDRAM row address strobe
VSM_M_UDQM	Versatile Stream Manager SDRAM upper data mask enable
VSM_M_WEN	Versatile Stream Manager SDRAM write enable
VSM_UART1_CTSN	Versatile Stream Manager UART1 clear to send to analog board (UART1 is gateway to analog board)
VSM_UART1_RTSN	Versatile Stream Manager UART2 clear to send to DVIO board (UART2 is gateway to DVIO board)
VSM_UART1_RX	Versatile Stream Manager UART1 ready to send to analog board
VSM_UART1_TX	Versatile Stream Manager UART2 ready to send to DVIO board
VSM_UART2_CTSN	Versatile Stream Manager UART1 received data to analog board
VSM_UART2_RTSN	Versatile Stream Manager UART2 received data to DVIO board
VSM_UART2_RX	Versatile Stream Manager UART1 transmitted data to analog board
VSM_UART2_TX	Versatile Stream Manager UART2 transmitted data to DVIO board
VSOUT	Vertical synchronisation OUT
WE	Write Enable
Y_IN	Luminance input from analog board
Y_OUT	Luminance output from Host Decoder
Y_OUT_B	Filtered luminance output
YY_OUT(9:0)	Luminance output from FLI

Digital Board Chrysalis

ADC	:Analog to Digital Converter
DAC	:Digital to Analog Converter
DENC	:Digital (Video) Encoder (Video DAC)
DV	: Digital Video (Camcorder)
EF	: Emitter Follower
OSD	:On-Screen Display
VIP	:Video Input Processor (Video ADC)
2Fh	: Progressive scan video
2V5	+2V5 Power supply for Link+Codec IC7431
3V3	+3V3 Power supply
3V3_A	+3V3 Analog power supply for PHY IC7400
3V3_D	+3V3 Digital power supply for PHY IC7400
3V3_DLY	+3V3 Power supply for IC7500
3V3_LINK	+3V3 Power supply for Link+Codec IC7431
3V3_F	+3V3 Power supply for optional Flash memory IC7432
3V3_RAM	+3V3 Power supply for SDRAM IC7430
3V3_uP	+3V3 Power supply for Micro-controller IC7802
3V3_32kHz	+3V3 Power supply for audio format adaptation circuitry IC7507 and IC7508
3V3_AC	+3V3 Power supply for audio system clock generator IC7605 and IC7606
+5V	+5V Power supply
5V_PLL	+5V Power supply for VCO of audio PLL IC7604
A (1:17)	Flash address lines of uPD72893
A_MUTE	Audio Mute
ABCK	Audio Bit Clock
AD (1:10)	Address bus lines for Host I/F of Link+Codec IC7431
AEMP1	PCM1 emphasis ON/OFF for PCM1 output
AFS1	Audio sampling frequency indication signal
ALRCLK	Audio Word Select
AMCLK44	11.2896MHz (=256 * 44.1 kHz) audio master clock signal for 44.1 kHz audio
AMCLK48	12.288MHz (=256 * 48 kHz) audio master clock signal for 32 kHz and 48 kHz audio
APWM	PWM signal for audio PLL
ASIC	Application Specific Integrated Circuit
BUFENn_AUD	Buffer Enable Audio
BUFENn_VID	Buffer Enable Video
CLK27M_CON	27MHz Clock to Digital Board
CS	Parallel interface chip select input of Link+Codec IC7431
CTL (0:1)	Link interface control lines
CTSN	Clear to Send
D (0:15)	Flash data lines of Link+Codec IC7431
DCDi	Directional Correlational Deinterlacing. Circuitry that reduces jaggies on diagonal edges when deinterlacing video-sourced material.
DV_STATUS	Interrupt pin for reading DV-status
HS_CLK	Video clock input of Link+Codec IC7431
INT	Interrupt request output of Link+Codec IC7431 (input to Micro-Controller)
IOR	Parallel interface IO read control input of Link+Codec IC7431
ISPN	In System Programming signal (used for programming IC7802)

LKON	Link-on signal output
LPS	Link power status input
LREQ	Link request input
MA (0:10)	SDRAM address lines of Link+Codec IC7431
MCAS	SDRAM column address strobe signal
MCLK	SDRAM clock signal
MD (0:15)	SDRAM data lines of Link+Codec IC7431
MRAS	SDRAM row-address strobe signal
MWE	SDRAM write enable signal
PCM1	Audio Serial Data Output of Link+Codec IC7431
PCM1_NEW	'MSB justified' to I2S converted audio serial data; audio serial data input of audio DAC UDA1334A
PD (0:15)	Data bus lines for Host I/F of Link+Codec IC7431
PHY_D (0:7)	Data bus connection between PHY and LINK device
RESETn	DVIO board reset
RESET_FM	Reset signal driven by Flashmaster programming device
RESTB	Reset input of Link+Codec IC7431
RTSN	Request to Send
RWZ	Parallel interface read/write control input of Link+Codec IC7431
RXD	Receive Data
SCLK	Link control output clock
TXD	Transmit Data
VPP	+10V switchable programming voltage of microcontroller
YUV (0:7)	Digital Video

Divio 1.8 Board

2V5	+2V5 Power supply for Link+Codec IC7431
3V3	+3V3 Power supply
3V3_A	+3V3 Analog power supply for PHY IC7400
3V3_D	+3V3 Digital power supply for PHY IC7400
3V3_DLY	+3V3 Power supply for IC7500
3V3_LINK	+3V3 Power supply for Link+Codec IC7431
3V3_F	+3V3 Power supply for optional Flash memory IC7432
3V3_RAM	+3V3 Power supply for SDRAM IC7430
3V3_uP	+3V3 Power supply for Micro-controller IC7802
3V3_32kHz	+3V3 Power supply for audio format adaptation circuitry IC7507 & IC7508
3V3_AC	+3V3 Power supply for audio system clock generator IC7605 & IC7606
+5V	+5V Power supply
5V_PLL	+5V Power supply for VCO of audio PLL IC7604
A(1:17)	Flash address lines of uPD72893
A_MUTE	Audio Mute
ABCK	Audio Bit Clock
AD(1:10)	Address bus lines for Host I/F of Link+Codec IC7431
AEMP1	PCM1 emphasis ON/OFF for PCM1 output
AFS1	Audio sampling frequency indication signal
ALRCLK	Audio Word Select
AMCLK44	11,2896MHz (=256*44.1kHz) audio master clock signal for 44.1kHz audio
AMCLK48	12,288MHz (=256*48kHz) audio master clock signal for 32kHz and 48kHz audio

APWM	PWM signal for audio PLL
BUFENn_AUD	Buffer Enable Audio
BUFENn_VID	Buffer Enable Video
CLK27M_CON	27MHz Clock to Digital Board
CS	Parallel interface chip select input of Link+Codec IC7431
CTL(0:1)	Link interface control lines
CTSN	Clear to Send
D(0:15)	Flash data lines of Link+Codec IC7431
DV_STATUS	Interrupt pin for reading DV-status
HS_CLK	Video clock input of Link+Codec IC7431
INT	Interrupt request output of Link+Codec IC7431 (input to Micro-Controller)
IOR	Parallel interface IO read control input of Link+Codec IC7431
ISPn	In System Programming signal (used for programming IC7802)
LKON	Link-on signal output
LPS	Link power status input
LREQ	Link request input
MA(0:10)	SDRAM address lines of Link+Codec IC7431
MCAS	SDRAM column address strobe signal
MCLK	
MD(0:15)	SDRAM data lines of Link+Codec IC7431
MRAS	SDRAM row-address strobe signal
MWE	SDRAM write enable signal
PCM1	Audio Serial Data Output of Link+Codec IC7431
PCM1_NEW	"MSB justified" to I2S converted audio serial data; audio serial data input of audio DAC UDA1334A
PD(0:15)	Data bus lines for Host I/F of Link+Codec IC7431
PHY_D(0:7)	Data bus connection between PHY and LINK device
RESETn	DVIO board reset
RESET_FM	Reset signal driven by Flashmaster programming device
RESTB	Reset input of Link+Codec IC7431
RTSN	Request to Send
RWZ	Parallel interface read/write control input of Link+Codec IC7431
RXD	Receive Data
SCLK	Link control output clock
TXD	Transmit Data
VPP	+10V switchable programming voltage of microcontroller
YUV(0:7)	Digital Video

10.2 Exploded View of the Front Panel Complete

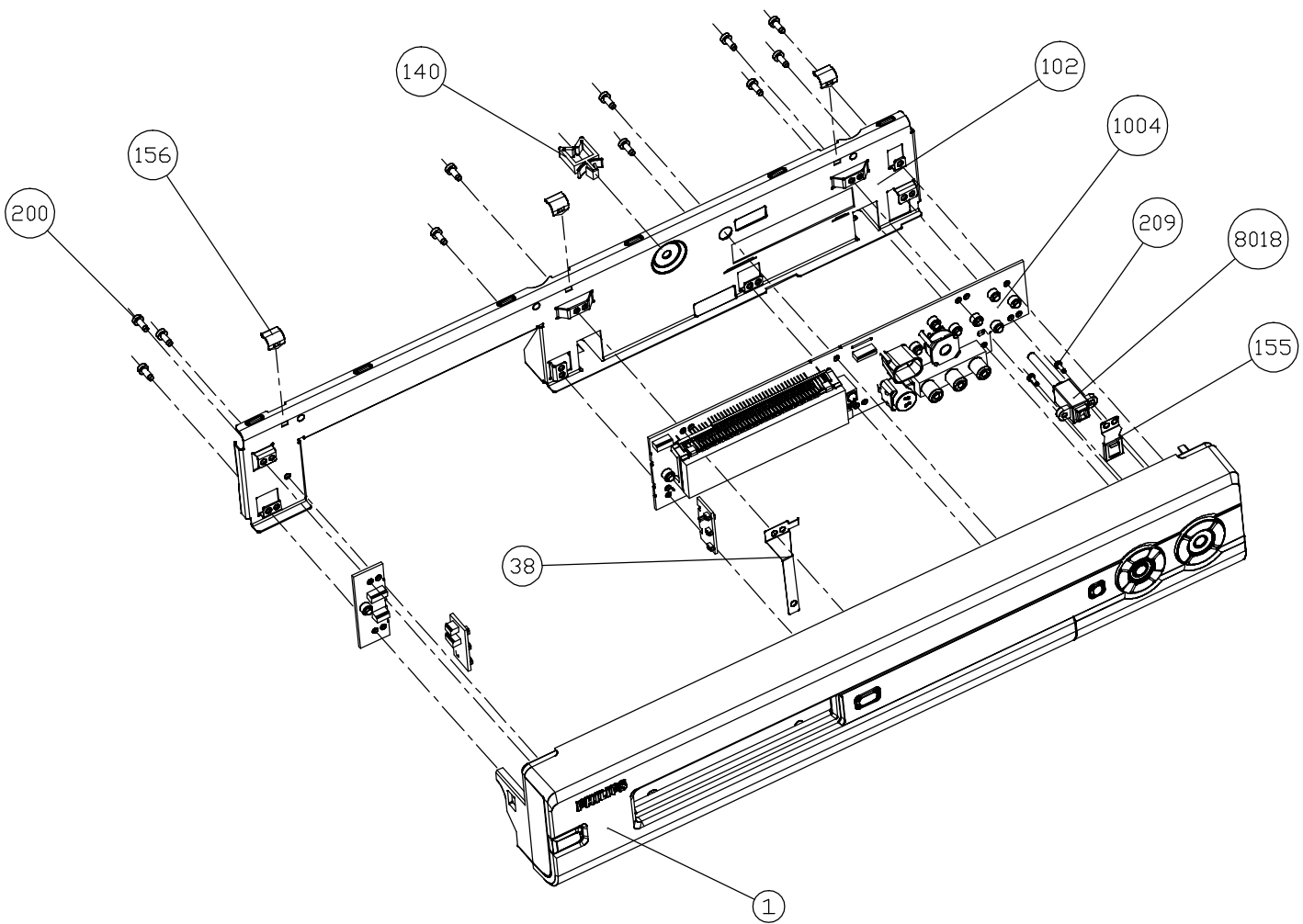
TR 06017_001
040203

Figure 10-2

Mechanical

Various

0001	3103 607 90601	FRONT DVDR70/001 AV3
0001	3103 607 90611	FRONT DVDR70/051 AV3
0001	3103 607 90621	FRONT DVDR75/001 AV3
0001	3103 607 90631	FRONT DVDR75/051 AV3
0001	3139 247 57931	FRONT DVDR70/001
0001	3139 247 58111	FRONT DVDR75/051
0001	3139 247 58121	FRONT DVDR75/001
0001	3139 247 58131	FRONT DVDR70/051
0011	3103 607 50341	BUTTON CAP STAND BY
0013	3103 607 50361	BUTTON CAP OPEN CL.
0020	3139 247 58041	WINDOW DISP DVDR75
0026	3139 247 58581	DOOR AV DVDR7X/051
0026	3139 247 58591	DOOR AV DVDR7X/001/021
0033	3103 604 00441	HINGE DOOR FRONT AV
0046	3139 247 58021	RING RECORD DVDR75
0047	3103 607 50411	BUTTON CAP RECORD
0048	3139 247 58001	RING ROCKER PLAY/P DVDR7x
0070	3103 607 90641	TRAY COVER DVDR7X AV3
0070	3139 247 57981	TRAY COVER DVDR7x
0105	3103 607 50491	FOOT ASSY
0164	3103 308 52950	FAN KD120 6PTS 3 - C112
0300	3103 607 50461	COVER ASSY
0350	3128 147 14551	REMOTE RC25115/05
0351▲	2422 070 98133	MAINSCORD EURO
0351▲	4822 321 10713	MAINS CORD UK
0352	3103 601 00111	SCART CABLE EU
0357	4822 320 50377	CONNECT. CABLE PAL
8001	3103 601 00190	FFC 22-POL-A-TYP 225MM (AB-DB)
8004	3103 601 00220	FFC 10-POL-D-TYP 350MM (UP-DB)
8005	3103 601 00230	FFC 22-POL-A-TYP 210MM (AB-DB)
8007	3103 601 00250	KR 4POL GESCH 180MM
8008	3103 601 00062	CBLE KR 12P/115/12P KR UL
8008	3103 601 00441	CBLE KR 12P/130/12P UL
8009	3103 601 00270	FFC 30/15-15-POL-A-TYP 400MM
8010	3103 601 00280	FFC 10-POL-A-TYP 650MM (AB-DC)
8012	3103 601 00400	CBLE KR 8P/125/8P KR UL
8013	3103 601 00310	KR 9POL GESCH 370MM
8018	3103 601 00350	IEEE 1394 DVIO
8019	3103 601 00360	IEEE 1394 CHRYSALIS 350MM
8026	3103 601 00431	FFC 22-POL-A-TYP 245MM (AB-DB)
8030	3103 601 00541	CBLE IDE 40P/380/40P UL

Display Board

Various

1110	4822 242 82114	EFOEC8004/T4
1130	4822 276 13732	Tact switch
1165	4822 276 13732	Tact switch
1166	4822 276 13732	Tact switch
1167	4822 276 13732	Tact switch
1168	4822 276 13732	Tact switch
1169	4822 276 13732	Tact switch
1170	4822 276 13732	Tact switch
1910	4822 267 11031	10P. FEM. V
1911	3103 601 00160	CABLE TREE ASSY 4 POL
1920	2422 026 05301	SOC CINCH V 3P
1921	2422 026 05307	CON MDIN H 4P F YKF51 B
1922	2422 025 10185	CON BM H 9P M 2.00 PH B

2100	5322 126 11583	10nF 10% 50V 0603
2101	3198 017 34730	47nF 16V 0603
2102	4822 124 11946	22µF 20% 16V
2103	5322 126 11583	10nF 10% 50V 0603
2104	2238 586 59812	100nF 20-80% 50V 0603
2110	4822 124 21732	10µF 20% 25V
2111	3198 017 34730	47nF 16V 0603
2112	4822 126 13879	220nF 20% 16V
2113	5322 121 42489	680nF 5% 63V
2114	5322 126 11578	1nF 10% 50V 0603
2115	3198 024 44730	47nF 50V 0603
2116	4822 124 11946	22µF 20% 16V
2117	4822 124 81151	22µF 50V
2118	2020 552 94427	100pF 5% 50v 0603
2119	2020 552 94427	100pF 5% 50v 0603

2120	2020 552 94427	100pF 5% 50v 0603
2121	2020 552 94427	100pF 5% 50v 0603
2122	2020 552 94427	100pF 5% 50v 0603
2123	2020 552 94427	100pF 5% 50v 0603
2124	2020 552 94427	100pF 5% 50v 0603
2125	2020 552 94427	100pF 5% 50v 0603
2126	2020 552 94427	100pF 5% 50v 0603
2200	4822 126 14241	330pF 50V 0603
2201	4822 126 14241	330pF 50V 0603
2202	2238 586 59812	100nF 20-80% 50V 0603

-W-

3100	4822 051 30223	22kΩ 5% 0.062W
3101	4822 051 30223	22kΩ 5% 0.062W
3102	4822 051 30222	2.2kΩ 5% 0.062W
3103	4822 051 30221	220Ω 5% 0.062W
3104	4822 051 30103	10kΩ 5% 0.062W
3106	4822 117 12925	47kΩ 1% 0.063W 0603
3107	4822 051 30222	2.2kΩ 5% 0.062W
3108	4822 117 12925	47kΩ 1% 0.063W 0603
3110	4822 051 30221	220Ω 5% 0.062W
3111	4822 051 30223	22kΩ 5% 0.062W
3112	4822 050 11002	1kΩ 1% 0.4W
3113	4822 051 30102	1kΩ 5% 0.062W
3114	4822 051 30101	100Ω 5% 0.062W
3115	4822 051 30101	100Ω 5% 0.062W
3116	4822 051 30331	330Ω 5% 0.062W
3117	4822 051 30103	10kΩ 5% 0.062W
3118	4822 051 30331	330Ω 5% 0.062W
3119	4822 051 30471	470Ω 5% 0.062W
3120	4822 051 30102	1kΩ 5% 0.062W
3121	4822 116 83872	220Ω 5% 0.5W
3122	4822 051 30103	10kΩ 5% 0.062W
3123	4822 051 30471	470Ω 5% 0.062W
3124	4822 051 30103	10kΩ 5% 0.062W
3125	4822 051 30471	470Ω 5% 0.062W
3126	4822 051 30101	100Ω 5% 0.062W
3127	4822 117 13632	100kΩ 1% 0.063 0.62W
3128	4822 117 13632	100kΩ 1% 0.063 0.62W
3130	4822 051 30103	10kΩ 5% 0.062W
3132	4822 051 30102	1kΩ 5% 0.062W
3134	4822 117 12063	NTC DC 5W 10K 5%
3137	4822 116 83876	270Ω 5% 0.5W
3139	4822 116 83876	270Ω 5% 0.5W
3141	4822 117 12925	47kΩ 1% 0.063W 0603
3144	4822 051 30103	10kΩ 5% 0.062W
3147	4822 116 52257	22kΩ 5% 0.5W
3148	4822 116 52257	22kΩ 5% 0.5W
3149	4822 116 52257	22kΩ 5% 0.5W
3150	4822 051 30223	22kΩ 5% 0.062W
3151	4822 051 30223	22kΩ 5% 0.062W
3152	4822 051 30223	22kΩ 5% 0.062W
3153	4822 051 30223	22kΩ 5% 0.062W
3200	4822 051 30102	1kΩ 5% 0.062W
3201	4822 051 30105	1MΩ 5% 0.062W
3202	4822 051 30102	1kΩ 5% 0.062W
3203	4822 051 30105	1MΩ 5% 0.062W
3204	4822 051 30689	68Ω 5% 0.063W 0603
3205	4822 051 30759	75Ω 5% 0.062W
3206	4822 051 30759	75Ω 5% 0.062W
3207	4822 051 30759	75Ω 5% 0.062W
3300	4822 051 30472	4.7kΩ 5% 0.062W
4111	4822 051 30008	Jumper 0603
4121	4822 051 30008	Jumper 0603
4122	4822 051 30008	Jumper 0603
4123	4822 051 30008	Jumper 0603

~

5100	4822 157 11706	10µH 5%
5101	2422 549 44607	Bead 600Ω at 100MHz
5103	2422 549 44607	Bead 600Ω at 100MHz
5104	4822 157 50964	100µH 20%

-D-

6100	4822 130 11416	PDZ6.8B
6101	9322 190 44676	LTL-1MHHR
6102	9322 190 44676	LTL-1MHHR
6103	9322 190 44676	LTL-1MHHR
6105	4822 130 11397	BAS316
6106	4822 130 11397	BAS316
6111	4822 130 11397	BAS316
6200	9322 146 61685	DF3A6.8FU
6201	9322 146 61685	DF3A6.8FU
6202	9322 146 61685	DF3A6.8FU
6203	9322 146 61685	DF3A6.8FU
6204	9322 146 61685	DF3A6.8FU



7100	2722 171 07736	VFD BJ900GNK
7101	3198 010 42310	BC847BW
7102	3198 010 42310	BC847BW
7103	3103 165 13731	TMP87C874F/LDCP1
7104	3198 010 42310	BC847BW
7105	3198 010 42310	BC847BW
7106	4822 130 40981	BC337-25
7107	9322 185 97667	TSOP4836ZC1
7108	4822 130 41241	BC327-25
7109	3198 010 42310	BC847BW
7112	4822 130 60854	DTA124EU-W

Analog Board

Various

1001▲	2422 086 10919	Fuse 65V 125mA
1300▲	2422 086 10899	FUSE5X20ET1A25 250V IEC B
1302▲	4822 252 11215	Spark gap
1303▲	4822 071 51002	19372(1A)
1304▲	2422 086 10786	FUSE 4A
1304▲	9965 000 07786	Fuse T4.0A 250V
1306▲	2422 086 10919	Fuse 65V 125mA
1307▲	4822 071 51002	19372(1A)
1308▲	2422 086 10951	PROT DEV 65V 500MA PSC
1308▲	4822 252 51187	19398E1(0,500A)
1309▲	2422 086 10783	LT 2A 250V IEC A
1309▲	4822 071 58001	19372(800MA)
1309▲	9965 000 07788	FUSE RAD T2A IEC UL250V
1600	4822 242 10434	Crystal 18.432 MHz
1701	4822 242 81436	Filter OFWK3953M
1702	2422 549 44341	SAW 38.9MHz OFWK9656M
1703	4822 242 10307	OFWK3956M
1703	4822 242 81436	Filter OFWK3953M
1704	2422 549 44611	5MHZ5 TPSR*MBQ2 BS A
1704	4822 242 72586	TPS5,5MB-TF20
1705	3139 147 17001	TUNER UV1316MK3
1706	2422 549 44612	6MHZ TPSR*MBQ2 BS A
1706	4822 242 81572	TPS6,0MB-TF21
1900	2422 025 18009	V 22P F 1.00 FFC 0.3 Y
1900	4822 265 11154	Connector 22p
1931▲	2422 030 00304	Socket 2P m h mains
1932	2422 025 10772	CON BM V 12P M 2.00 PH B
1933	4822 265 11352	Connector 8p
1934	4822 267 10565	Connector 4p
1940	2422 033 00334	CON BM EURO H 42P
1942	2422 025 10769	CON BMT 9P VERT PH-B
1943	2422 025 18143	CON V 10P F 1.00 FFC 0.3
1943	4822 267 11031	10P. FEM. V
1947	2422 025 18009	V 22P F 1.00 FFC 0.3 Y
1947	4822 265 11154	Connector 22p
1948	4822 267 10994	Socket SVHS
1949	2422 026 05308	SOC CINCH H 3P
1951	4822 267 31729	CONNECTOR
1960	2422 025 09406	Connector 4p
1990	4822 242 73552	13,875 000 MC

2000	4822 124 80483	47µF20% 6,3V
2001	4822 124 42234	100µF 20% 6,3V
2001	4822 124 80483	47µF20% 6,3V
2002	2238 586 59812	100nF 20-80% 50V 0603
2002	4822 124 42234	100µF 20% 6,3V
2003	2238 586 59812	100nF 20-80% 50V 0603
2004	2238 586 59812	100nF 20-80% 50V 0603
2004	4822 124 80483	47µF20% 6,3V
2005	4822 124 42234	100µF 20% 6,3V
2006	2238 916 11449	1nF 2% NPO 25V 0603
2006	3198 016 31020	1nF 10% 25V 0603
2006	4822 126 11785	47pF 5% 50V 0603
2007	4822 124 21732	10µF 20% 25V
2008	2238 916 11449	1nF 2% NPO 25V 0603
2008	3198 016 31020	1nF 10% 25V 0603
2009	2020 552 94427	100pF 5% 50v 0603
2009	2238 586 59812	100nF 20-80% 50V 0603
2010	4822 124 80483	47µF20% 6,3V
2011	2238 586 59812	100nF 20-80% 50V 0603
2011	4822 124 21732	10µF 20% 25V
2012	2238 586 59812	100nF 20-80% 50V 0603
2013	4822 124 42234	100µF 20% 6,3V
2014	2238 586 59812	100nF 20-80% 50V 0603
2015	2238 586 59812	100nF 20-80% 50V 0603
2016	4822 124 22652	2.2µF 20% 50V
2017	2020 552 94427	100pF 5% 50v 0603
2018	2238 586 59812	100nF 20-80% 50V 0603
2018	4822 124 21732	10µF 20% 25V

2019	2238 586 59812	100nF 20-80% 50V 0603	2340▲	2020 554 90169	470pF 250V 10%	2585	2238 586 59812	100nF 20-80% 50V 0603
2019	4822 124 21732	10µF 20% 25V	2341	3198 017 41050	1µF 10V 0603	2586	5322 126 11578	1nF 10% 50V 0603
2020	4822 124 21732	10µF 20% 25V	2342	3198 017 41050	1µF 10V 0603	2587	3198 017 41050	1µF 10V 0603
2020	4822 124 80483	47µF20% 6,3V	2343	2238 586 59812	100nF 20-80% 50V 0603	2590	4822 122 33741	150pF 5% 50V
2021	2238 586 59812	100nF 20-80% 50V 0603	2402	2238 586 59812	100nF 20-80% 50V 0603	2600	4822 124 21732	10µF 20% 25V
2023	2238 916 11449	1nF 2% NPO 25V 0603	2403	4822 124 80483	47µF20% 6,3V	2601	5322 126 11583	10nF 10% 50V 0603
2023	3198 016 31020	1nF 10% 25V 0603	2404	2238 586 59812	100nF 20-80% 50V 0603	2602	4822 124 21732	10µF 20% 25V
2023	4822 124 12392	47?F 20% 16V	2405	4822 124 80483	47µF20% 6,3V	2603	2238 586 59812	100nF 20-80% 50V 0603
2023	4822 124 80483	47µF20% 6,3V	2406	5322 126 11583	10nF 10% 50V 0603	2604	5322 126 11583	10nF 10% 50V 0603
2024	4822 126 11669	27pF 5% 50V 0603	2407	4822 122 33741	10pF 10% 50V	2605	4822 124 21732	10µF 20% 25V
2025	2238 916 11449	1nF 2% NPO 25V 0603	2408	3198 017 41050	1µF 10V 0603	2606	2238 586 59812	100nF 20-80% 50V 0603
2025	3198 016 31020	1nF 10% 25V 0603	2409	2238 586 59812	100nF 20-80% 50V 0603	2607	4822 126 14225	56pF 5% 50V 0603
2026	4822 126 11669	27pF 5% 50V 0603	2410	3198 017 41050	1µF 10V 0603	2608	4822 124 21732	10µF 20% 25V
2029	4822 124 12392	47?F 20% 16V	2411	2238 586 59812	100nF 20-80% 50V 0603	2609	4822 126 14225	56pF 5% 50V 0603
2029	4822 124 80483	47µF20% 6,3V	2412	4822 122 33741	10pF 10% 50V	2610	5322 126 11583	10nF 10% 50V 0603
2030	2238 916 11449	1nF 2% NPO 25V 0603	2413	4822 124 80483	47µF20% 6,3V	2611	4822 124 80231	47µF20% 16V
2030	3198 016 31020	1nF 10% 25V 0603	2414	2238 586 59812	100nF 20-80% 50V 0603	2612	4822 124 40769	4.7µF 20% 100V
2031	4822 124 22652	2.2µF 20% 50V	2416	3198 017 41050	1µF 10V 0603	2616	5322 126 11578	1nF 10% 50V 0603
2032	2238 916 11449	1nF 2% NPO 25V 0603	2417	4822 124 11947	10?F 20% 16V	2617	5322 126 11578	1nF 10% 50V 0603
2032	3198 016 31020	1nF 10% 25V 0603	2418	3198 017 41050	1µF 10V 0603	2620	3198 016 33380	3.3pF 50V 0603
2032	5322 126 11583	10nF 10% 50V 0603	2419	3198 017 41050	1µF 10V 0603	2621	3198 016 33380	3.3pF 50V 0603
2033	2020 552 94427	100pF 5% 50V 0603	2420	2238 586 59812	100nF 20-80% 50V 0603	2623	2238 586 59812	100nF 20-80% 50V 0603
2033	4822 126 13881	470pF 5% 50V	2421	4822 124 11947	10?F 20% 16V	2626	4822 124 22652	2.2µF 20% 50V
2034	4822 126 13881	470pF 5% 50V	2422	5322 126 11583	10nF 10% 50V 0603	2627	4822 124 22652	2.2µF 20% 50V
2035	2238 586 59812	100nF 20-80% 50V 0603	2423	3198 017 41050	1µF 10V 0603	2713	4822 124 11946	22µF 20% 16V
2037	2238 586 59812	100nF 20-80% 50V 0603	2424	4822 124 80483	47µF20% 6,3V	2719	4822 126 13883	220pF 5% 50V
2037	4822 126 13193	4.7nF 10% 63V	2425	2238 586 59812	100nF 20-80% 50V 0603	2720	4822 124 42234	100µF 20% 6,3V
2038	4822 124 42234	100µF 20% 6,3V	2427	3198 017 41050	1µF 10V 0603	2721	5322 126 13861	120pF10% 50V
2038	4822 126 13193	4.7nF 10% 63V	2428	4822 124 11947	10?F 20% 16V	2722	2022 020 00861	2.2µF 50V 20%
2039	4822 126 13193	4.7nF 10% 63V	2429	4822 124 11946	22µF 20% 16V	2722	5322 124 41379	2.2?F 20% 50V
2040	4822 126 13193	4.7nF 10% 63V	2430	2238 586 59812	100nF 20-80% 50V 0603	2723	4822 126 13881	470pF 5% 50V
2041	2020 552 94427	100pF 5% 50V 0603	2432	4822 124 42234	100µF 20% 6,3V	2724	2238 586 59812	100nF 20-80% 50V 0603
2042	2238 586 59812	100nF 20-80% 50V 0603	2433	3198 017 34730	47nF 16V 0603	2725	4822 122 33761	22pF 5% 50V
2043	4822 124 80483	47µF20% 6,3V	2434	4822 124 80483	47µF20% 6,3V	2727	2238 586 59812	100nF 20-80% 50V 0603
2045	2238 916 11449	1nF 2% NPO 25V 0603	2435	2238 586 59812	100nF 20-80% 50V 0603	2728	5322 126 11583	10nF 10% 50V 0603
2045	3198 016 31020	1nF 10% 25V 0603	2436	3198 017 41050	1µF 10V 0603	2729	4822 124 21732	10µF 20% 25V
2047	2238 916 11449	1nF 2% NPO 25V 0603	2437	3198 017 41050	1µF 10V 0603	2730	4822 126 13879	220nF 20% 16V
2047	3198 016 31020	1nF 10% 25V 0603	2438	3198 017 41050	1µF 10V 0603	2731	2020 552 94523	8.2pF 50V 0603
2048	2020 009 90097	100µF BP 16V 20%	2439	2238 586 59812	100nF 20-80% 50V 0603	2732	4822 124 22652	2.2µF 20% 50V
2048	2022 036 00005	10µF 16V 20%	2440	3198 017 41050	1µF 10V 0603	2733	2238 586 59812	100nF 20-80% 50V 0603
2048	4822 124 12392	47?F 20% 16V	2441	3198 017 41050	1µF 10V 0603	2734	5322 126 11578	1nF 10% 50V 0603
2048	4822 124 80483	47µF20% 6,3V	2442	4822 124 11946	22µF 20% 16V	2735	4822 126 14225	56pF 5% 50V 0603
2049	5322 126 11583	10nF 10% 50V 0603	2443	4822 124 42234	100µF 20% 6,3V	2736	4822 126 14225	56pF 5% 50V 0603
2050	2020 009 90097	100µF BP 16V 20%	2444	4822 126 13881	470pF 5% 50V	2737	4822 124 80483	47µF20% 6,3V
2050	2022 036 00005	10µF 16V 20%	2445	4822 126 13881	470pF 5% 50V	2740	4822 124 22652	2.2µF 20% 50V
2050	4822 124 12392	47?F 20% 16V	2446	3198 017 41050	1µF 10V 0603	2741	5322 126 11578	1nF 10% 50V 0603
2050	4822 124 80483	47µF20% 6,3V	2447	4822 126 13881	470pF 5% 50V	2742	5322 126 11578	1nF 10% 50V 0603
2301▲	2020 554 90173	2.2nF 20% 250V	2448	4822 126 13881	470pF 5% 50V	2932	2238 586 59812	100nF 20-80% 50V 0603
2301▲	4822 126 14088	2.2nF 20% 250V	2449	4822 126 13956	68pF 5% 63V 0603	2933	4822 124 80483	47µF20% 6,3V
2302▲	4822 121 10512	220nF 275V 20%	2450	2238 586 59812	100nF 20-80% 50V 0603	2934	2238 586 59812	100nF 20-80% 50V 0603
2303	4822 122 31175	1nF 10% 500V	2459	3198 017 41050	1µF 10V 0603	2935	2238 586 59812	100nF 20-80% 50V 0603
2304▲	4822 121 51598	2.2nF 5% 400V	2460	4822 124 40769	4.7µF 20% 100V	2936	4822 122 33761	22pF 5% 50V
2304	4822 126 10206	2.2nF 10% 500V	2461	4822 124 40769	4.7µF 20% 100V	2937	4822 122 33761	22pF 5% 50V
2305	2020 021 91506	1000µF 20% 16V	2462	4822 124 11947	10?F 20% 16V	2938	2238 586 59812	100nF 20-80% 50V 0603
2305	4822 124 40849	330µF 20% 16V	2463	4822 124 11947	10?F 20% 16V	2940	2238 586 59812	100nF 20-80% 50V 0603
2306	2020 021 91528	560µF 6V3 20%	2464	4822 124 21732	10µF 20% 25V	2941	4822 124 21732	10µF 20% 25V
2306	4822 124 40184	1000µF 20% 10V	2501	3198 017 41050	1µF 10V 0603	2942	4822 126 14238	2.2nF 50V 0603
2307	4822 122 31175	1nF 10% 500V	2502	2238 586 59812	100nF 20-80% 50V 0603	2943	4822 126 14508	180pF 5% 50V
2308	2022 318 00108	47nF 250V 10%	2503	2238 586 59812	100nF 20-80% 50V 0603	2944	4822 126 14238	2.2nF 50V 0603
2308	4822 121 70386	47nF 10% 250V	2504	3198 017 41050	1µF 10V 0603	2945	4822 126 14508	180pF 5% 50V
2309▲	2222 151 90053	68µF 400V 20%	2505	3198 017 41050	1µF 10V 0603	2946	3198 017 41050	1µF 10V 0603
2310	5322 126 11578	1nF 10% 50V 0603	2506	3198 017 41050	1µF 10V 0603	2947	3198 017 41050	1µF 10V 0603
2311	5322 126 11578	1nF 10% 50V 0603	2507	3198 017 41050	1µF 10V 0603			
2312	2020 021 91506	1000µF 20% 16V	2508	3198 017 41050	1µF 10V 0603			
2313	2020 021 91528	560µF 6V3 20%	2509	2238 586 59812	100nF 20-80% 50V 0603			
2313	4822 124 40184	1000µF 20% 10V	2510	4822 124 42234	100µF 20% 6,3V			
2315▲	4822 126 14525	47pF 5% 1kV	2511	2020 009 90097	100µF BP 16V 20%			
2317	5322 126 11578	1nF 10% 50V 0603	2511	2022 036 00005	10µF 16V 20%			
2318	4822 126 10206	2.2nF 10% 500V	2512	2238 586 59812	100nF 20-80% 50V 0603			
2319	2020 021 91506	1000µF 20% 16V	2513	2020 552 96807	1µF 10V 0603 X5R			
2319	4822 124 40849	330µF 20% 16V	2513	3198 017 41050	1µF 10V 0603			
2320	4822 124 40849	330µF 20% 16V	2514	2238 586 59812	100nF 20-80% 50V 0603			
2320	4822 124 80791	470µF 20% 16V	2515	2020 552 96807	1µF 10V 0603 X5R			
2321	2238 586 59812	100nF 20-80% 50V 0603	2515	3198 017 41050	1µF 10V 0603			
2322▲	2020 021 91506	1000µF 20% 16V	2516	2020 009 90097	100µF BP 16V 20%			
2322	2020 021 91569	470µF 10V	2516	2022 036 00005	10µF 16V 20%			
2322	4822 124 41584	100µF 20% 10V	2517	5322 126 11578	1nF 10% 50V 0603			
2323	4822 124 42234	100µF 20% 6,3V	2518	2238 586 59812	100nF 20-80% 50V 0603			
2324	2238 586 59812	100nF 20-80% 50V 0603	2519	4822 124 42234	100µF 20% 6,3V			
2325	4822 124 81151	22µF 50V	2520	5322 126 11578	1nF 10% 50V 0603			
2326	4822 121 41857	10nF 5% 250V	2521	2238 586 59812	100nF 20-80% 50V 0603			
2327	2238 586 59812	100nF 20-80% 50V 0603	2522	2020 009 90097	100µF BP 16V 20%			
2328	4822 124 81151	22µF 50V	2522	2022 036 00005	10µF 16V 20%			
2329	2238 586 59812	100nF 20-80% 50V 0603	2523	5322 126 11578	1nF 10% 50V 0603			
2330	5322 126 11578	1nF 10% 50V 0603	2524	3198 017 41050	1µF 10V 0603			
2331	2238 586 59812	100nF 20-80% 50V 0603	2525	3198 017 41050	1µF 10V 0603			
2332	4822 124 22651	1µF 20% 50V	2526	2020 009 90097	100µF BP 16V 20%			
2334	2238 586 59812	100nF 20-80% 50V 0603	2526	2022 036 00005	10µF 16V 20%			
2335	4822 124 21732	10µF 20% 25V	2527	5322 126 11578	1nF 10% 50V 0603			
2336	2238 586 59812	100nF 20-80						

3013	2322 704 67502	7.5K 1% 0.5W	3318	4822 116 52175	100Ω 5% 0.5W	3437	4822 051 30103	10kΩ 5% 0.062W
3013	4822 117 12139	22Ω 5% 0.062W	3321	2322 193 14477	0.47Ω PR01 PM5	3438	4822 051 30103	10kΩ 5% 0.062W
3013	5322 117 13053	6.8kΩ 1% 0.063W 0603	3323	4822 117 12891	220kΩ 1% 0.063W 0603	3439	4822 051 30103	10kΩ 5% 0.062W
3014	2120 108 93941	5.62kΩ 1% 0603	3324	2322 702 60564	560kΩ 5% 0603	3440	4822 051 30103	10kΩ 5% 0.062W
3014	4822 051 30103	10kΩ 5% 0.062W	3325	4822 117 12925	47kΩ 1% 0.063W 0603	3441	4822 116 52201	75Ω 5% 0.5W
3014	5322 117 13031	5.6kΩ 1% 0603	3326	4822 116 52175	100Ω 5% 0.5W	3442	4822 051 30154	150kΩ 5% 0.062W
3015	4822 051 30471	470Ω 5% 0.062W	3326	4822 116 52195	47Ω 5% 0.5W	3443	4822 117 13632	100kΩ 1% 0603 0.62W
3015	4822 117 13613	2R2 5% 0603	3327	4822 051 30105	1MΩ 5% 0.062W	3444	4822 117 13632	100kΩ 1% 0603 0.62W
3016	5322 117 13038	27K 1% 0.063W 0603 RC22H	3328	4822 051 30103	10kΩ 5% 0.062W	3445	4822 051 30151	150Ω 5% 0.062W
3017	4822 117 13613	2R2 5% 0603	3329	3198 021 32250	2.2MΩ 5% 0603	3446	4822 117 12925	47kΩ 1% 0.063W 0603
3017	5322 117 13024	33kΩ 1% 0.063W 0603	3330	4822 051 30471	470Ω 5% 0.062W	3447	4822 116 83884	47kΩ 5% 0.5W
3018	2120 108 93941	5.62kΩ 1% 0603	3331	4822 051 30109	10Ω 5% 0.062W	3448	4822 051 30271	270Ω 5% 0.062W
3018	4822 117 12139	22Ω 5% 0.062W	3332	2120 108 93941	5.62kΩ 1% 0603	3448	4822 051 30471	470Ω 5% 0.062W
3018	5322 117 13031	5.6kΩ 1% 0603	3332	5322 117 13031	5.6kΩ 1% 0603	3449	4822 051 30151	150Ω 5% 0.062W
3019	4822 116 52186	22Ω 5% 0.5W	3333	5322 117 13026	4.7kΩ 1% 0.063W 0603	3450	4822 051 30271	270Ω 5% 0.062W
3019	4822 117 12139	22Ω 5% 0.062W	3334	4822 051 30563	56kΩ 5% 0.062W	3450	4822 051 30471	470Ω 5% 0.062W
3020	4822 051 30472	4.7kΩ 5% 0.062W	3335	4822 051 30471	470Ω 5% 0.062W	3451	4822 050 21003	10kΩ 1% 0.6W
3020	4822 117 12139	22Ω 5% 0.062W	3336	4822 051 30471	470Ω 5% 0.062W	3452	4822 051 30151	150Ω 5% 0.062W
3021	4822 051 30103	10kΩ 5% 0.062W	3337	4822 051 30102	1kΩ 5% 0.062W	3454	4822 050 11002	1kΩ 1% 0.4W
3022	4822 117 12139	22Ω 5% 0.062W	3338	4822 051 30221	220Ω 5% 0.062W	3455	4822 051 30103	10kΩ 5% 0.062W
3023	4822 117 12139	22Ω 5% 0.062W	3339	5322 117 13026	4.7kΩ 1% 0.063W 0603	3458	4822 051 30472	4.7kΩ 5% 0.062W
3024	4822 117 12139	22Ω 5% 0.062W	3340	5322 117 13026	4.7kΩ 1% 0.063W 0603	3459	4822 051 30103	10kΩ 5% 0.062W
3024	4822 117 12925	47kΩ 1% 0.063W 0603	3341	4822 051 30683	68kΩ 5% 0.062W	3460	4822 051 30472	4.7kΩ 5% 0.062W
3025	4822 117 13632	100kΩ 1% 0603 0.62W	3342	4822 116 52283	4.7kΩ 5% 0.5W	3461	2122 551 00031	VDR 0805 1mA/6V4 21V
3026	4822 117 12139	22Ω 5% 0.062W	3342	5322 117 13026	4.7kΩ 1% 0.063W 0603	3461	2322 574 10402	VDR 0805 1mA/6V4 21V
3026	4822 117 12925	47kΩ 1% 0.063W 0603	3343	5322 117 13026	4.7kΩ 1% 0.063W 0603	3462	2122 551 00031	VDR 0805 1mA/6V4 21V
3027	5322 117 13024	33kΩ 1% 0.063W 0603	3344	4822 051 30683	68kΩ 5% 0.062W	3462	2322 574 10402	VDR 0805 1mA/6V4 21V
3027	5322 117 13026	4.7kΩ 1% 0.063W 0603	3344	4822 117 12925	47kΩ 1% 0.063W 0603	3462	2322 574 10402	VDR 0805 1mA/6V4 21V
3028	4822 117 12139	22Ω 5% 0.062W	3344	4822 051 30222	2.2kΩ 5% 0.062W	3463	2122 551 00031	VDR 0805 1mA/6V4 21V
3029	4822 051 30101	100Ω 5% 0.062W	3347	4822 051 30472	4.7kΩ 5% 0.062W	3463	2322 574 10402	VDR 0805 1mA/6V4 21V
3029	4822 117 12917	1Ω 5% 0.062W 0603	3348	4822 051 30681	680Ω 5% 0.062W	3464	2122 551 00031	VDR 0805 1mA/6V4 21V
3030	5322 117 13038	27K 1% 0.063W 0603 RC22H	3348	4822 051 30479	47Ω 5% 0.062W	3464	2322 574 10402	VDR 0805 1mA/6V4 21V
3030	5322 117 13047	330Ω 1% 0.063W 0603	3349	4822 051 30479	47Ω 5% 0.062W	3465	2122 551 00031	VDR 0805 1mA/6V4 21V
3031	4822 051 30103	10kΩ 5% 0.062W	3350	4822 051 30102	1kΩ 5% 0.062W	3465	2322 574 10402	VDR 0805 1mA/6V4 21V
3032	2322 704 67502	7.5K 1% 0.5W	3351	2322 702 60564	560kΩ 5% 0603	3466	2122 551 00031	VDR 0805 1mA/6V4 21V
3032	5322 117 13053	6.8kΩ 1% 0.063W 0603	3351	4822 051 30105	1MΩ 5% 0.062W	3466	2322 574 10402	VDR 0805 1mA/6V4 21V
3033	4822 117 12139	22Ω 5% 0.062W	3352	2322 193 14687	0.68Ω PR01 PM5	3467	2122 551 00031	VDR 0805 1mA/6V4 21V
3034	4822 117 12925	47kΩ 1% 0.063W 0603	3353	4822 051 30272	2.7kΩ 5% 0.062W	3467	2322 574 10402	VDR 0805 1mA/6V4 21V
3034	4822 117 13613	2R2 5% 0603	3354	4822 051 30272	2.7kΩ 5% 0.062W	3468	2122 551 00031	VDR 0805 1mA/6V4 21V
3035	4822 050 21003	10kΩ 1% 0.6W	3355	4822 051 30479	47Ω 5% 0.062W	3468	2322 574 10402	VDR 0805 1mA/6V4 21V
3035	4822 117 13613	2R2 5% 0603	3356	4822 116 52231	820Ω 5% 0.5W	3469	4822 117 13632	100kΩ 1% 0603 0.62W
3036	2322 704 67502	7.5K 1% 0.5W	3357	4822 051 30472	4.7kΩ 5% 0.062W	3470	4822 117 13632	100kΩ 1% 0603 0.62W
3036	5322 117 13053	6.8kΩ 1% 0.063W 0603	3358	4822 051 30109	10Ω 5% 0.062W	3471	4822 117 13632	100kΩ 1% 0603 0.62W
3039	4822 050 21003	10kΩ 1% 0.6W	3358	4822 116 52231	820Ω 5% 0.5W	3472	4822 117 13632	100kΩ 1% 0603 0.62W
3039	5322 117 13038	27K 1% 0.063W 0603 RC22H	3360	4822 051 30102	1kΩ 5% 0.062W	3473	4822 051 30101	100Ω 5% 0.062W
3040	5322 117 13024	33kΩ 1% 0.063W 0603	3361	4822 051 30102	1kΩ 5% 0.062W	3474	4822 051 30101	100Ω 5% 0.062W
3041	4822 050 21003	10kΩ 1% 0.6W	3362	4822 051 30681	680Ω 5% 0.062W	3475	4822 051 30101	100Ω 5% 0.062W
3042	4822 050 21003	10kΩ 1% 0.6W	3363	4822 051 30222	2.2kΩ 5% 0.062W	3476	4822 051 30101	100Ω 5% 0.062W
3043	4822 117 12139	22Ω 5% 0.062W	3364	4822 051 30103	10kΩ 5% 0.062W	3477	4822 051 30101	100Ω 5% 0.062W
3043	4822 117 12925	47kΩ 1% 0.063W 0603	3365	4822 051 30332	3.3kΩ 5% 0.062W	3478	4822 051 30101	100Ω 5% 0.062W
3044	4822 051 30103	10kΩ 5% 0.062W	3366	4822 051 30152	1.5kΩ 5% 0.062W	3478	4822 051 30101	100Ω 5% 0.062W
3044	4822 117 12925	47kΩ 1% 0.063W 0603	3367	4822 117 12903	1.8kΩ 1% 0.063W 0603	3487	4822 117 13632	100kΩ 1% 0603 0.62W
3045	4822 051 30102	1kΩ 5% 0.062W	3368	4822 051 30152	1.5kΩ 5% 0.062W	3488	4822 117 13632	100kΩ 1% 0603 0.62W
3045	4822 117 12925	47kΩ 1% 0.063W 0603	3368	4822 051 30332	3.3kΩ 5% 0.062W	3489	4822 117 12864	82kΩ 5% 0.6W
3045	4822 117 13632	100kΩ 1% 0603 0.62W	3371	4822 051 30479	47Ω 5% 0.062W	3490	4822 051 30151	150Ω 5% 0.062W
3046	4822 051 30471	470Ω 5% 0.062W	3372	4822 051 30339	33Ω 5% 0.062W	3491	4822 051 30151	150Ω 5% 0.062W
3046	4822 116 52257	22kΩ 5% 0.5W	3373	4822 051 30339	33Ω 5% 0.062W	3492	4822 051 30151	150Ω 5% 0.062W
3047	4822 050 21003	10kΩ 1% 0.6W	3374	4822 051 30471	470Ω 5% 0.062W	3493	4822 051 30151	150Ω 5% 0.062W
3047	4822 117 13632	100kΩ 1% 0603 0.62W	3375	4822 051 30471	470Ω 5% 0.062W	3494	4822 051 30151	150Ω 5% 0.062W
3048	4822 051 30101	100Ω 5% 0.062W	3376	4822 051 30471	470Ω 5% 0.062W	3495	4822 051 30471	470Ω 5% 0.062W
3049	4822 051 30472	4.7kΩ 5% 0.062W	3378	4822 051 30152	1.5kΩ 5% 0.062W	3495	4822 051 30472	4.7kΩ 5% 0.062W
3050	4822 117 13632	100kΩ 1% 0603 0.62W	3401	5322 117 13055	75R 1% 0.063W 0603	3496	4822 051 30471	470Ω 5% 0.062W
3051	4822 051 30223	22kΩ 5% 0.062W	3402	5322 117 13055	75R 1% 0.063W 0603	3496	4822 051 30472	4.7kΩ 5% 0.062W
3051	4822 117 13632	100kΩ 1% 0603 0.62W	3403	5322 117 13055	75R 1% 0.063W 0603	3501	4822 051 30102	1kΩ 5% 0.062W
3052	4822 051 30223	22kΩ 5% 0.062W	3404	4822 051 30759	75Ω 5% 0.062W	3502	4822 050 11002	1kΩ 1% 0.4W
3052	4822 051 30332	3.3kΩ 5% 0.062W	3405	4822 051 30223	22kΩ 5% 0.062W	3503	4822 117 13632	100kΩ 1% 0603 0.62W
3053	4822 050 21003	10kΩ 1% 0.6W	3406	4822 117 12891	220kΩ 1% 0.063W 0603	3504	4822 117 13632	100kΩ 1% 0603 0.62W
3053	4822 117 13632	100kΩ 1% 0603 0.62W	3407	4822 051 30332	3.3kΩ 5% 0.062W	3505	4822 117 13632	100kΩ 1% 0603 0.62W
3054	4822 051 30332	3.3kΩ 5% 0.062W	3408	4822 051 30392	3.9kΩ 5% 0.063W 0603	3506	4822 117 13632	100kΩ 1% 0603 0.62W
3054	4822 117 12139	22Ω 5% 0.062W	3409	5322 117 13055	75R 1% 0.063W 0603	3507	4822 117 13632	100kΩ 1% 0603 0.62W
3300▲	4822 053 21335	3.3MΩ 5% 0.5W	3410	5322 117 13055	75R 1% 0.063W 0603	3508	4822 051 30102	1kΩ 5% 0.062W
3301▲	4822 053 21335	3.3MΩ 5% 0.5W	3411	4822 051 30759	75Ω 5% 0.062W	3509	4822 050 11002	1kΩ 1% 0.4W
3302	4822 051 30102	1kΩ 5% 0.062W	3412	4822 116 52201	75Ω 5% 0.5W	3510	4822 117 13632	100kΩ 1% 0603 0.62W
3303	4822 051 30102	1kΩ 5% 0.062W	3413	5322 117 13055	75R 1% 0.063W 0603	3511	4822 117 13632	100kΩ 1% 0603 0.62W
3304	4822 051 30103	10kΩ 5% 0.062W	3414	4822 051 30759	75Ω 5% 0.062W	3512	4822 051 30102	1kΩ 5% 0.062W
3305▲	4822 053 21684	680kΩ 5% 0.5W	3415	4822 051 30102	1kΩ 5% 0.062W	3513	4822 051 30102	1kΩ 5% 0.062W
3306	4822 116 83872	220Ω 5% 0.5W	3416	4822 051 30472	4.7kΩ 5% 0.062W	3514	4822 117 13632	100kΩ 1% 0603 0.62W
3307	4822 051 30103	10kΩ 5% 0.062W	3417	4822 051 30759	75Ω 5% 0.062W	3515	4822 050 11002	1kΩ 1% 0.4W
3308	4822 116 52227	330k 5% 0.5W	3418	4822 117 13632	100kΩ 1% 0603 0.62W	3516	4822 117 13632	100kΩ 1% 0603 0.62W
3309	4822 116 52272	330k 5% 0.5W	3419	4822 051 30223	22kΩ 5% 0.062W	3517	4822 116 52283	4.7kΩ 5% 0.5W
3310	4822 116 52272	330k 5% 0.5W	3420	4822 051 30151	150Ω 5% 0.062W	3518	4822 051 30102	1kΩ 5% 0.062W
3311	4822 051 30102	1kΩ 5% 0.062W	3421	4822 051 30273	27kΩ 5% 0.062W	3519	4822 116	

3534	4822 117 13632	100kΩ 1% 0603 0.62W
3580	4822 051 30759	75Ω 5% 0.062W
3581	4822 051 30222	2.2kΩ 5% 0.062W
3582	4822 051 30331	330Ω 5% 0.062W
3584	4822 051 30471	470Ω 5% 0.062W
3585	4822 051 30561	560Ω 5% 0.062W
3600	4822 051 30103	10kΩ 5% 0.062W
3601	4822 116 52175	100Ω 5% 0.5W
3602	4822 051 30472	4.7kΩ 5% 0.062W
3603	4822 116 52175	100Ω 5% 0.5W
3606	4822 051 30102	1kΩ 5% 0.062W
3607	4822 051 30102	1kΩ 5% 0.062W
3611	4822 051 30101	100Ω 5% 0.062W
3612	4822 051 30101	100Ω 5% 0.062W
3701	4822 116 52228	680Ω 5% 0.5W
3702	4822 051 30471	470Ω 5% 0.062W
3703	4822 116 52245	150kΩ 5% 0.5W
3704	4822 051 30221	220Ω 5% 0.062W
3705	4822 051 30103	10kΩ 5% 0.062W
3710	4822 051 30562	5.6kΩ 5% 0.063W 0603
3711	4822 051 30333	33kΩ 5% 0.062W
3714	4822 051 30183	18kΩ 5% 0.062W
3715	4822 051 30103	10kΩ 5% 0.062W
3716	4822 051 30472	4.7kΩ 5% 0.062W
3717	4822 051 30472	4.7kΩ 5% 0.062W
3720	4822 051 30331	330Ω 5% 0.062W
3724	4822 100 12158	22k 30%
3725	4822 117 12902	8.2kΩ 1% 0.063W 0603
3726	4822 051 30101	100Ω 5% 0.062W
3727	4822 117 12917	1Ω 5% 0.062W 0603
3728	4822 051 30101	100Ω 5% 0.062W
3729	4822 117 12917	1Ω 5% 0.062W 0603
3730	4822 051 30472	4.7kΩ 5% 0.062W
3731	4822 051 30271	270Ω 5% 0.062W
3731	4822 051 30331	330Ω 5% 0.062W
3732	4822 051 30102	1kΩ 5% 0.062W
3733	4822 051 30472	4.7kΩ 5% 0.062W
3734	4822 051 30272	2.7kΩ 5% 0.062W
3735	4822 051 30332	3.3kΩ 5% 0.062W
3736	4822 051 30331	330Ω 5% 0.062W
3737	4822 051 30222	2.2kΩ 5% 0.062W
3738	4822 051 30682	6.8kΩ 5% 0.062W
3739	4822 051 30562	5.6kΩ 5% 0.063W 0603
3740	4822 051 30681	680Ω 5% 0.062W
3741	4822 051 30472	4.7kΩ 5% 0.062W
3742	4822 051 30472	4.7kΩ 5% 0.062W
3743	4822 051 30563	56kΩ 5% 0.062W
3744	4822 117 13632	100kΩ 1% 0603 0.62W
3745	4822 051 30562	5.6kΩ 5% 0.063W 0603
3746	4822 051 30562	5.6kΩ 5% 0.063W 0603
3758	4822 051 30103	10kΩ 5% 0.062W
3931	4822 117 12925	47kΩ 1% 0.063W 0603
3932	4822 117 12925	47kΩ 1% 0.063W 0603
3933	4822 117 12925	47kΩ 1% 0.063W 0603
3934	4822 051 30101	100Ω 5% 0.062W
3935	4822 051 30101	100Ω 5% 0.062W
3936	4822 051 30103	10kΩ 5% 0.062W
3937	4822 051 30222	2.2kΩ 5% 0.062W
3938	4822 051 30222	2.2kΩ 5% 0.062W
3939	4822 051 30472	4.7kΩ 5% 0.062W
3940	3198 021 31060	10MΩ 5% 0.062W 0603
3941	3198 021 31060	10MΩ 5% 0.062W 0603
3942	4822 051 30333	33kΩ 5% 0.062W
3943	4822 051 30333	33kΩ 5% 0.062W
3944	4822 051 30333	33kΩ 5% 0.062W
3945	4822 051 30333	33kΩ 5% 0.062W
3946	4822 051 30333	33kΩ 5% 0.062W
3947	4822 051 30333	33kΩ 5% 0.062W
3948	4822 051 30472	4.7kΩ 5% 0.062W
3950	4822 117 13632	100kΩ 1% 0603 0.62W
3951	4822 051 30223	22kΩ 5% 0.062W
3952	4822 051 30153	15kΩ 5% 0.062W
3953	4822 051 30472	4.7kΩ 5% 0.062W
3954	4822 051 30472	4.7kΩ 5% 0.062W
3955	4822 051 30103	10kΩ 5% 0.062W
4001	4822 051 30008	Jumper 0603
4002	4822 051 30008	Jumper 0603
4003	4822 051 30008	Jumper 0603
4004	4822 051 30008	Jumper 0603
4402	4822 051 30008	Jumper 0603
4411	4822 051 30008	Jumper 0603
4412	4822 051 30008	Jumper 0603
4413	4822 051 30008	Jumper 0603
4414	4822 051 30008	Jumper 0603
4415	4822 051 30008	Jumper 0603
4416	4822 051 30008	Jumper 0603
4417	4822 051 30008	Jumper 0603
4418	4822 051 30008	Jumper 0603
4419	4822 051 30008	Jumper 0603
4420	4822 051 30008	Jumper 0603
4421	4822 051 30008	Jumper 0603
4422	4822 051 30008	Jumper 0603
4423	4822 051 30008	Jumper 0603
4424	4822 051 30008	Jumper 0603

4425	4822 051 30008	Jumper 0603
4426	4822 051 30008	Jumper 0603
4427	4822 051 30008	Jumper 0603
4428	4822 051 30008	Jumper 0603
4429	4822 051 30008	Jumper 0603
4430	4822 051 30008	Jumper 0603
4431	4822 051 30008	Jumper 0603
4433	4822 051 30008	Jumper 0603
4434	4822 051 30008	Jumper 0603
4435	4822 051 30008	Jumper 0603
4437	4822 051 30008	Jumper 0603
4442	4822 051 30008	Jumper 0603
4443	4822 051 30008	Jumper 0603
4444	4822 051 30008	Jumper 0603
4445	4822 051 30008	Jumper 0603
4446	4822 051 30008	Jumper 0603
4447	4822 051 30008	Jumper 0603
4448	4822 051 30008	Jumper 0603
4449	4822 051 30008	Jumper 0603
4452	4822 051 30008	Jumper 0603
4453	4822 051 30008	Jumper 0603
4454	4822 051 30008	Jumper 0603
4455	4822 051 30008	Jumper 0603
4456	2422 549 43062	Bead 600Ω at 100MHz
4456	4822 051 30008	Jumper 0603
4457	4822 051 30008	Jumper 0603
4459	4822 051 30008	Jumper 0603
4460	4822 051 10008	Jumper 1206
4461	4822 051 30008	Jumper 0603
4601	4822 051 30008	Jumper 0603
4700	4822 051 30008	Jumper 0603
4701	4822 051 30008	Jumper 0603
4999	4822 051 30008	Jumper 0603
~		
5001	2422 549 43062	Bead 600Ω at 100MHz
5002	2422 549 43062	Bead 600Ω at 100MHz
5300▲	2422 531 02546	SRW28EC9-E01V0* B
5300▲	3128 138 40782	CT286D8 B
5302▲	2422 549 44509	25MH OA4 HF2022R Y
5304	4822 157 70826	2.4μH
5305	4822 157 70826	2.4μH
5306	2422 535 94634	2.2μH LHL08 20%
5307	4822 157 11737	22μH 10%
5308	4822 157 11737	22μH 10%
5309	4822 157 11737	22μH 10%
5401	4822 157 11706	10μH 5%
5402	4822 157 11706	10μH 5%
5403	4822 157 11706	10μH 5%
5404	4822 157 11706	10μH 5%
5405	2422 549 43062	Bead 600Ω at 100MHz
5406	4822 157 11706	10μH 5%
5407	2422 549 43062	Bead 600Ω at 100MHz
5580	2422 536 00019	TRANSFORMER 6RG
5581	4822 157 11706	10μH 5%
5600▲	4822 157 11706	10μH 5%
5601▲	4822 157 11706	10μH 5%
5602▲	4822 157 11706	10μH 5%
5701	2422 549 43062	Bead 600Ω at 100MHz
5702	2422 549 43062	Bead 600Ω at 100MHz
5705	4822 157 11139	6.8μH 5%
5709	4822 157 11139	6.8μH 5%
5710	2422 549 44162	IND VAR 7MM 7KMY 77M8
5711	2422 549 44162	IND VAR 7MM 7KMY 77M8
5711	2422 549 45833	IND VAR 7MM 7KLY 77MHZ8
5713	4822 157 11747	15UH 5%
5714	4822 157 11747	15UH 5%
5931	4822 157 11706	10μH 5%
5932	2422 549 43062	Bead 600Ω at 100MHz
⊥		
6001	4822 130 11397	BAS316
6002	4822 130 11397	BAS316
6003	4822 130 11397	BAS316
6003	4822 130 30621	1N4148
6004	4822 130 11397	BAS316
6004	4822 130 30621	1N4148
6005	4822 130 11397	BAS316
6006	9340 260 20115	BAW56W
6007	4822 130 11397	BAS316
6300	5322 130 32677	1N5822
6300	9322 161 77682	SB340L-7024
6300	9322 182 65682	DIO REC STTH302-C2 (ST00) B
6301	4822 130 31603	1N4006
6302	4822 130 31603	1N4006
6303	5322 130 32677	1N5822
6303	9322 161 77682	SB340L-7024

6303	9322 182 65682	DIO REC STTH302-C2 (ST00) B
6304	4822 130 31878	1N4003G
6305	4822 130 31603	1N4006
6306	4822 130 31603	1N4006
6307	4822 130 82627	SB540
6307	9322 161 77682	SB540L-7024
6307	9322 184 68682	STPS5L40-C2
6308	4822 130 82627	SB540
6308	9322 161 77682	SB540L-7024
6308	9322 184 68682	STPS5L40-C2
6309	9322 126 71673	BYT42M
6310	9322 161 78682	SB360L-7024
6310	9322 182 65682	DIO REC STTH302-C2
6310	9322 188 34682	STPS3L60-C2
6311	4822 130 31878	1N4003G
6312	4822 130 11416	PDZ6.8B
6313	4822 130 10871	SBYV27-200
6313	9322 199 50673	UF202G
6314	4822 130 10837	UDZS8.2B
6315	4822 130 11397	BAS316
6316	4822 130 30842	BAV21
6317	4822 130 42488	BYD33D
6317	9322 126 71673	BYT42M
6317	9322 196 45673	PG102R
6318	3198 010 53390	BZX79-B33
6318	4822 130 34142	BZX79-B33
6319	4822 130 42488	BYD33D
6319	9322 126 71673	BYT42M
6319	9322 196 45673	PG102R
6320	4822 130 11397	BAS316
6321	4822 130 10654	BAT254
6321	4822 130 80622	BAT54
6322	4822 130 11416	PDZ6.8B
6324	9340 548 69115	PDZ27B
6325	4822 130 10871	SBYV27-200
6325	4822 130 81234	1N5819
6401	9340 548 61115	PDZ12B
6402	9340 548 61115	PDZ12B
6403	9340 548 61115	PDZ12B
6404	9340 548 61115	PDZ12B
6409	4822 130 11416	PDZ6.8B
6414	4822 130 11416	PDZ6.8B
6415	9340 548 61115	PDZ12B
6416	9340 548 61115	PDZ12B
6417	9340 548 61115	PDZ12B
6418	9340 548 61115	PDZ12B
6419	9340 548 61115	PDZ12B
6420	9340 548 61115	PDZ12B
6422	4822 130 11564	UDZ3.9B
6423	9340 548 61115	PDZ12B
6424	9340 548 61115	PDZ12B
6425	9340 548 61115	PDZ12B
6426	9340 548 61115	PDZ12B
6427	9340 548 61115	PDZ12B
6428	9340 548 61115	PDZ12B
6429	9340 548 61115	PDZ12B
6600	4822 130 11397	BAS316
6703	9340 552 30115	BA591
6704	9340 552 30115	BA591
6705	9340 552 30115	BA591
☐		
7001	3198 010 42320	BC857BW
7001	4822 130 60854	DTA124EU-W
7001	9352 668 47118	UDA1334BTS/N2
7002	4822 209 62312	MC33078D
7003	4822 130 60854	DTA124EU-W
7003	4822 209 62312	MC33078D
7004	9322 148 78668	IC SM AD1852JRS
7005	3198 010 42310	BC847BW
7005	9352 670 99118	UDA1361TS/N1
7006	3198 010 42310	BC847BW
7006	3198 010 42320	BC857BW
7007	9352 670 99118	UDA1361TS/N1
7008	3198 010 42310	BC847BW
7008	3198 010 42320	BC857BW
7009	3198 010 42310	BC847BW
7009	3198 010 42320	BC857BW
7010	3198 010 42310	BC847BW
7010	4822 130 61553	DTC124EU
7011	3198 010 42320	BC857BW
7301	4822 209 14933	TL431Z
7302	4822 130 11	

DVIO Board

Various

1400	2422 543 01115	24.576MHz 12P QS06
1500	2422 025 17084	Connector 4P m h 2.00 SMD CON BM V 60P F 0.80 179161 R
1501	2422 025 16543	Connector 4P m h 2.00 SMD
1502	2422 086 11075	FUSE 750mA 125V
1800	2422 543 89022	Crystal 6MHz 20pF CX5F
1901	2422 025 17106	CON BM H 4P F 0.8 IEEE R
1903	2422 025 16542	CON BM H 2P M 2.00 PH SMD R

2400	2238 586 59812	100nF 20-80% 50V 0603
2401	3198 017 41050	1µF 10V 0603
2402	4822 126 14506	270pF 5% 50V 0603
2403	4822 124 80151	47µF 20% 16V
2404	2238 586 59812	100nF 20-80% 50V 0603
2405	2238 586 59812	100nF 20-80% 50V 0603
2406	2238 586 59812	100nF 20-80% 50V 0603
2407	2238 586 59812	100nF 20-80% 50V 0603
2408	2238 586 59812	100nF 20-80% 50V 0603
2412	4822 122 33741	10pF 10% 50V
2413	4822 122 33741	10pF 10% 50V
2415	4822 124 80151	47µF 20% 16V
2416	2238 586 59812	100nF 20-80% 50V 0603
2417	2238 586 59812	100nF 20-80% 50V 0603
2418	2238 586 59812	100nF 20-80% 50V 0603
2419	2238 586 59812	100nF 20-80% 50V 0603
2420	2238 586 59812	100nF 20-80% 50V 0603
2431	4822 124 80151	47µF 20% 16V
2432	2238 586 59812	100nF 20-80% 50V 0603
2433	2238 586 59812	100nF 20-80% 50V 0603
2434	2238 586 59812	100nF 20-80% 50V 0603
2435	2238 586 59812	100nF 20-80% 50V 0603
2436	2238 586 59812	100nF 20-80% 50V 0603
2437	2238 586 59812	100nF 20-80% 50V 0603
2438	2238 586 59812	100nF 20-80% 50V 0603
2439	2238 586 59812	100nF 20-80% 50V 0603
2440	2238 586 59812	100nF 20-80% 50V 0603
2441	2238 586 59812	100nF 20-80% 50V 0603
2442	2238 586 59812	100nF 20-80% 50V 0603
2443	2238 586 59812	100nF 20-80% 50V 0603
2444	2238 586 59812	100nF 20-80% 50V 0603
2445	2238 586 59812	100nF 20-80% 50V 0603
2446	2238 586 59812	100nF 20-80% 50V 0603
2447	2238 586 59812	100nF 20-80% 50V 0603
2449	2238 586 59812	100nF 20-80% 50V 0603
2450	4822 124 23002	10µF 20% 16V
2451	2238 586 59812	100nF 20-80% 50V 0603
2452	2238 586 59812	100nF 20-80% 50V 0603
2453	2238 586 59812	100nF 20-80% 50V 0603
2454	2238 586 59812	100nF 20-80% 50V 0603
2455	2238 586 59812	100nF 20-80% 50V 0603
2456	2238 586 59812	100nF 20-80% 50V 0603
2501	2238 586 59812	100nF 20-80% 50V 0603
2502	2238 586 59812	100nF 20-80% 50V 0603
2503	2238 586 59812	100nF 20-80% 50V 0603
2504	2238 586 59812	100nF 20-80% 50V 0603
2505	2238 586 59812	100nF 20-80% 50V 0603
2506	4822 124 80151	47µF 20% 16V
2507	4822 124 80151	47µF 20% 16V
2508	2238 586 59812	100nF 20-80% 50V 0603
2512	2238 586 59812	100nF 20-80% 50V 0603
2513	2238 586 59812	100nF 20-80% 50V 0603
2514	4822 124 80151	47µF 20% 16V
2520	2238 586 59812	100nF 20-80% 50V 0603
2521	4822 124 80151	47µF 20% 16V
2522	4822 124 80151	47µF 20% 16V
2523	5322 126 11583	10nF 10% 50V 0603
2524	5322 126 11583	10nF 10% 50V 0603
2525	4822 124 80151	47µF 20% 16V
2526	2238 586 59812	100nF 20-80% 50V 0603
2527	2238 586 59812	100nF 20-80% 50V 0603
2528	2238 586 59812	100nF 20-80% 50V 0603
2529	2238 586 59812	100nF 20-80% 50V 0603
2534	2238 586 59812	100nF 20-80% 50V 0603
2600	2238 586 59812	100nF 20-80% 50V 0603
2601	4822 124 23002	10µF 20% 16V
2602	3198 017 44740	470nF 10V 0603
2603	2238 586 59812	100nF 20-80% 50V 0603
2605	2238 586 59812	100nF 20-80% 50V 0603
2606	3198 016 31020	1nF 10% 25V 0603
2607	2238 586 59812	100nF 20-80% 50V 0603
2608	2238 586 59812	100nF 20-80% 50V 0603
2609	2238 586 59812	100nF 20-80% 50V 0603
2610	2238 586 59812	100nF 20-80% 50V 0603
2611	2238 586 59812	100nF 20-80% 50V 0603

2612	2238 586 59812	100nF 20-80% 50V 0603
2613	2238 586 59812	100nF 20-80% 50V 0603
2614	3198 017 44740	470nF 10V 0603
2617	2238 586 59812	100nF 20-80% 50V 0603
2618	2238 861 18229	22pF 1% 50V 0805
2801	4822 126 11669	27pF 5% 50V 0603
2802	4822 126 11669	27pF 5% 50V 0603
2803	2238 586 59812	100nF 20-80% 50V 0603
2804	2238 586 59812	100nF 20-80% 50V 0603
2805	4822 124 80151	47µF 20% 16V
2806	2238 586 59812	100nF 20-80% 50V 0603
2807	4822 124 80151	47µF 20% 16V
2808	2238 586 59812	100nF 20-80% 50V 0603
2809	2238 586 59812	100nF 20-80% 50V 0603
2810	2238 586 59812	100nF 20-80% 50V 0603
2812	2238 586 59812	100nF 20-80% 50V 0603
2813	2238 586 59812	100nF 20-80% 50V 0603
2814	5322 124 41945	22µF 20% 35V SMD
2816	2238 586 59812	100nF 20-80% 50V 0603
2818	2238 586 59812	100nF 20-80% 50V 0603
2820	2238 586 59812	100nF 20-80% 50V 0603
2822	3198 016 31020	1nF 10% 25V 0603

---W---

3400	4822 051 30103	10kΩ 5% 0.062W
3401	2322 734 65609	56Ω 1% 0.125W 0805
3402	2322 734 65609	56Ω 1% 0.125W 0805
3403	4822 117 12139	22Ω 5% 0.062W
3404	2322 734 65609	56Ω 1% 0.125W 0805
3405	2322 734 65609	56Ω 1% 0.125W 0805
3406	2322 704 65102	5.1kΩ 1% 0603
3407	4822 051 30103	10kΩ 5% 0.062W
3408	4822 117 13632	100kΩ 1% 0603 0.62W
3409	2350 546 09102	9.1kΩ 0603 RC23H 5%
3409	4822 117 12902	8.2kΩ 1% 0.063W 0603
3410	4822 117 12139	22Ω 5% 0.062W
3413	4822 117 12139	22Ω 5% 0.062W
3414	4822 117 12139	22Ω 5% 0.062W
3415	4822 117 12139	22Ω 5% 0.062W
3416	4822 117 12139	22Ω 5% 0.062W
3417	4822 117 12139	22Ω 5% 0.062W
3418	4822 117 12139	22Ω 5% 0.062W
3419	4822 117 12139	22Ω 5% 0.062W
3420	4822 117 12139	22Ω 5% 0.062W
3421	4822 117 12139	22Ω 5% 0.062W
3422	4822 117 12139	22Ω 5% 0.062W
3423	4822 117 12139	22Ω 5% 0.062W
3424	4822 117 12139	22Ω 5% 0.062W
3425	4822 051 30103	10kΩ 5% 0.062W
3426	4822 051 30103	10kΩ 5% 0.062W
3427	4822 051 30103	10kΩ 5% 0.062W
3428	4822 051 30103	10kΩ 5% 0.062W
3429	4822 051 30103	10kΩ 5% 0.062W
3430	4822 051 30103	10kΩ 5% 0.062W
3431	4822 051 30103	10kΩ 5% 0.062W
3432	4822 051 30103	10kΩ 5% 0.062W
3433	4822 051 30103	10kΩ 5% 0.062W
3434	4822 051 30103	10kΩ 5% 0.062W
3435	4822 051 30103	10kΩ 5% 0.062W
3436	4822 051 30103	10kΩ 5% 0.062W
3437	4822 051 30103	10kΩ 5% 0.062W
3438	4822 051 30103	10kΩ 5% 0.062W
3439	4822 051 30103	10kΩ 5% 0.062W
3440	4822 051 30103	10kΩ 5% 0.062W
3441	4822 051 30103	10kΩ 5% 0.062W
3442	4822 051 30103	10kΩ 5% 0.062W
3443	4822 051 30103	10kΩ 5% 0.062W
3444	4822 051 30103	10kΩ 5% 0.062W
3445	4822 051 30103	10kΩ 5% 0.062W
3446	4822 051 30103	10kΩ 5% 0.062W
3447	4822 051 30103	10kΩ 5% 0.062W
3448	4822 051 30103	10kΩ 5% 0.062W
3449	4822 051 30103	10kΩ 5% 0.062W
3450	4822 051 30103	10kΩ 5% 0.062W
3451	4822 051 30103	10kΩ 5% 0.062W
3452	4822 051 30103	10kΩ 5% 0.062W
3453	4822 051 30102	1kΩ 5% 0.062W
3454	4822 051 30103	10kΩ 5% 0.062W
3455	4822 051 30103	10kΩ 5% 0.062W
3456	4822 051 30103	10kΩ 5% 0.062W
3457	4822 051 30103	10kΩ 5% 0.062W
3458	4822 051 30103	10kΩ 5% 0.062W
3459	4822 051 30103	10kΩ 5% 0.062W
3460	4822 051 30103	10kΩ 5% 0.062W
3461	4822 117 12925	47kΩ 1% 0.063W 0603
3462	4822 051 30103	10kΩ 5% 0.062W
3463	4822 051 30103	10kΩ 5% 0.062W
3464	4822 051 30103	10kΩ 5% 0.062W
3465	4822 051 30103	10kΩ 5% 0.062W
3466	4822 051 30103	10kΩ 5% 0.062W
3467	4822 051 30103	10kΩ 5% 0.062W
3468	4822 051 30103	10kΩ 5% 0.062W

3469	4822 051 30103	10kΩ 5% 0.062W
3470	4822 051 30103	10kΩ 5% 0.062W
3471	4822 051 30103	10kΩ 5% 0.062W
3472	4822 051 30102	1kΩ 5% 0.062W
3473	4822 051 30103	10kΩ 5% 0.062W
3474	4822 051 30102	1kΩ 5% 0.062W
3475	4822 051 30103	10kΩ 5% 0.062W
3476	4822 051 30103	10kΩ 5% 0.062W
3477	4822 051 30103	10kΩ 5% 0.062W
3478	4822 051 30102	1kΩ 5% 0.062W
3481	4822 051 30103	10kΩ 5% 0.062W
3482	4822 051 30103	10kΩ 5% 0.062W
3483	4822 051 30103	10kΩ 5% 0.062W
3484	4822 051 30103	10kΩ 5% 0.062W
3485	4822 051 30103	10kΩ 5% 0.062W
3486	4822 051 30103	10kΩ 5% 0.062W
3487	4822 051 30103	10kΩ 5% 0.062W
3488	4822 051 30103	10kΩ 5% 0.062W
3489	4822 051 30103	10kΩ 5% 0.062W
3490	4822 051 30103	10kΩ 5% 0.062W
3491	4822 051 30103	10kΩ 5% 0.062W
3492	4822 051 30103	10kΩ 5% 0.062W
3493	4822 051 30103	10kΩ 5% 0.062W
3494	4822 051 30103	10kΩ 5% 0.062W
3495	4822 051 30103	10kΩ 5% 0.062W
3496	4822 051 30103	10kΩ 5% 0.062W
3497	4822 051 30103	10kΩ 5% 0.062W
3498	4822 051 30103	10kΩ 5% 0.062W
3499	4822 051 30103	10kΩ 5% 0.062W
3502	4822 051 30479	47Ω 5% 0.062W
3503	4822 051 30479	47Ω 5% 0.062W
3504	4822 051 30479	47Ω 5% 0.062W
3505	4822 051 30479	47Ω 5% 0.062W
3506	4822 051 30479	47Ω 5% 0.062W
3507	4822 051 30479	47Ω 5% 0.062W
3508	4822 051 30479	47Ω 5% 0.062W
3509	4822 051 30479	47Ω 5% 0.062W
3510	4822 051 30479	47Ω 5% 0.062W
3514	4822 051 30479	47Ω 5% 0.062W
3515	4822 051 30479	47Ω 5% 0.062W
3516	4822 051 30479	47Ω 5% 0.062W
3517	4822 051 30101	100Ω 5% 0.062W
3518	4822 051 30101	100Ω 5% 0.062W
3519	4822 117 12891	220kΩ 1% 0.063W 0603
3520	4822 117 12891	220kΩ 1% 0.063W 0603
3530	4822 117 12139	22Ω 5% 0.062W
3531	4822 117 12139	22Ω 5% 0.062W
3532	4822 117 12139	

3617	4822 051 30103	10kΩ 5% 0.062W
3618	4822 051 30103	10kΩ 5% 0.062W
3800	4822 051 30331	330Ω 5% 0.062W
3801	4822 051 30103	10kΩ 5% 0.062W
3802	4822 051 30223	22kΩ 5% 0.062W
3803	4822 051 30103	10kΩ 5% 0.062W
3804	4822 051 30103	10kΩ 5% 0.062W
3806	4822 051 30103	10kΩ 5% 0.062W
3807	4822 051 30103	10kΩ 5% 0.062W
3808	4822 051 30008	Jumper 0603
3809	4822 051 30103	10kΩ 5% 0.062W
3810	4822 051 30103	10kΩ 5% 0.062W
3812	4822 051 30103	10kΩ 5% 0.062W
3814	4822 051 30472	4.7kΩ 5% 0.062W
3815	5322 117 13047	330Ω 1% 0.063W 0603
3816	5322 117 13018	1kΩ 1% 0.063W 0603
3817	4822 051 30103	10kΩ 5% 0.062W
3818	4822 051 30103	10kΩ 5% 0.062W
3819	4822 051 30102	1kΩ 5% 0.062W
3820	4822 117 12925	47kΩ 1% 0.063W 0603
3821	4822 051 30103	10kΩ 5% 0.062W
3822	4822 117 13632	100kΩ 1% 0.063W 0.62W
3823	5322 117 13018	1kΩ 1% 0.063W 0603
3824	5322 117 13042	3.9kΩ 1% 0.063W 0603
3825	4822 051 30101	100Ω 5% 0.062W
3826	4822 051 30101	100Ω 5% 0.062W
3827	4822 051 30103	10kΩ 5% 0.062W
3828	4822 051 30101	100Ω 5% 0.062W
3829	4822 117 12925	47kΩ 1% 0.063W 0603
3831	4822 117 13632	100kΩ 1% 0.063W 0.62W
3832	4822 051 30103	10kΩ 5% 0.062W
3833	4822 051 30103	10kΩ 5% 0.062W
3834	4822 051 30103	10kΩ 5% 0.062W
3835	4822 051 30102	1kΩ 5% 0.062W
3836	4822 051 30472	4.7kΩ 5% 0.062W
3837	4822 051 30103	10kΩ 5% 0.062W
3838	4822 051 30102	1kΩ 5% 0.062W
3839	4822 051 30222	2.2kΩ 5% 0.062W
4401	4822 051 30008	Jumper 0603
4402	4822 051 30008	Jumper 0603
4501	4822 051 30008	Jumper 0603
4503	4822 051 30008	Jumper 0603
4602	4822 051 30008	Jumper 0603
4603	4822 051 30008	Jumper 0603
4605	4822 051 30008	Jumper 0603
4606	4822 051 30008	Jumper 0603
4608	4822 051 30008	Jumper 0603
4609	4822 051 30008	Jumper 0603

5400	4822 157 11499	BLM11P600SPT
5401	4822 157 11499	BLM11P600SPT
5431	4822 157 11499	BLM11P600SPT
5432	4822 157 11499	BLM11P600SPT
5433	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT
5504	4822 157 11499	BLM11P600SPT
5505	4822 157 11499	BLM11P600SPT
5600	4822 157 11499	BLM11P600SPT
5601	4822 157 11499	BLM11P600SPT
5602	4822 157 11499	BLM11P600SPT
5603	4822 157 11499	BLM11P600SPT
5800	4822 157 11499	BLM11P600SPT
5801	4822 157 11499	BLM11P600SPT
5802	4822 157 71593	10μH 10% 0805



6801	9340 548 52115	PDZ5.1B
6802	4822 130 11397	BAS316
6803	4822 130 11397	BAS316
6804	4822 130 11397	BAS316



7400	9322 182 04671	UPD72852GB-8EU
7430	9322 144 59668	MT48LC1M16A1TG-7S
7431	9322 184 70671	UPD72893GD-LML
7433	9322 142 88668	LF25CDT
7501	9352 685 96115	74LVC1GU04GW
7505	9352 029 90118	74LVT16244BDGG
7506	9352 668 39118	UDA1334ATS/N2
7507	9351 751 40118	74LV74PW
7508	9352 685 96115	74LVC1GU04GW
7601	2722 171 08709	27MHZ 120P FXO-31
7602	9352 456 40115	74HCT1G04GW
7604	9322 186 60668	BA7082F
7605	9322 186 59668	BU2288FV
7606	9351 751 40118	74LV74PW
7608	9352 685 96115	74LVC1GU04GW

7800	9340 310 30215	PDTC144ET
7801	9322 186 70668	LM2931D
7802	3103 607 40011	UPD78F0988AGC
		DV91XX0105
7803	3198 010 42310	BC847BW
7804	3198 010 42310	BC847BW
7805	3198 010 42310	BC847BW
7806	9340 310 30215	PDTC144ET
7807	9352 683 81115	74LVC1G32GW
7808	9340 560 36235	BSH111
7809	9352 683 81115	74LVC1G32GW
7810	3198 010 42320	BC857BW
7811	3198 010 42310	BC847BW

Digital Board 1.5 (Empress)

Various

1100	2422 025 17018	V 15P F 1.00 FFC 0.3 R
1101	2422 025 17018	V 15P F 1.00 FFC 0.3 R
1200	2422 025 16794	V 7P F 1.00 FFC 0.3 R
1500	2422 543 01115	24.576MHz 12P QS06
1600	2422 025 16729	Connector FFC 10p m
1601	2422 025 16389	BM V 22P F 1.00 FFC 0.3 R
1602	2422 025 16389	BM V 22P F 1.00 FFC 0.3 R
1603	2422 025 16939	BM V 60P F 0.80 84616 R
1900	2422 025 17441	BM V 12P M 2.00 PH SMD R

2100	2238 586 59812	100nF 20-80% 50V 0603
2101	2238 586 59812	100nF 20-80% 50V 0603
2102	2238 586 59812	100nF 20-80% 50V 0603
2103	2238 586 59812	100nF 20-80% 50V 0603
2104	2238 586 59812	100nF 20-80% 50V 0603
2105	2238 586 59812	100nF 20-80% 50V 0603
2106	2238 586 59812	100nF 20-80% 50V 0603
2107	2238 586 59812	100nF 20-80% 50V 0603
2108	2238 586 59812	100nF 20-80% 50V 0603
2109	2238 586 59812	100nF 20-80% 50V 0603
2110	2238 586 59812	100nF 20-80% 50V 0603
2111	2238 586 59812	100nF 20-80% 50V 0603
2112	2238 586 59812	100nF 20-80% 50V 0603
2113	2238 586 59812	100nF 20-80% 50V 0603
2114	2238 586 59812	100nF 20-80% 50V 0603
2115	2238 586 59812	100nF 20-80% 50V 0603
2116	2238 586 59812	100nF 20-80% 50V 0603
2117	2238 586 59812	100nF 20-80% 50V 0603
2118	2238 586 59812	100nF 20-80% 50V 0603
2119	3198 030 74780	4u7 20% 35V
2120	2238 586 59812	100nF 20-80% 50V 0603
2121	2238 586 59812	100nF 20-80% 50V 0603
2122	2238 586 59812	100nF 20-80% 50V 0603
2123	2238 586 59812	100nF 20-80% 50V 0603
2124	2238 586 59812	100nF 20-80% 50V 0603
2125	2238 586 59812	100nF 20-80% 50V 0603
2126	2238 586 59812	100nF 20-80% 50V 0603
2127	3198 030 74780	4u7 20% 35V
2128	3198 016 31020	1nF 10% 25V 0603
2129	2222 867 15339	33pF 5% 50V 0603
2129	4822 126 13956	68pF 5% 63V 0603
2130	3198 030 82280	2.2μF 10% 25V 0603
2131	3198 030 74780	4u7 20% 35V
2131	5322 124 41945	22μF 20% 35V SMD
2132	2238 586 59812	100nF 20-80% 50V 0603
2135	3198 030 74780	4u7 20% 35V
2136	4822 126 11785	47pF 5% 50V 0603
2137	2238 586 59812	100nF 20-80% 50V 0603
2139	2238 586 59812	100nF 20-80% 50V 0603
2141	4822 126 11785	47pF 5% 50V 0603
2146	2238 586 59812	100nF 20-80% 50V 0603
2154	4822 126 13879	220nF 20% 16V
2200	3198 016 31020	1nF 10% 25V 0603
2201	4822 126 14494	22nF 10% 25V 0603
2202	2238 586 59812	100nF 20-80% 50V 0603
2203	3198 030 74780	4u7 20% 35V
2204	2222 867 15339	33pF 5% 50V 0603
2205	2238 586 59812	100nF 20-80% 50V 0603
2206	2238 586 59812	100nF 20-80% 50V 0603
2207	2222 867 15339	33pF 5% 50V 0603
2208	2238 586 59812	100nF 20-80% 50V 0603
2209	2238 586 59812	100nF 20-80% 50V 0603
2210	2238 586 59812	100nF 20-80% 50V 0603
2211	2238 586 59812	100nF 20-80% 50V 0603
2212	2238 586 59812	100nF 20-80% 50V 0603
2213	2238 586 59812	100nF 20-80% 50V 0603
2214	2238 586 59812	100nF 20-80% 50V 0603
2215	2238 586 59812	100nF 20-80% 50V 0603
2216	2238 586 59812	100nF 20-80% 50V 0603
2217	2238 586 59812	100nF 20-80% 50V 0603
2218	3198 030 74780	4u7 20% 35V

2219	2238 586 59812	100nF 20-80% 50V 0603
2220	2238 586 59812	100nF 20-80% 50V 0603
2221	2238 586 59812	100nF 20-80% 50V 0603
2222	2238 586 59812	100nF 20-80% 50V 0603
2223	2238 586 59812	100nF 20-80% 50V 0603
2224	2238 586 59812	100nF 20-80% 50V 0603
2225	2238 586 59812	100nF 20-80% 50V 0603
2226	2238 586 59812	100nF 20-80% 50V 0603
2227	2238 586 59812	100nF 20-80% 50V 0603
2228	2238 586 59812	100nF 20-80% 50V 0603
2229	2238 586 59812	100nF 20-80% 50V 0603
2230	3198 030 74780	4u7 20% 35V
2231	2238 586 59812	100nF 20-80% 50V 0603
2300	2238 586 59812	100nF 20-80% 50V 0603
2301	2238 586 59812	100nF 20-80% 50V 0603
2302	2238 586 59812	100nF 20-80% 50V 0603
2303	2238 586 59812	100nF 20-80% 50V 0603
2304	3198 030 74780	4u7 20% 35V
2305	3198 030 74780	4u7 20% 35V
2306	2238 586 59812	100nF 20-80% 50V 0603
2307	2238 586 59812	100nF 20-80% 50V 0603
2308	2238 586 59812	100nF 20-80% 50V 0603
2309	2238 586 59812	100nF 20-80% 50V 0603
2310	2238 586 59812	100nF 20-80% 50V 0603
2311	3198 030 74780	4u7 20% 35V
2312	2238 586 59812	100nF 20-80% 50V 0603
2402	2238 586 59812	100nF 20-80% 50V 0603
2403	3198 030 74780	4u7 20% 35V
2404	2238 586 59812	100nF 20-80% 50V 0603
2405	2238 586 59812	100nF 20-80% 50V 0603
2406	2238 586 59812	100nF 20-80% 50V 0603
2407	2238 586 59812	100nF 20-80% 50V 0603
2408	2238 586 59812	100nF 20-80% 50V 0603
2409	2238 586 59812	100nF 20-80% 50V 0603
2410	2238 586 59812	100nF 20-80% 50V 0603
2411	3198 030 74780	4u7 20% 35V
2412	2238 586 59812	100nF 20-80% 50V 0603
2413	2238 586 59812	100nF 20-80% 50V 0603
2414	2238 586 59812	100nF 20-80% 50V 0603
2415	2238 586 59812	100nF 20-80% 50V 0603
2416	2238 586 59812	100nF 20-80% 50V 0603
2417	2238 586 59812	100nF 20-80% 50V 0603
2418	2238 586 59812	100nF 20-80% 50V 0603
2419	2238 586 59812	100nF 20-80% 50V 0603
2420	2238 586 59812	100nF 20-80% 50V 0603
2421	2238 586 59812	100nF 20-80% 50V 0603
2422	2238 586 59812	100nF 20-80% 50V 0603
2423	2238 586 59812	100nF 20-80% 50V 0603
2424	2238 586 59812	100nF 20-80% 50V 0603
2425	2238 586 59812	100nF 20-80% 50V 0603
2426	2238 586 59812	100nF 20-80% 50V 0603
2427	2238 586 59812	100nF 20-80% 50V 0603
2428	2238 586 59812	100nF 20-80% 50V 0603
2429	2238 586 59812	100nF 20-80% 50V 0603
243		

2522	2238 586 59812	100nF 20-80% 50V 0603	3119	4822 051 30222	2.2kΩ 5% 0.062W	3607	5322 117 13059	560Ω 1% 0.063W 0603
2523	2238 586 59812	100nF 20-80% 50V 0603	3120	4822 051 30153	15kΩ 5% 0.062W	3608	4822 051 30102	1kΩ 5% 0.062W
2524	2238 586 59812	100nF 20-80% 50V 0603	3121	4822 117 12917	1Ω 5% 0.062W 0603	3610	4822 117 12917	1Ω 5% 0.062W 0603
2525	2238 586 59812	100nF 20-80% 50V 0603	3122	4822 051 30123	12kΩ 5% 0.062W	3611	5322 117 13059	560Ω 1% 0.063W 0603
2526	2238 586 59812	100nF 20-80% 50V 0603	3122	5322 117 13033	15kΩ 1% 0.063W 0603	3612	5322 117 13059	560Ω 1% 0.063W 0603
2527	2238 586 59812	100nF 20-80% 50V 0603	3123	2322 704 61103	11kΩ 0603 RC22H 1%	3613	4822 051 30102	1kΩ 5% 0.062W
2528	2238 586 59812	100nF 20-80% 50V 0603	3123	2322 704 62002	22kΩ 1% 0603	3615	4822 051 30101	100Ω 5% 0.062W
2529	2238 586 59812	100nF 20-80% 50V 0603	3124	2322 704 63002	3kΩ 1% 0603	3616	5322 117 13059	560Ω 1% 0.063W 0603
2530	2238 586 59812	100nF 20-80% 50V 0603	3124	4822 051 30562	5.6kΩ 5% 0.063W 0603	3617	5322 117 13059	560Ω 1% 0.063W 0603
2531	2238 586 59812	100nF 20-80% 50V 0603	3125	4822 117 12139	2.2kΩ 5% 0.062W	3618	4822 051 30102	1kΩ 5% 0.062W
2532	2238 586 59812	100nF 20-80% 50V 0603	3126	4822 117 12891	220kΩ 1% 0.063W 0603	3619	4822 051 30561	560Ω 5% 0.062W
2533	2238 586 59812	100nF 20-80% 50V 0603	3127	4822 051 30479	47Ω 5% 0.062W	3620	4822 051 30222	2.2kΩ 5% 0.062W
2534	2238 586 59812	100nF 20-80% 50V 0603	3128	4822 051 30479	47Ω 5% 0.062W	3621	5322 117 13059	560Ω 1% 0.063W 0603
2535	2238 586 59812	100nF 20-80% 50V 0603	3129	4822 051 30479	47Ω 5% 0.062W	3622	5322 117 13059	560Ω 1% 0.063W 0603
2536	2238 586 59812	100nF 20-80% 50V 0603	3130	2120 611 00019	4.7kΩ NTC 0603 0.1W 5%	3623	4822 051 30101	100Ω 5% 0.062W
2537	2238 586 59812	100nF 20-80% 50V 0603	3131	4822 117 12917	1Ω 5% 0.062W 0603	3624	4822 051 30102	1kΩ 5% 0.062W
2538	2238 586 59812	100nF 20-80% 50V 0603	3132	4822 117 12917	1Ω 5% 0.062W 0603	3625	4822 051 30101	100Ω 5% 0.062W
2539	3198 030 74780	4u7 20% 35V	3133	4822 117 12917	1Ω 5% 0.062W 0603	3626	5322 117 13059	560Ω 1% 0.063W 0603
2540	3198 030 74780	4u7 20% 35V	3134	4822 117 12917	1Ω 5% 0.062W 0603	3627	5322 117 13059	560Ω 1% 0.063W 0603
2541	3198 030 74780	4u7 20% 35V	3135	4822 117 12917	1Ω 5% 0.062W 0603	3628	4822 051 30102	1kΩ 5% 0.062W
2542	3198 030 74780	4u7 20% 35V	3136	4822 117 12917	1Ω 5% 0.062W 0603	3629	4822 051 30181	180Ω 5% 0.062W
2543	2238 586 59812	100nF 20-80% 50V 0603	3137	4822 051 30472	4.7kΩ 5% 0.062W	3630	4822 051 30181	180Ω 5% 0.062W
2544	2238 586 59812	100nF 20-80% 50V 0603	3138	4822 051 30472	4.7kΩ 5% 0.062W	3631	4822 117 12917	1Ω 5% 0.062W 0603
2565	4822 122 33753	150pF 5% 50V	3200	4822 051 30332	3.3kΩ 5% 0.062W	3632	4822 051 30561	560Ω 5% 0.062W
2600	2238 586 59812	100nF 20-80% 50V 0603	3201	4822 051 30152	1.5kΩ 5% 0.062W	3633	4822 051 30561	560Ω 5% 0.062W
2601	4822 126 11785	47pF 5% 50V 0603	3202	4822 051 30103	10kΩ 5% 0.062W	3635	4822 051 30101	100Ω 5% 0.062W
2602	4822 126 11785	47pF 5% 50V 0603	3203	4822 117 12139	22Ω 5% 0.062W	3636	4822 051 30181	180Ω 5% 0.062W
2605	2238 586 59812	100nF 20-80% 50V 0603	3204	4822 051 30103	100Ω 5% 0.062W	3637	4822 051 30101	100Ω 5% 0.062W
2606	4822 126 11785	47pF 5% 50V 0603	3205	4822 051 30101	100Ω 5% 0.062W	3638	4822 051 30222	2.2kΩ 5% 0.062W
2607	4822 126 11785	47pF 5% 50V 0603	3206	4822 051 30101	100Ω 5% 0.062W	3639	4822 051 20008	Jumper 0805
2608	2238 586 59812	100nF 20-80% 50V 0603	3207	4822 051 30103	10kΩ 5% 0.062W	3639	4822 051 30008	Jumper 0603
2609	2238 586 59812	100nF 20-80% 50V 0603	3208	4822 117 12139	22Ω 5% 0.062W	3900	4822 051 30103	10kΩ 5% 0.062W
2610	2238 586 59812	100nF 20-80% 50V 0603	3209	4822 051 30103	10kΩ 5% 0.062W	3901	4822 117 12139	22Ω 5% 0.062W
2611	4822 126 11785	47pF 5% 50V 0603	3211	4822 051 30222	2.2kΩ 5% 0.062W	3902	4822 051 30472	4.7kΩ 5% 0.062W
2612	4822 126 11785	47pF 5% 50V 0603	3212	4822 051 30152	1.5kΩ 5% 0.062W	3902	4822 117 12925	47kΩ 1% 0.063W 0603
2613	2238 586 59812	100nF 20-80% 50V 0603	3213	4822 051 30103	10kΩ 5% 0.062W	3903	4822 051 30472	4.7kΩ 5% 0.062W
2614	2238 586 59812	100nF 20-80% 50V 0603	3214	4822 051 30103	10kΩ 5% 0.062W	3903	4822 117 13632	100kΩ 1% 0603 0.62W
2615	2238 586 59812	100nF 20-80% 50V 0603	3215	4822 051 30103	10kΩ 5% 0.062W	3904	4822 117 12139	22Ω 5% 0.062W
2616	4822 126 11785	47pF 5% 50V 0603	3216	4822 051 30103	10kΩ 5% 0.062W	3906	4822 051 30479	47Ω 5% 0.062W
2617	4822 126 11785	47pF 5% 50V 0603	3217	4822 051 30101	100Ω 5% 0.062W	3908	4822 117 12139	22Ω 5% 0.062W
2618	2238 586 59812	100nF 20-80% 50V 0603	3218	4822 051 30101	100Ω 5% 0.062W	3910	4822 051 30101	100Ω 5% 0.062W
2619	2238 586 59812	100nF 20-80% 50V 0603	3219	4822 051 30103	10kΩ 5% 0.062W	3911	4822 051 30103	10kΩ 5% 0.062W
2620	2238 586 59812	100nF 20-80% 50V 0603	3220	4822 051 30103	10kΩ 5% 0.062W	3913	4822 051 30682	6.8kΩ 5% 0.062W
2621	4822 126 11785	47pF 5% 50V 0603	3221	4822 051 30103	10kΩ 5% 0.062W	3914	4822 051 30479	47Ω 5% 0.062W
2622	4822 126 11785	47pF 5% 50V 0603	3222	4822 051 30103	10kΩ 5% 0.062W	3915	4822 051 30479	47Ω 5% 0.062W
2625	2238 586 59812	100nF 20-80% 50V 0603	3223	4822 051 30222	2.2kΩ 5% 0.062W	3916	4822 117 13632	100kΩ 1% 0603 0.62W
2626	4822 126 11785	47pF 5% 50V 0603	3224	4822 051 30103	10kΩ 5% 0.062W	3917	4822 117 12139	22Ω 5% 0.062W
2627	4822 126 11785	47pF 5% 50V 0603	3225	4822 051 30103	10kΩ 5% 0.062W	3918	4822 117 13632	100kΩ 1% 0603 0.62W
2628	2238 586 59812	100nF 20-80% 50V 0603	3226	4822 051 30103	10kΩ 5% 0.062W	3919	4822 051 30101	100Ω 5% 0.062W
2629	2238 586 59812	100nF 20-80% 50V 0603	3227	4822 117 12139	22Ω 5% 0.062W	3920	4822 117 12139	22Ω 5% 0.062W
2630	3198 030 74780	4u7 20% 35V	3228	4822 117 12139	22Ω 5% 0.062W	3921	4822 051 30103	10kΩ 5% 0.062W
2632	2238 586 59812	100nF 20-80% 50V 0603	3229	2322 704 61303	13kΩ 1% 0603	3922	4822 051 30682	6.8kΩ 5% 0.062W
2633	2238 586 59812	100nF 20-80% 50V 0603	3230	2322 704 61303	13kΩ 1% 0603	3923	4822 117 13632	100kΩ 1% 0603 0.62W
2634	4822 126 14494	22nF 10% 25V 0603	3231	5322 117 13042	3.9kΩ 1% 0.063W 0603	3924	4822 051 30152	1.5kΩ 5% 0.062W
2635	2238 586 59812	100nF 20-80% 50V 0603	3232	5322 117 13042	3.9kΩ 1% 0.063W 0603	3925	4822 051 30472	4.7kΩ 5% 0.062W
2636	3198 030 74780	4u7 20% 35V	3234	3198 031 14720	1206 4X4K7 PM5	4100	4822 051 30008	Jumper 0603
2722	2238 586 59812	100nF 20-80% 50V 0603	3235	4822 117 12917	1Ω 5% 0.062W 0603	4103	4822 051 30008	Jumper 0603
2900	2238 586 59812	100nF 20-80% 50V 0603	3236	4822 117 13576	NETW 4 X 33R 5% 1206	4104	4822 051 30008	Jumper 0603
2901	2238 586 59812	100nF 20-80% 50V 0603	3237	4822 117 13576	NETW 4 X 33R 5% 1206	4106	4822 051 30008	Jumper 0603
2902	2238 586 59812	100nF 20-80% 50V 0603	3239	4822 051 30103	10kΩ 5% 0.062W	4107	4822 051 30008	Jumper 0603
2903	2238 586 59812	100nF 20-80% 50V 0603	3241	4822 051 30103	10kΩ 5% 0.062W	4108	4822 051 30008	Jumper 0603
2904	2238 586 59812	100nF 20-80% 50V 0603	3243	4822 051 30103	10kΩ 5% 0.062W	4109	4822 051 30008	Jumper 0603
2906	2238 586 59812	100nF 20-80% 50V 0603	3244	4822 051 30103	10kΩ 5% 0.062W	4110	4822 051 30008	Jumper 0603
2907	3198 030 74780	4u7 20% 35V	3245	4822 051 30103	10kΩ 5% 0.062W	4111	4822 051 30008	Jumper 0603
2908	2238 586 59812	100nF 20-80% 50V 0603	3300	4822 051 30479	47Ω 5% 0.062W	4406	4822 051 30008	Jumper 0603
2909	4822 126 14247	1.5nF 50V 0603	3301	4822 051 30479	47Ω 5% 0.062W	4409	4822 051 30008	Jumper 0603
2911	2238 586 59812	100nF 20-80% 50V 0603	3400	4822 051 30101	100Ω 5% 0.062W	4501	4822 051 30008	Jumper 0603
2912	4822 126 14247	1.5nF 50V 0603	3401	4822 051 30101	100Ω 5% 0.062W			
2914	3198 030 74780	4u7 20% 35V	3403	4822 051 30103	10kΩ 5% 0.062W			
2915	2238 586 59812	100nF 20-80% 50V 0603	3404	4822 051 30008	Jumper 0603			
2916	4822 126 14494	22nF 10% 25V 0603	3405	4822 051 30332	3.3kΩ 5% 0.062W			
			3406	4822 051 30479	47Ω 5% 0.062W	5100	4822 157 11717	BLM31P500SPT
			3407	4822 051 30181	180Ω 5% 0.062W	5101	4822 157 11717	BLM31P500SPT
			3408	4822 117 12139	22Ω 5% 0.062W	5102	4822 157 11499	BLM11P600SPT
			3409	4822 117 12139	22Ω 5% 0.062W	5103	4822 157 11499	BLM11P600SPT
			3410	4822 117 12139	22Ω 5% 0.062W	5200	4822 157 11499	BLM11P600SPT
			3500	4822 051 30101	100Ω 5% 0.062W	5201	4822 157 11499	BLM11P600SPT
			3501	4822 051 30101	100Ω 5% 0.062W	5202	4822 157 11499	BLM11P600SPT
			3502	4822 051 30222	2.2kΩ 5% 0.062W	5203	4822 157 11499	BLM11P600SPT
			3503	4822 051 30102	1kΩ 5% 0.062W	5204	4822 157 11499	BLM11P600SPT
			3504	4822 051 30681	680Ω 5% 0.062W	5205	4822 157 11499	BLM11P600SPT
			3505	4822 117 12139	22Ω 5% 0.062W	5206	4822 157 11499	BLM11P600SPT
			3506	4822 051 30222	2.2kΩ 5% 0.062W	5207	4822 157 11499	BLM11P600SPT
			3507	4822 051 30472	4.7kΩ 5% 0.062W	5208	4822 157 11499	BLM11P600SPT
			3508	4822 051 30103	10kΩ 5% 0.062W	5209	4822 157 11499	BLM11P600SPT
			3513	4822 051 30681	680Ω 5% 0.062W	5300	4822 157 11499	BLM11P600SPT
			3515	4822 117 12917	1Ω 5% 0.062W 0603	5302	4822 157 11	

5503	4822 157 11499	BLM11P600SPT	2016	2238 586 59812	100nF 20-80% 50V 0603	2410	2238 586 59812	100nF 20-80% 50V 0603
5504	4822 157 11499	BLM11P600SPT	2017	2238 586 59812	100nF 20-80% 50V 0603	2411	2238 586 59812	100nF 20-80% 50V 0603
5505	4822 157 11499	BLM11P600SPT	2018	2238 586 59812	100nF 20-80% 50V 0603	2412	2238 586 59812	100nF 20-80% 50V 0603
5506	4822 157 11499	BLM11P600SPT	2019	2238 586 59812	100nF 20-80% 50V 0603	2413	2238 586 59812	100nF 20-80% 50V 0603
5507	4822 157 11499	BLM11P600SPT	2020	2238 586 59812	100nF 20-80% 50V 0603	2414	2238 586 59812	100nF 20-80% 50V 0603
5508	4822 157 11499	BLM11P600SPT	2021	2238 586 59812	100nF 20-80% 50V 0603	2415	2238 586 59812	100nF 20-80% 50V 0603
5600	4822 157 70651	12µH (NL322522T-120J)	2022	2020 021 91729	4.7µF 20% 35V	2416	2238 586 59812	100nF 20-80% 50V 0603
5601	4822 157 70651	12µH (NL322522T-120J)	2026	2238 586 59812	100nF 20-80% 50V 0603	2417	2238 586 59812	100nF 20-80% 50V 0603
5602	4822 157 70651	12µH (NL322522T-120J)	2027	2238 586 59812	100nF 20-80% 50V 0603	2418	4822 124 23002	10µF 20% 16V
5603	4822 157 70651	12µH (NL322522T-120J)	2028	2238 586 59812	100nF 20-80% 50V 0603	2419	2238 586 59812	100nF 20-80% 50V 0603
5604	4822 157 70651	12µH (NL322522T-120J)	2029	2238 586 59812	100nF 20-80% 50V 0603	2420	4822 124 23002	10µF 20% 16V
5605	4822 157 70651	12µH (NL322522T-120J)	2030	2238 586 59812	100nF 20-80% 50V 0603	2421	2238 586 59812	100nF 20-80% 50V 0603
5606	4822 157 70649	4.7µH (NL322522T-4R7J)	2031	2238 586 59812	100nF 20-80% 50V 0603	2422	2238 586 59812	100nF 20-80% 50V 0603
5607	4822 157 70649	4.7µH (NL322522T-4R7J)	2032	2238 586 59812	100nF 20-80% 50V 0603	2423	2238 586 59812	100nF 20-80% 50V 0603
5900	4822 157 11717	BLM31P500SPT	2033	2020 021 91729	4.7µF 20% 35V	2424	2238 586 59812	100nF 20-80% 50V 0603
5901	4822 157 11717	BLM31P500SPT	2035	2238 586 59812	100nF 20-80% 50V 0603	2425	2238 586 59812	100nF 20-80% 50V 0603
5903	4822 157 11499	BLM11P600SPT	2036	4822 126 14506	270pF 5% 50V 0603	2426	2238 586 59812	100nF 20-80% 50V 0603
5904	4822 157 11717	BLM31P500SPT	2037	2238 586 59812	100nF 20-80% 50V 0603	2427	2238 586 59812	100nF 20-80% 50V 0603
5905	4822 157 11499	BLM11P600SPT	2038	2238 586 59812	100nF 20-80% 50V 0603	2428	2238 586 59812	100nF 20-80% 50V 0603
5907	4822 157 11499	BLM11P600SPT	2039	2238 586 59812	100nF 20-80% 50V 0603	2429	2238 586 59812	100nF 20-80% 50V 0603
			2040	2238 586 59812	100nF 20-80% 50V 0603	2432	2238 586 59812	100nF 20-80% 50V 0603
			2041	2238 586 59812	100nF 20-80% 50V 0603	2433	2238 586 59812	100nF 20-80% 50V 0603
			2042	2238 586 59812	100nF 20-80% 50V 0603	2512	2020 001 90085	82µF 6V3 20%
			2043	2238 586 59812	100nF 20-80% 50V 0603	2512	2020 021 91672	100µF 6V3 20%
			2044	2020 021 91729	4.7µF 20% 35V	2512	2020 021 91857	100µF 6V3 20%
			2046	4822 122 33761	22pF 5% 50V	2514	2238 586 59812	100nF 20-80% 50V 0603
			2048	4822 122 33753	150pF 5% 50V	2515	3198 017 44740	470nF 10V 0603
			2049	2020 021 91729	4.7µF 20% 35V	2516	2020 001 90085	82µF 6V3 20%
			2050	2238 586 59812	100nF 20-80% 50V 0603	2516	2020 021 91672	100µF 6V3 20%
			2052	2238 586 59812	100nF 20-80% 50V 0603	2516	2020 021 91857	100µF 6V3 20%
			2053	2238 586 59812	100nF 20-80% 50V 0603	2518	2020 552 94427	100pF 5% 50V 0603
			2054	2238 586 59812	100nF 20-80% 50V 0603	2519	2238 586 59812	100nF 20-80% 50V 0603
			2056	2238 586 59812	100nF 20-80% 50V 0603	2521	2238 586 59812	100nF 20-80% 50V 0603
			2058	2238 586 59812	100nF 20-80% 50V 0603	2524	2238 586 59812	100nF 20-80% 50V 0603
			2059	4822 126 14507	18pF 5% 50V 0603	2525	2238 586 59812	100nF 20-80% 50V 0603
			2060	4822 126 14507	18pF 5% 50V 0603	2526	2238 586 59812	100nF 20-80% 50V 0603
			2061	2238 586 59812	100nF 20-80% 50V 0603	2527	5322 126 11583	10nF 10% 50V 0603
			2063	2238 586 59812	100nF 20-80% 50V 0603	2806	2238 586 59812	100nF 20-80% 50V 0603
			2064	2238 586 59812	100nF 20-80% 50V 0603	2807	2238 586 59812	100nF 20-80% 50V 0603
			2065	2238 586 59812	100nF 20-80% 50V 0603	2808	2238 586 59812	100nF 20-80% 50V 0603
			2066	3198 016 31020	1nF 10% 25V 0603	2809	2238 586 59812	100nF 20-80% 50V 0603
			2067	2238 586 59812	100nF 20-80% 50V 0603	2810	2238 586 59812	100nF 20-80% 50V 0603
			2071	2238 586 59812	100nF 20-80% 50V 0603	2811	2238 586 59812	100nF 20-80% 50V 0603
			2101	2238 916 15641	22nF 10% 25V 0603	2812	2238 586 59812	100nF 20-80% 50V 0603
			2103	2238 586 59812	100nF 20-80% 50V 0603	2820	2238 586 59812	100nF 20-80% 50V 0603
			2108	4822 126 14585	100nF 10% 50V	2821	2238 586 59812	100nF 20-80% 50V 0603
			2112	4822 126 14247	1.5nF 50V 0603	2822	2238 586 59812	100nF 20-80% 50V 0603
			2113	4822 126 13881	470pF 5% 50V	2823	2238 586 59812	100nF 20-80% 50V 0603
			2116	2238 586 59812	100nF 20-80% 50V 0603	2824	2238 586 59812	100nF 20-80% 50V 0603
			2119	4822 126 14247	1.5nF 50V 0603	2825	2238 586 59812	100nF 20-80% 50V 0603
			2120	2238 586 59812	100nF 20-80% 50V 0603	2826	2238 586 59812	100nF 20-80% 50V 0603
			2125	2238 586 59812	100nF 20-80% 50V 0603	2830	2238 586 59812	100nF 20-80% 50V 0603
			2200	3198 017 41050	1µF 10V 0603	2832	2238 586 59812	100nF 20-80% 50V 0603
			2201	4822 126 14506	270pF 5% 50V 0603	2833	2238 586 59812	100nF 20-80% 50V 0603
			2202	4822 126 11663	12pF 5% 50V 0603	2900	2238 586 59812	100nF 20-80% 50V 0603
			2203	4822 126 11663	12pF 5% 50V 0603	2901	2238 586 59812	100nF 20-80% 50V 0603
			2206	2238 586 59812	100nF 20-80% 50V 0603	2902	2238 586 59812	100nF 20-80% 50V 0603
			2207	2238 586 59812	100nF 20-80% 50V 0603	2903	2238 586 59812	100nF 20-80% 50V 0603
			2209	2238 586 59812	100nF 20-80% 50V 0603	2904	2238 586 59812	100nF 20-80% 50V 0603
			2210	2238 586 59812	100nF 20-80% 50V 0603	2905	2238 586 59812	100nF 20-80% 50V 0603
			2212	4822 124 12095	100µF 20% 16V	2906	2238 586 59812	100nF 20-80% 50V 0603
			2214	2238 586 59812	100nF 20-80% 50V 0603	2907	2238 586 59812	100nF 20-80% 50V 0603
			2215	2238 586 59812	100nF 20-80% 50V 0603	2908	2238 586 59812	100nF 20-80% 50V 0603
			2217	2238 586 59812	100nF 20-80% 50V 0603	2909	2238 586 59812	100nF 20-80% 50V 0603
			2218	2238 586 59812	100nF 20-80% 50V 0603	2910	4822 122 33761	22pF 5% 50V
			2219	2238 586 59812	100nF 20-80% 50V 0603	2911	2238 916 15641	22nF 10% 25V 0603
			2220	2238 586 59812	100nF 20-80% 50V 0603	2912	2238 586 59812	100nF 20-80% 50V 0603
			2221	2238 586 59812	100nF 20-80% 50V 0603	2913	2238 586 59812	100nF 20-80% 50V 0603
			2222	2238 586 59812	100nF 20-80% 50V 0603	2914	4822 126 14506	270pF 5% 50V 0603
			2223	2238 586 59812	100nF 20-80% 50V 0603	2915	4822 126 14506	270pF 5% 50V 0603
			2224	2238 586 59812	100nF 20-80% 50V 0603	2916	4822 126 14506	270pF 5% 50V 0603
			2225	2238 586 59812	100nF 20-80% 50V 0603	2917	4822 126 14506	270pF 5% 50V 0603
			2226	2238 586 59812	100nF 20-80% 50V 0603	2918	4822 122 33761	22pF 5% 50V
			2227	2238 586 59812	100nF 20-80% 50V 0603	2919	4822 122 33761	22pF 5% 50V
			2228	2238 586 59812	100nF 20-80% 50V 0603	2920	2238 586 59812	100nF 20-80% 50V 0603
			2229	2238 586 59812	100nF 20-80% 50V 0603	2921	4822 122 33761	22pF 5% 50V
			2230	2238 586 59812	100nF 20-80% 50V 0603	2922	4822 122 33761	22pF 5% 50V
			2231	2238 586 59812	100nF 20-80% 50V 0603	2923	2238 586 59812	100nF 20-80% 50V 0603
			2232	2238 586 59812	100nF 20-80% 50V 0603	2924	2238 586 59812	100nF 20-80% 50V 0603
			2233	2238 586 59812	100nF 20-80% 50V 0603	2925	2238 586 59812	100nF 20-80% 50V 0603
			2234	2238 586 59812	100nF 20-80% 50V 0603	2926	4822 126 14506	270pF 5% 50V 0603
			2235	3198 016 31020	1nF 10% 25V 0603	2927	4822 126 14506	270pF 5% 50V 0603
			2236	2020 021 91729	4.7µF 20% 35V	2928	4822 126 14506	270pF 5% 50V 0603
			2237	2238 586 59812	100nF 20-80% 50V 0603	2929	4822 126 14506	270pF 5% 50V 0603
			2238	2238 586 59812	100nF 20-80% 50V 0603	2930	2238 586 59812	100nF 20-80% 50V 0603
			2308	2238 586 59812	100nF 20-80% 50V 0603	2931	2020 021 91729	4.7µF 20% 35V
			2310	2238 586 59812	100nF 20-80% 50V 0603	2933	2238 586 59812	100nF 20-80% 50V 0603
			2403	2238 586 59812	100nF 20-80% 50V 0603	2934	2238 586 59812	100nF 20-80% 50V 0603
			2404	4822 124 23002	10µF 20% 16V	2935	4822 126 14506	270pF 5% 50V 0603
			2405	2238 586 59812	100nF 20-80% 50V 0603	2936	4822 126 14506	270pF 5% 50V 0603
			2406	2238 586 59812	100nF 20-80% 50V 0603	2937	4822 126 14506	270pF 5% 50V 0603
			2407	2238 586 59812	100nF 20-80% 50V 0603	2938	2238 586 59812	100nF 20-80% 50V 0603
			2408	4822 124 23002	10µF 20% 16V	2939	2020 021 91729	4.7µF 20% 35V
			2409	2238 586 59812	100nF 20-80% 50V 0603	2940	2238 586 59812	100nF 20-80% 50V 0603
6500	4822 130 80622	BAT54						
6900	4822 130 80622	BAT54						
</								

11. Revision List

11.1 3122 785 13321

- May 19th 2003.
Added Digital Board Chrysalis 2.1.
The Digital Board Chrysalis 2.1_E1 replaces Digital Board 1.5
Empress and DVIO 1.8 board in DVDR75/0x1.
The Digital Board Chrysalis 2.1_E2 replaces Digital Board 1.5
Empress in DVDR70/0x1.

11.2 3122 785 13322

- Sep 22th 2003.
Added parts for drive AV3 / VAD8031
The AV3 is used as alternative to the AV2 / VAE8020.